LANSDALE Semiconductor, Inc.

ML145040
ML145041
8-Bit A/D Converters With Serial Interface

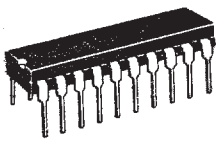
Silicon-Gate CMOS
SEMICONDUCTOR TECHNICAL DATA

Legacy Device: *Motorola MC145040, MC145041*

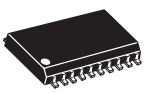
The ML145040 and ML145041 are low-cost 8-bit A/D Converters with serial interface ports to provide communication with microprocessors and microcomputers. The converters operate from a single power supply with a maximum nonlinearity of ± 1/2 LSB over the full temperature range. No external trimming is required.

The ML145040 allows an external clock input (A/D CLK) to operate the dynamic A/D conversion sequence. The ML145041 has an internal clock and an end–of–conversion signal (EOC) is provided.

- Operating Voltage Range: V_{DD} = 4.5 to 5.5 Volts
- Successive Approximation Conversion Time:
  ML145040 – 10 µs (with 2 MHz A/D CLK)
  ML145041 – 20 µs Maximum (Internal Clock)
- 11 Analog Input Channels with Internal Sample and Hold
- 0- to 5-Volt Analog Input Range with Single 5-Volt Supply
- Ratiometric Conversion
- Separate V_{ref} and V_{AG} Pins for Noise Immunity
- Wide V_{ref} Range
- No External Trimming Required
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- TTL/NMOS–Compatible Inputs May be Driven with CMOS
- Outputs are CMOS, NMOS or TTL Compatible
- Very Low Reference Current Requirements
- Low Power Consumption: 11 mW
- Internal Test Mode for Self Test



P DIP 20 = RP
CERAMIC PLASTIC
CASE 732 CASE 738



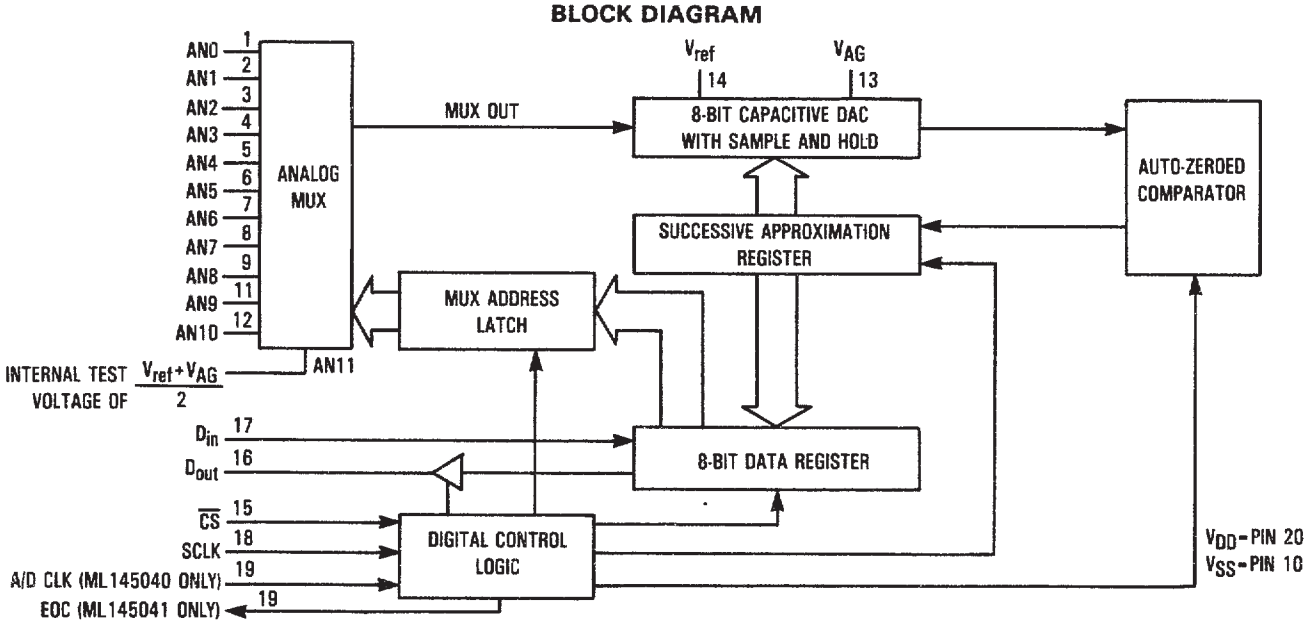
SO 20W = -6P
SOG
CASE 751D

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 20	MC145040P	ML145040RP
SO 20W	MC145040DW	ML145040-6P
P DIP 20	MC145041P	ML145041RP
SO 20W	MC145041DW	ML145041-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

BLOCK DIAGRAM



MICROWIRE is a trademark of National Semiconductor.

MAXIMUM RATINGS* (For all product grades)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +7.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD} + 0.1	V
V_{AG}	Analog Ground	V_{SS} − 0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS} − 1.5 to V_{DD} + 1.5	V
V_{out}	DC Output Voltage	V_{SS} − 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD},I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

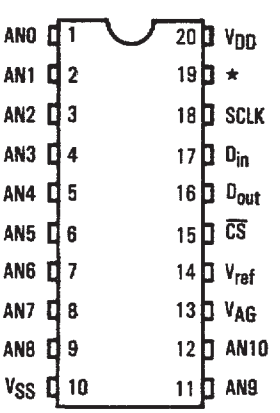
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.) Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits for all product grades)

Symbol	Parameter	Suffix				Unit
		L1	L2	P1, FN1	P2, FN2	
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG} + 2.5 to V_{DD}	V_{DD}	V_{AG} + 2.5 to V_{DD}	V_{DD}	V
V_{AG}	Analog Ground (Note 1)	V_{SS} to V_{ref} − 2.5	V_{SS}	V_{SS} to V_{ref} − 2.5	V_{SS}	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
T_A	Operating Temperature	−55 to +125	−55 to +125	−40 to +85	−40 to +85	°C

NOTES:
1. Reference voltages down to 1.0 V ($V_{ref} - V_{AG} = 1.0$ V) are functional, but the A/D Converter Electrical Characteristics are not guaranteed.
2. $V_{SS} \le V_{AI} \le V_{AG}$ produces an output of $00 and $V_{ref} \le V_{AI} \le V_{DD}$ produces an output of $FF. See V_{AG} and V_{ref} pin descriptions.

PIN ASSIGNMENTS



★NOTE:
A/D CLK (ML145040)
EOC (ML145041)

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	$I_{out} = -200\ \mu A$ $I_{out} = -100\ \mu A$ $I_{out} = -20\ \mu A$	2.4 2.4 $V_{DD} - 0.1$	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	$I_{out} = +1.6$ mA $I_{out} = +1.0$ mA $I_{out} = 20\ \mu A$	0.4 0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, A/D CLK)	$V_{in} = V_{SS}$ or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out} = V_{SS}$ or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	$V_{in} = V_{SS}$ or V_{DD}, All Outputs Open ML145040: A/D CLK = 2 MHz	2	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref} = V_{DD}$ $V_{AG} = V_{SS}$	10	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input. (AN0-AN10)	$V_{AI} = V_{SS}$ to V_{DD}, L1 and L2 Suffix P1,P2, FN1, FN2 Suffix	±1000 ±400	nA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(ML145040: 1 MHz ≤ A/D CLK ≤ 2 MHz, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Minimum Resolution	Number of bits resolved by the A/D	8	Bits
Maximum Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	± ½	LSB
Maximum Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	± ½	LSB
Maximum Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	± ½	LSB
Maximum Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	± ½	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion ML145040 ML145041	20 20	A/D CLK cycles μs
Maximum Data Transfer Time	Total time to transfer digital serial data into and out of the device	8	SCLK cycles
Maximum Sample Acquisition Time	Analog input acquisition time window ML145040: A/D CLK = 2 MHz, SCLK = 1 MHz ML140541: SCLK = 1 MHz	 10 16	μs
Maximum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion ML145040: A/D CLK = 2 MHz, SCLK = 1 MHz ML145041: SCLK = 1 MHz	 24 40	μs
Maximum Sample Rate	Rate at Which Analog Inputs May be Sampled ML145040: A/D CLK = 2 MHz, SCLK = 1 MHz ML145041: SCLK = 1 MHz	 41 25	kHz

AC ELECTRICAL CHARACTERISTICS ($t_r = t_f = 6$ ns, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Maximum Clock Frequency (50% Duty Cycle), SCLK		1.1	MHz
1 (same as SCLK)	f	Clock Frequency (50% Duty Cycle), A/D CLK (ML145040)	Minimum Maximum	1.0 2.1	MHz
1,7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		400	ns
1,7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2,7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}		150	ns
2,7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}	ML145040 ML145041	3 A/D CLK cycles + 400 ns 3.4	μs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		400	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4,7,8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	ML145041	400	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	ML145040 ML145041	3 A/D CLK cycles + 800 ns 3.8	μs
5	t_h	Minimum Hold Time, 8th SCLK to $\overline{CS}$		0	ns
6,8	t_{PHL}	Maximum Propagation Delay, 8th SCLK to EOC		500	ns
1	t_r, t_f	Maximum Input Rise and Fall Times, Any Digital Input		100	ns
1,4,6,7,8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
—	C_{in}	Maximum Input Capacitance	AN0-AN10 A/D CLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
—	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

SWITCHING WAVEFORMS

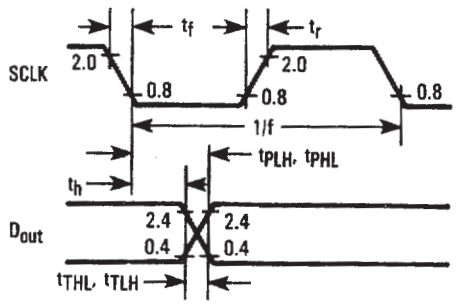


Figure 1

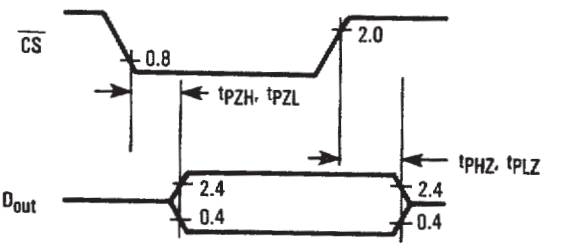


Figure 2

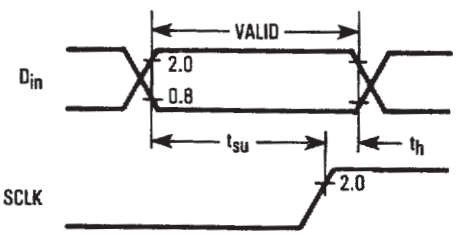


Figure 3

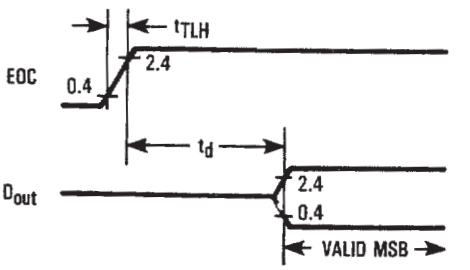


Figure 4

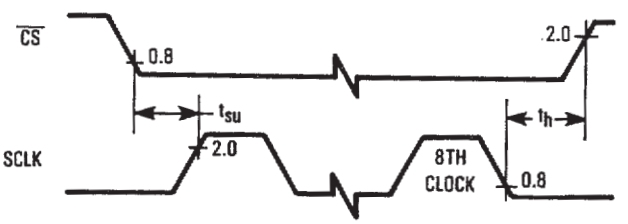


Figure 5

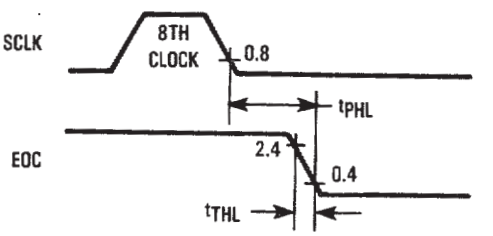


Figure 6

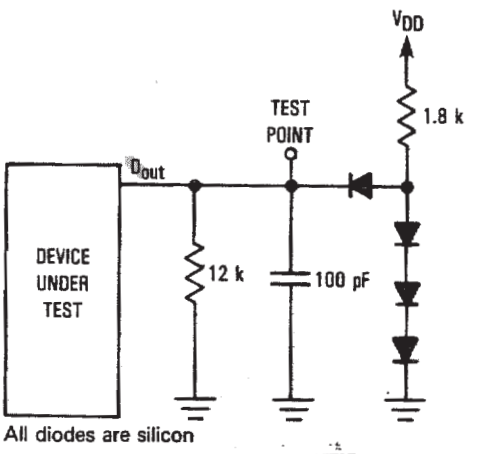


Figure 7. Test Circuit

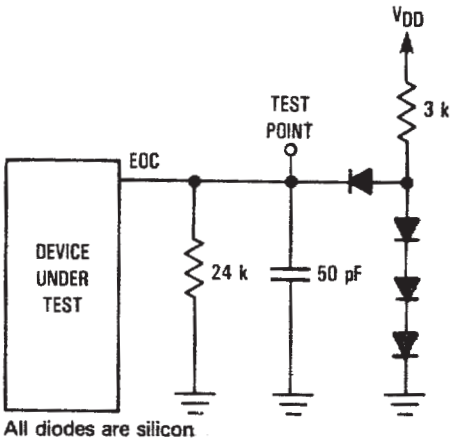


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

CS (Pin 15)

Active–low chip select input. $\overline{CS}$ provides three–state control of D_{out}. $\overline{CS}$ at a high logic level forces D_{out} to a high–impedance state. IN addition, the device recognizes the falling edge of $\overline{CS}$ as a serial interface reset to provide synchronization between the MPU and the A/D converter's serial data stream. To prevent a spurious reset from occurring due to noise on the $\overline{CS}$ input, a delay circuit has been included such that a $\overline{CS}$ signal of duration ≤1 A/D CLK period (ML145040) or ≤500 ns (ML145041) is ignored. A valid $\overline{CS}$ signal is acknowledged when the duration is ≥3 A/D CLK periods (ML145040) or ≥3 µs (ML145041)

CAUTION

A reset aborts a conversion sequence, therefore high–to–low transitions on $\overline{CS}$ must be avoided during the conversion sequence.

Dout (Pin 16)

Serial data output of the A/D conversion result. The 8–bit serial data stream begins with the most significant bit and is shifted out on the high–to–low transition of SCLK. D_{out} is a three–state output as controlled by $\overline{CS}$. However, D_{out} is forced into a high–impedance state after the eighth SCLK, independent of the state of $\overline{CS}$. See Figures 9, 10, 11, or 12.

D_{in} (Pin 17)

Serial data input. The 4–bit serial data stream begins with the most significant address bit of the analog mux and is shifted in on the low–to–high transition of SCLK.

SCLK (Pin 18)

Serial data clock. THe serial data register is completely static, allowing SCLK rates down to DC in a continuos or intermittent mode. SCLK need not be synchronous to the A/D CLK (ML145040) or the internal clock (ML145041). Eight SCLK cycles are required for each simultaneous data transfer, the low–to–high transition shifting in the new address and the high–to–low transition shifting out the previous conversion result. The address is acquired during the first four SCLK cycles, with the interval produced by the remaining four cycles being used to begin charging the on–chip sample–and–hold capacitors. After the eighth SCLK, the SCLK input is inhibited (on–chip) until the conversion is complete.

A/D CLK (Pin 18, ML145040 only)

A/D clock input. This pin clocks the dynamic A/D conversion sequence, and may be asynchronous and unrelated to SCLK. The signal must be free running, and may be obtained from the MPU system clock. Deviations from a 50% duty cycle can be tolerated if each half period is > 238 ns.

EOC (Pin 19, ML145041 only)

End–of–conversion output. EOC goes low on the negative edge of the eighth SCLK. The low–to–high transition of EOC indicates the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10 (Pins 1-9, 11, 12)

Analog multiplexer inputs. The input AN0 is addressed by loading $0 into the serial data input, D_{in}. AN1 is addressed by $1, AN2 by $2…AN10 via $A. The mux features a break–before–make switching structure to minimize noise injection into the analog inputs. The source impedance driving these inputs must be ≤ 10 kΩ. NOTE: $B addresses an on–chip test voltage of $(V_{ref} + V_{AG})/2$, and produces an output of $80 if the converter is functioning properly. However, a ± 1 LSB deviation from $80 occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref} or V_{AG}.

POWER AND REFERENCE PINS

VSS and VDD (Pins 10 and 20)

Device supply pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. $V_{DD} - V_{SS}$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. Excessive inductance in the V_{DD} or V_{SS} lines as on automatic test equipment, may cause A/D offsets > ½ LSB.

V_{AG} and V_{ref} (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages ≥ V_{ref} produce an output of $FF and input voltages ≤ V_{AG} produce an output of $00. CAUTION: THe analog input voltage must be ≥ V_{SS} and ≤ V_{DD}. The A/D conversion result is ratiometric to $V_{ref} - V_{AG}$ as shown by the formula:

$$V_{in} = \left[\frac{\text{output code}}{\$FF} \times (V_{ref} - V_{AG})\right] + \frac{\text{quantizing}}{\text{error}} + \frac{\text{linearity}}{\text{error}}$$

V_{ref} and V_{AG} should be as noise–free as possible to avoid degradation of the A/D conversion. Noise on either of these pins will couple 1:1 to the analog input signal i.e. a 20 mV change in V_{ref} can cause a 20 mV error in the conversion result. Ideally V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers.

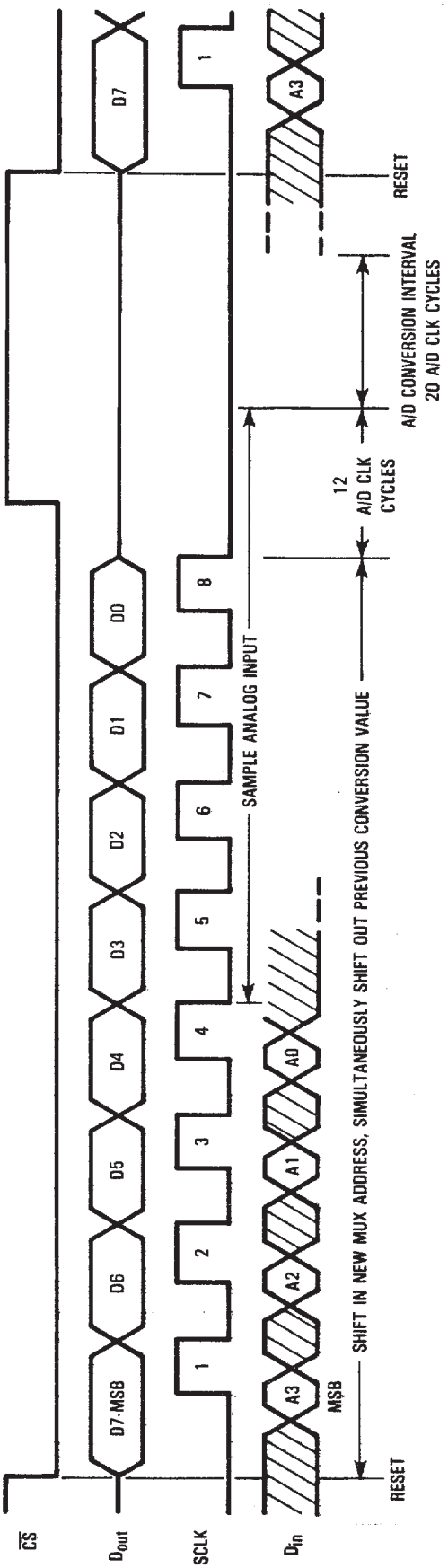


Figure 9. ML145040 Timing Diagram Utilizing $\overline{CS}$ to Three-State Dout

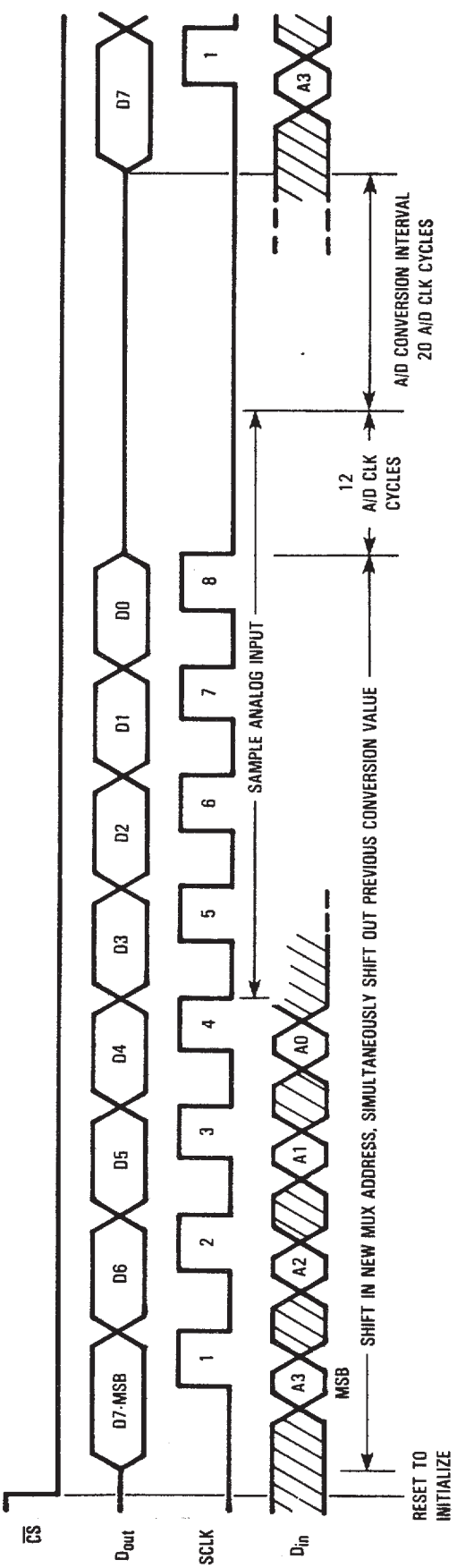


Figure 10. ML145040 Timing Diagram Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

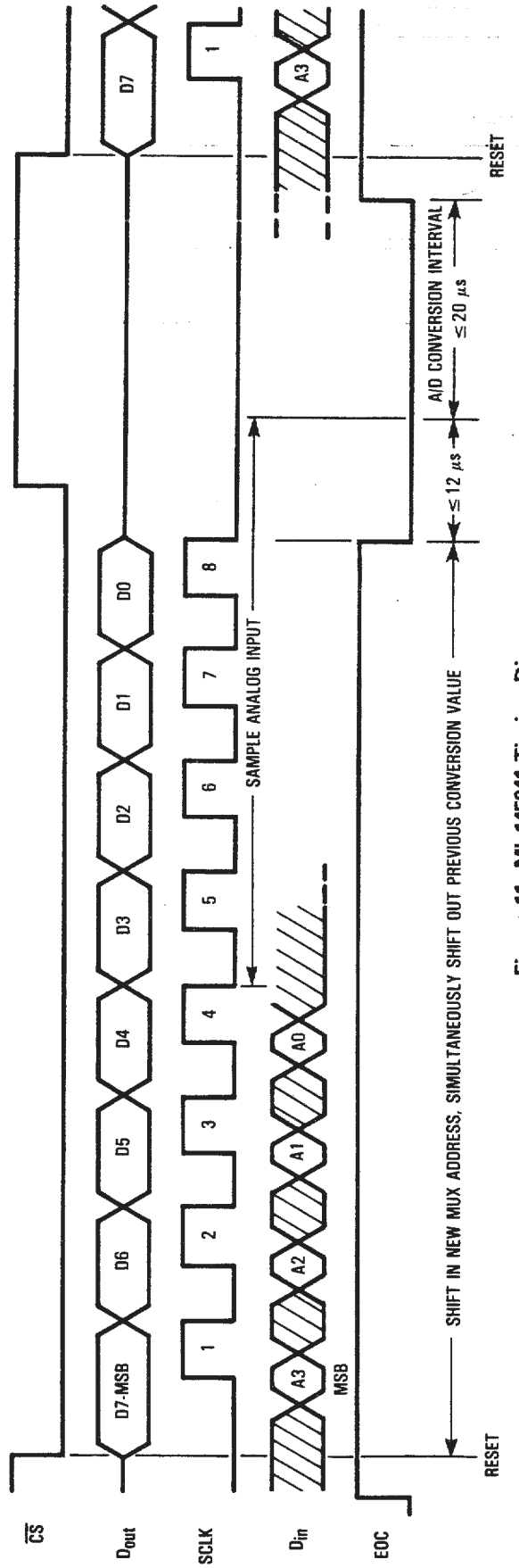


Figure 11. ML145041 Timing Diagram
Utilizing $\overline{CS}$ to Three-State D_{out}

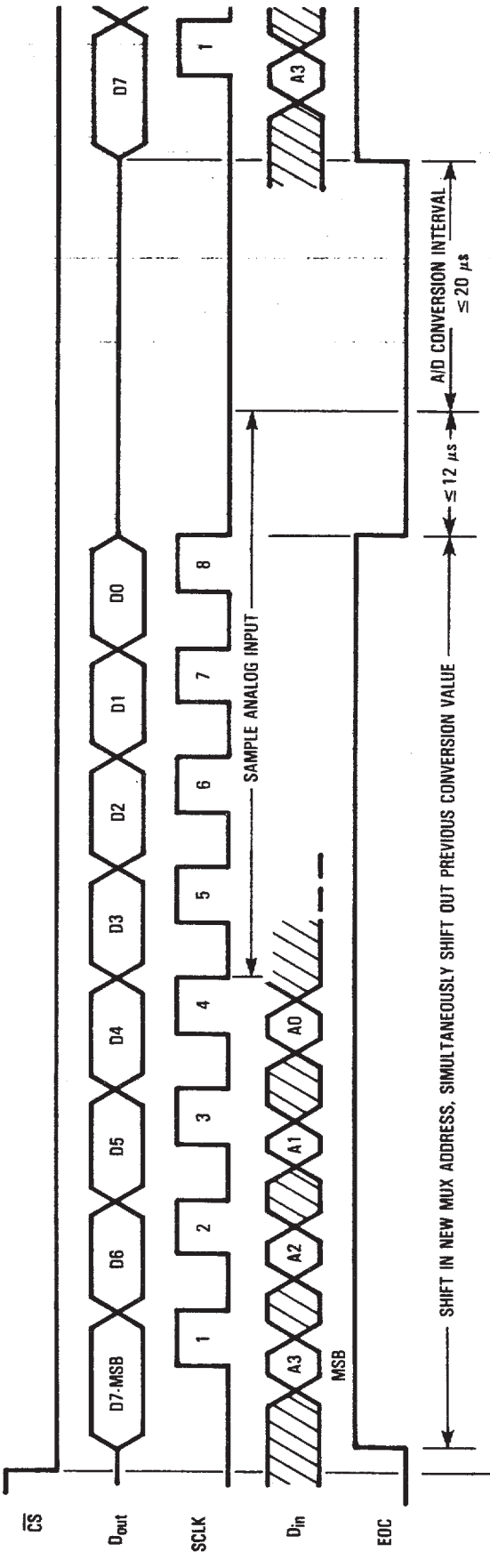


Figure 12. ML145041 Timing Diagram
Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

Legacy Applications Information

DESCRIPTION

This example application of the ML145040/ML145041 ADCs interfaces three controllers to a microprocessor and processes data in real–time for a video game. The standard joystick X–axis (left/right) and Y–axis (up/down) controls as well as engine thrust controls are accommodated

Figure 13 illustrates how the ML145040/ML145041 is used as a cost–effective means to simplify this type of circuit design. Utilizing one ADC, three controllers are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SP) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} to V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

Both the ML145040 and ML145041 will accommodate all the analog system inputs. The ML145040, when used with a 2 MHz MCU, takes 24 μs to sample the analog input, perform the conversion, and transfer the serial data at 1 MHz. Thirty–two A/D Clock cycles (2 MHz at input pin 19) must be provided and counted by the MCU after the eighth SCLK before reading the ADC results. The ML145041 has the end–of–conversion (EOC) signal (at output pin 19) to define when data is ready, but has a slower 40 μs cycle time. However, the 40 μs is constant for serial data rates of 1 MHz independent of the MCU clock frequency. Therefore, the ML145041 may be used with CMOS MCU operating at the reduced clock rates to minimize power consumption without sacrificing ADS cycle times, with EOC being used to generate an interrupt. The ML145041 may also be used with MCU's which do not provide a system clock.)

ANALOG DESIGN CONSIDERATIONS

Controllers with output impedances of less than 10 kilohms may be direcly interfaced to these ADCs, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 13, the V_{ref} and controller ouput lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil–shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair of the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for this application. The reference circuitry may be as simple as tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 14.) However, the system power supply noise may require that a seperate supply be used for the voltage reference. This supply must provide source current for V_{ref} as well as current for the controller potentionmeters.

A bypass capacitor across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The nine analog inputs, AN0 through AN8, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to to be read to the ADC, simultaneously. All nine inputs may be scanned in a minimum of 216 μs (ML145040) or 360 μs (ML145041).

If the design in realized using the ML145040, 32 A/D clock cycles (at pin 19) must be counted by the MCU to allow time for A/D conversion. The designer utilizing the ML145041 has the end–of–conversion signal (at pin 19) to define the conversion interval. EOC may be used to generated an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data, and transfer the information to the video circuitry for updating the display.

Legacy Applications Information

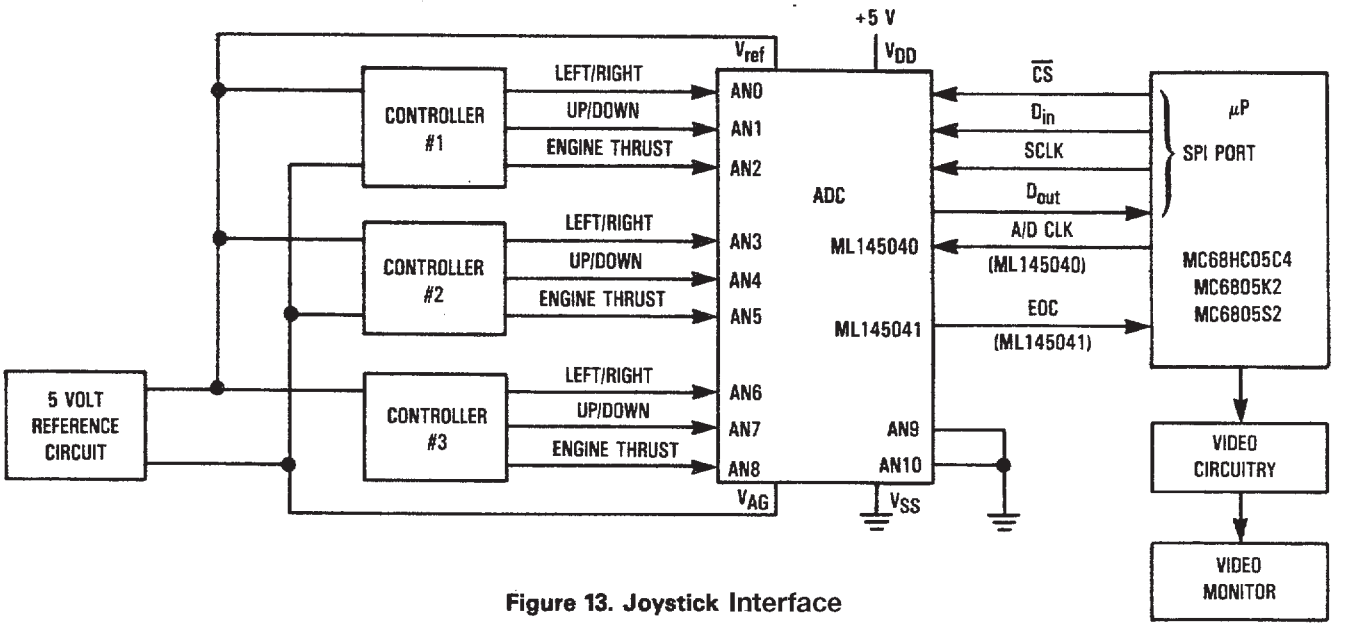


Figure 13. Joystick Interface

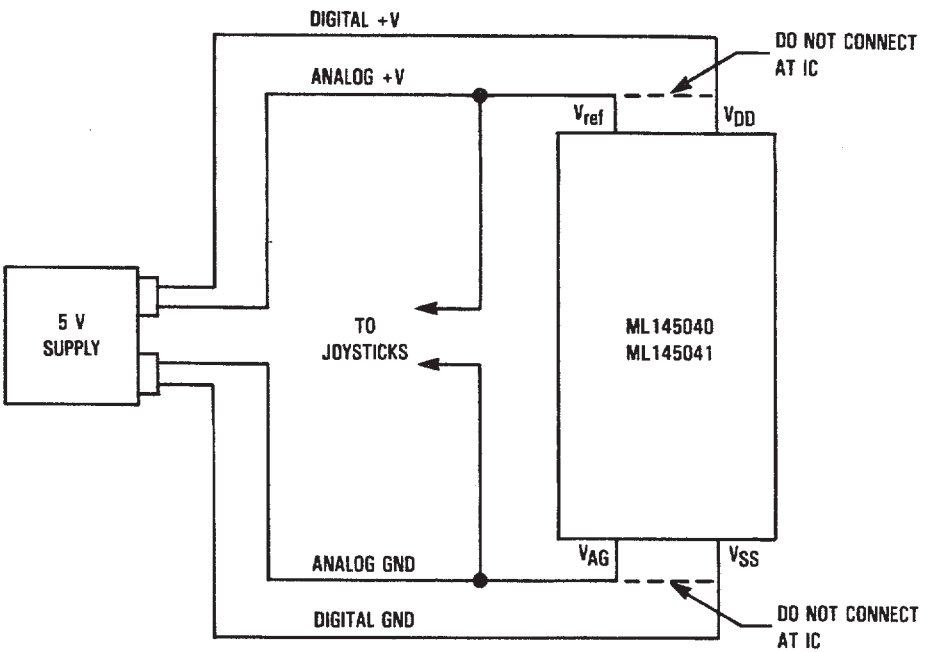
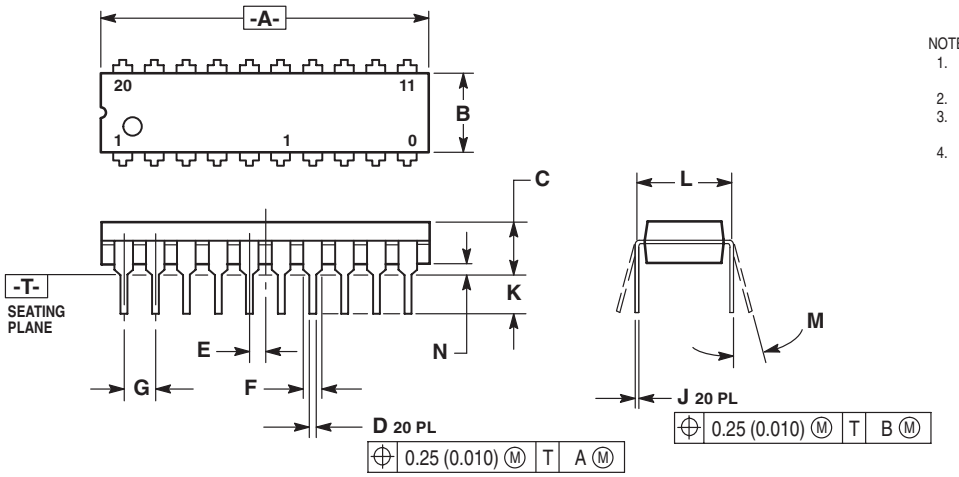


Figure 14. Alternate Configuration Using the Digital Supply for the Reference Voltage

OUTLINE DIMENSIONS

P DIP 20 = RP
(ML145040RP, ML145041RP)
CASE 738-03

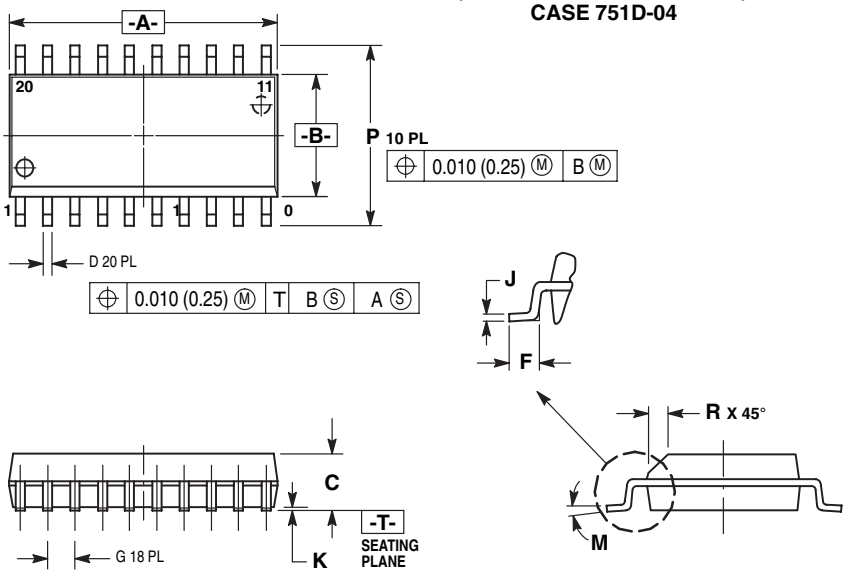


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

SOG 20W = -6P
(ML145040-6P, ML145041-6P)
CASE 751D-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029