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28:4 LVDS Receiver

GENERAL DESCRIPTION

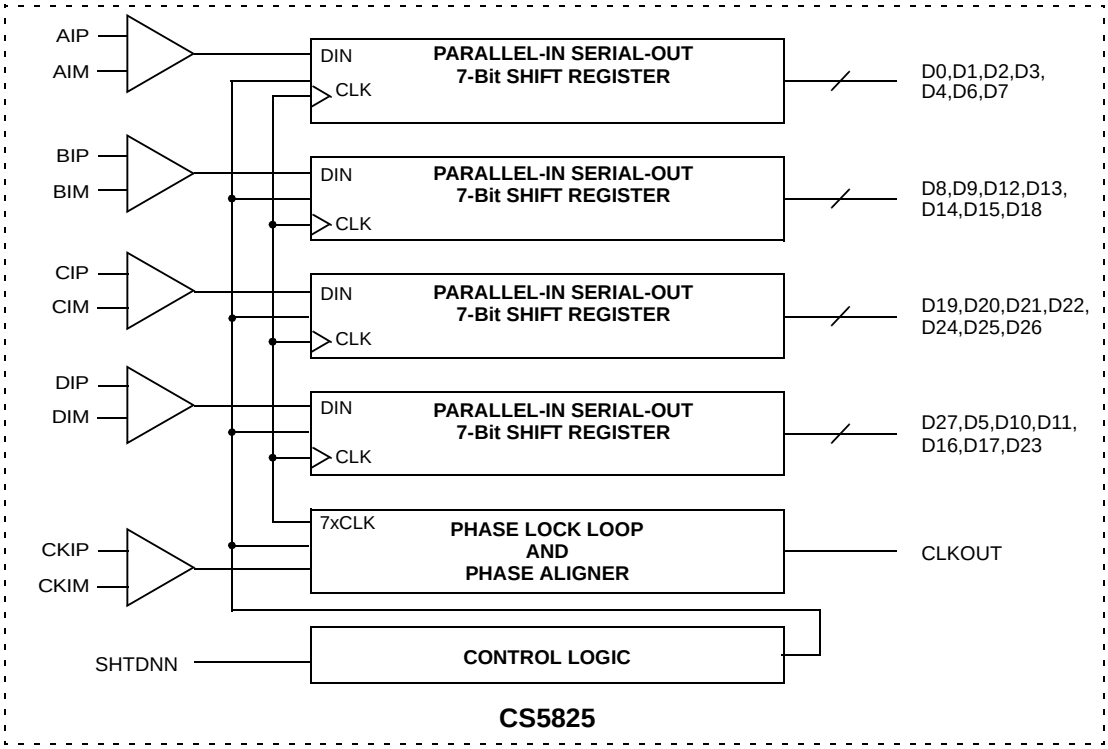
CS5825 receives four LVDS data channels and one LVDS clock channel. Each data channel is deserialized into 7-bit parallel data bus for output. The clock channel is used for frame sync and fed into an internal PLL that generates the 7X serial clock used in the deserializer. A digital phase alignment circuit can generate the sampling clock of the deserializer front-end. The frame sync clock aligned to the output 7-bit data is also output for timing reference.

CS5825 supports open-safe design of LVDS when the input is not connected to LVDS drivers and the receiver outputs are forced low. Putting CS5825 into inhibit mode by a shutdown control (SHTDNN) signal can lower power consumption.

FEATURES

- Four 7-bit serial data LVDS channels and one clock LVDS channel.
- Compatible with ANSI TIA/EIA-644 LVDS standard.
- Wide serial clocking speed ranges from 31MHz to 68MHz.
- Support open-safe LVDS design.
- Fully integrated on-chip PLL and digital phase alignment provide accurate deserializer operation.
- Support power-down mode.
- 5V/3.3V tolerant data input.
- Single 3.3V supply operation.
- CMOS low power consumption.
- Functional compatible with DS90CF384 and SN75LVDS86.
- Available in 56-pin TSSOP package.

BLOCK DIAGRAM



Century Semiconductor, Inc.
Taiwan:
No. 2, Industry East Rd. 3rd,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

USA:
1485 Saratoga Ave. #200
San Jose, CA, 95129
Tel: 408-973-8388 Fax: 408-973-9388

Sales@century-semi.com
Sales@century-semi.com.tw
www.century-semi.com

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PIN CONNECTION DIAGRAM

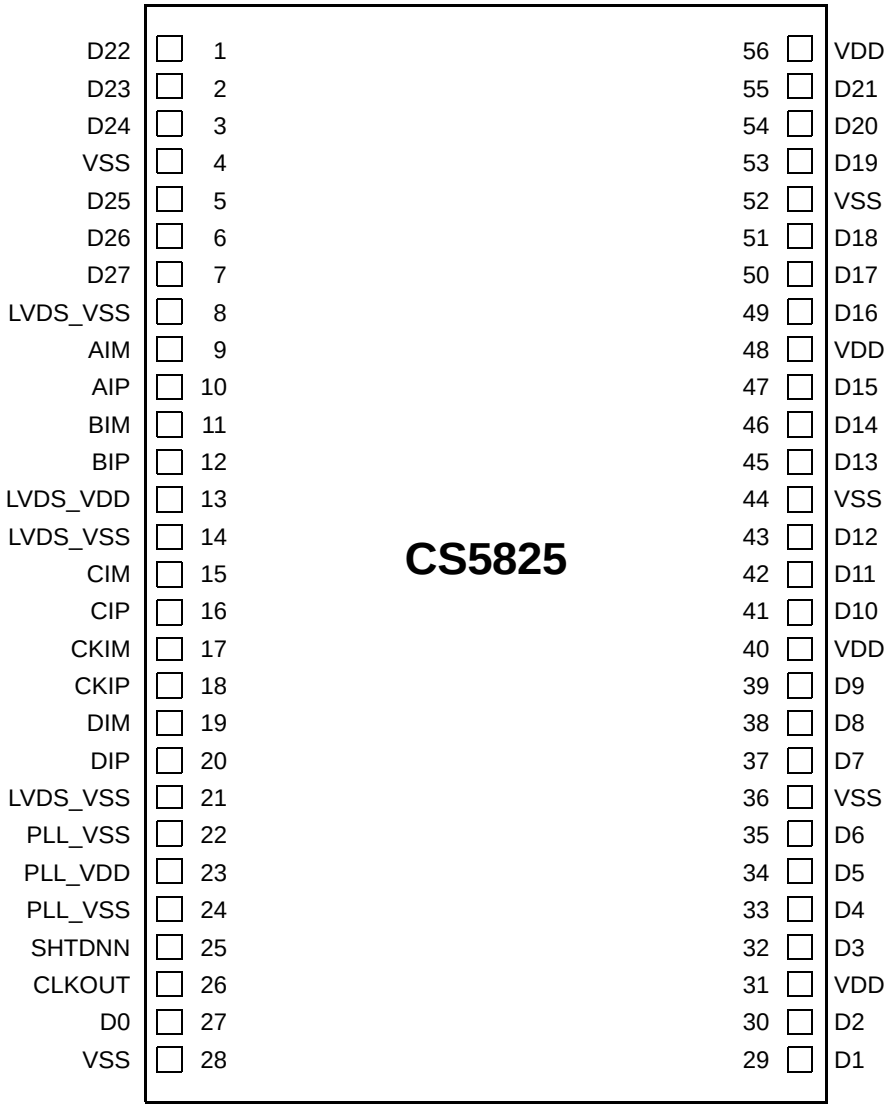

Figure-1 56-pin TSSOP

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PIN DESCRIPTION

Name	Pin	Description
AIP, AIM	I	LVDS data channel A input. These are differential LVDS inputs for A channel corresponds to D0, D1, D2, D3, D4, D6, D7. AIP is the positive data input and AIM is the negative input.
BIP, BIM	I	LVDS data channel B output. These are differential LVDS inputs for B channel corresponds to D8, D9, D12, D13, D14, D15, D18.
CIP, CIM	I	LVDS data channel C output. These are differential LVDS outputs for C channel corresponds to D19, D20, D21, D22, D24, D25, D26.
DIP, DIM	I	LVDS data channel C output. These are differential LVDS outputs for D channel corresponds to D27, D5, D10, D11, D16, D17, D23.
CKIP, CKIM	I	LVDS clock channel input. These are differential LVDS input for the frame sync clock. The clock is sent to an on-chip PLL to generate 7X serial clock; An phase aligner is used to align the deserializer clock.
D0,D1,D2,D3,D4, D6, D7	O	Parallel data output for LVDS channel A. D[0] is LSB and D[7] is MSB. MSB is shifted in first.
D8,D9,D12,D13, D14,D15,D18	O	Parallel data output for LVDS channel B. D[8] is LSB and D[18] is MSB.
D19,D20,D21,D22 ,D24,D25,D26	O	Parallel data output for LVDS channel C. D[19] is LSB and D[26] is MSB.
D27,D5,D10,D11, D16,D17,D23	O	Parallel data output for LVDS channel C. D[19] is LSB and D[23] is MSB.
CLKOUT	O	Parallel data clock output. This clock signal recovered clock for data output reference. The falling edge should be used as the strobe for the next stage.
SHTDNN	I	Shutdown control (low active). When SHTDNN is low, the internal PLL is put into inhibit mode and all data outputs are forced low. This also resets all internal registers. For normal operation, SHTDNN should be set to high.
VDD	P	Positive power supply for TTL outputs. A 3.3V supply should be used.
VSS	P	Negative power supply. Connect to 0V.
LVDS_VDD	P	Positive power supply for LVDS inputs.
LVDS_VSS	P	Negative power supply for LVDS inputs.
PLL_VDD	P	Positive power supply for PLL.
PLL_VSS	P	Negative power supply for PLL.

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FUNCTIONAL DESCRIPTION

Serial-In Parallel-Out 7-Bit Shift Register

It receives the serial data from the transmitter. It uses the 7xclk to strobe the serial data and sends 7-bit parallel data with input clock's frequency.

Phase Lock Loop and Phase Aligner

The PLL generates the seven times input clock which is used for deserialized. The phase aligner is used for synchronous the input clock and output.

Control logic

There are two modes in this circuit. One is normal mode, and another is power down mode. Two modes are controlled by the control signal "SHTDNN". If SHTDNN is high, the circuit is in the normal mode, else if low, the circuit is in the power down mode. In the power down mode, every block is off to make sure the least power consumption.

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Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
$V_{IH}(\overline{SHTDN})$	High-level input voltage	2	-	-	V
$V_{IL}(\overline{SHTDN})$	Low-level input voltage	-	-	0.8	V
	Receiver input range	0	-	2.4	V
T_A	Operating free-air temperature	0	-	70	°C

Timing Requirements

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Cycle time, input clock*	14.7	t_c	32.4	ns
t_{su1}	Setup time, input	600	-	-	ps
t_{h1}	Hold time, input	600	-	-	ps

Note: Parameter t_c is defined as the mean duration of a minimum of 32000 clock cycles.

Electrical Characteristics over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IT+}	Differential input high threshold voltage		-	-	100	mV
V_{IT-}	Differential input low threshold voltage		-100	-	-	mV
V_{OH}	High-level output voltage	I_{OH} = -4mA	2.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = 4mA	-	-	0.4	V
I_{CC}	Quiescent current (average)	Disabled (power down mode), All inputs open	-	280	-	µA
		Enabled, AnP = 1V, AnM = 1.4V, t_c = 15.38ns	-	58	72	mA
		Enabled, C_L = 8 pF, Grayscale pattern, t_c = 15.38ns	-	69	-	mA
		Enabled, C_L = 8 pF, Grayscale pattern, t_c = 15.38ns	-	94	-	mA
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$	-	-	±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0	-	-	±20	µA
I_I	Input current (LVDS input terminals A and CLKIN)	$0 \le V_1 \le 2.4V$	-	-	±10	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}	-	-	±10	µA

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Switching Characteristics over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{su2}	Setup time, D0 - D20 valid to CLKOUT↓	C_L = 8pF (Figure-3)	5	-	-	ns
t_{h2}	Hold time, CLKOUT↓ to D0 - D20 valid		5	-	-	ns
t_{RSKM}	Receive input skew margin	t_c = 15.38 ns (±0.2%), Input clock jitter < 50 ps (Figure-4)	490	-	-	ps
t_d	Delay time, CLKIN↑ to CLKOUT ↓	t_c = 15.38 ns (±0.2%), C_L = 8 pF	-	3.7	-	ns
$\Delta t_{c(o)}$	Cycle time, change in output clock period#		-	± 100	-	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to Dn valid	Figure-6	-	1	-	ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state	Figure-7	-	400	-	ns
t_t	Transition time, output (10% to 90% t_r or t_f)	CL = 8pF	-	3	-	ns
t_w	Pulse duration, output clock	-	-	0.43t_c	-	ns

Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
LHT	low to high transition time	-	2.2	5	ns
HLT	high to low transitions time	-	2.2	5	ns
Pos0	input strobe position for bit 0 (f = 65MHz)	0.7	1.1	1.4	ns
Pos1	input strobe position for bit 1 (f = 65MHz)	2.9	3.3	3.6	ns
Pos2	input strobe position for bit 2 (f = 65MHz)	5.1	5.5	5.8	ns
Pos3	input strobe position for bit 3 (f = 65MHz)	7.3	7.7	8.0	ns
Pos4	input strobe position for bit 4 (f = 65MHz)	9.5	9.9	10.2	ns
Pos5	input strobe position for bit 5 (f = 65MHz)	11.7	12.1	12.4	ns
Pos6	input strobe position for bit 6 (f = 65MHz)	13.9	14.3	14.6	ns
SKM	Rxin skew margin (f = 65MHz)	400	-	-	ps
COP	RxCLK OUT Period	14.7	-	32.2	ns
COH	RxCLK OUT high time (f = 65MHz)	7.5	-	-	ns
COL	RxCKK OUT low time (f = 65MHz)	3.5	-	-	ns
SRC	RxOUT setup to RxCLKOUT (f = 65MHz)	2.5	-	-	ns
HRC	RxOUT hold to RxCLKOUT (f = 65MHz)	2.5	-	-	ns
CCD	RxCLK In to RxCLK OUT delay	5	-	9	ns
PLLs	Phase Lock Loop set	-	-	10	ms
PDD	Power down delay	-	-	1	µs

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Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IRCCG	Receiver Supply Current	C_L= 8pF, f = 65MHz (Worst Case pattern)	-	-	-	mA
IRCCW	Receiver Supply Current	C_L = 8pF,f = 65MHz (Grayscale pattern)	-	-	-	mA
IRCCS	Receiver Power Down Supply Current	Power Down = Low	-	200	300	µA

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TIMING DIAGRAMS

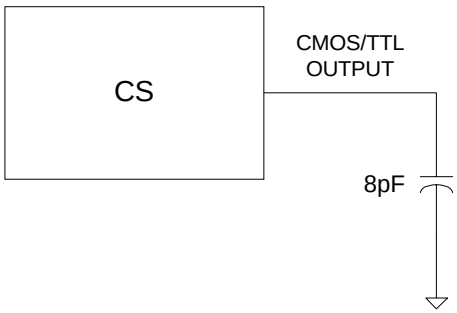

Figure-2 CMOS/TTL Output Load

Figure-3 CMOS/TTL Output Transition Times

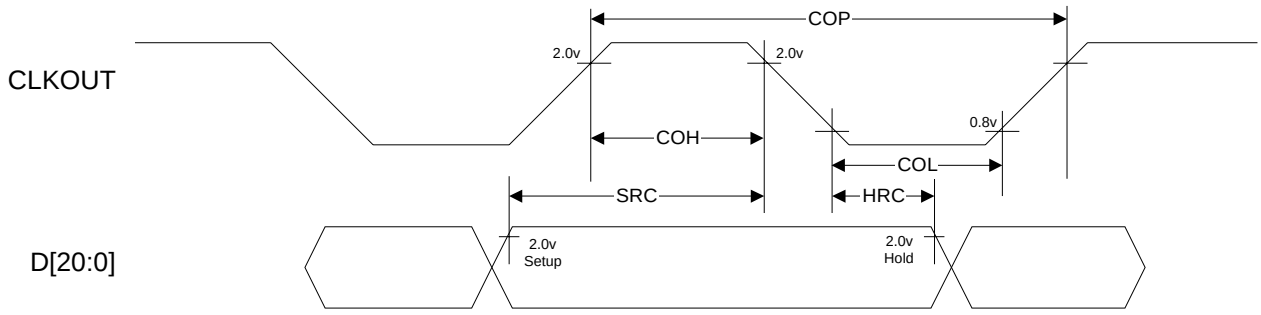

Figure-4 Setup/Hold and High/Low Times

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TEST PATTERN

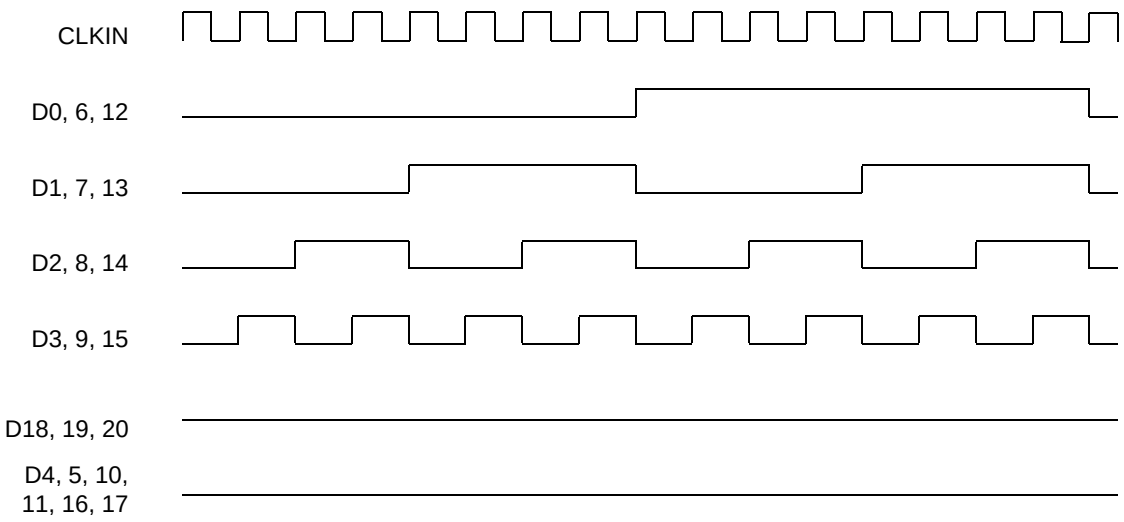

Figure-5 16-Grayscale Testing Pattern Waveforms

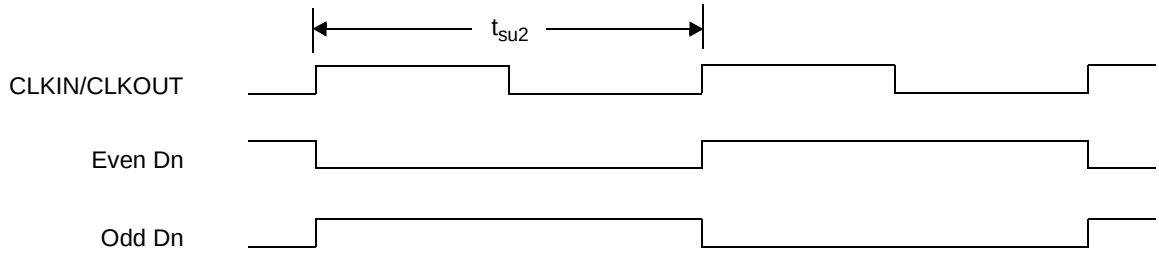

Figure-6 The Worst-case Testing Pattern Waveforms

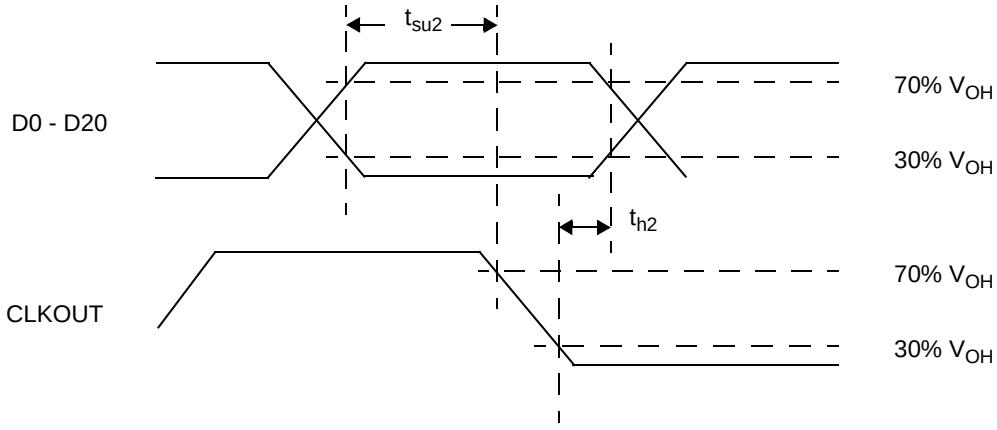

Figure-7 Setup and Hold Time Waveforms

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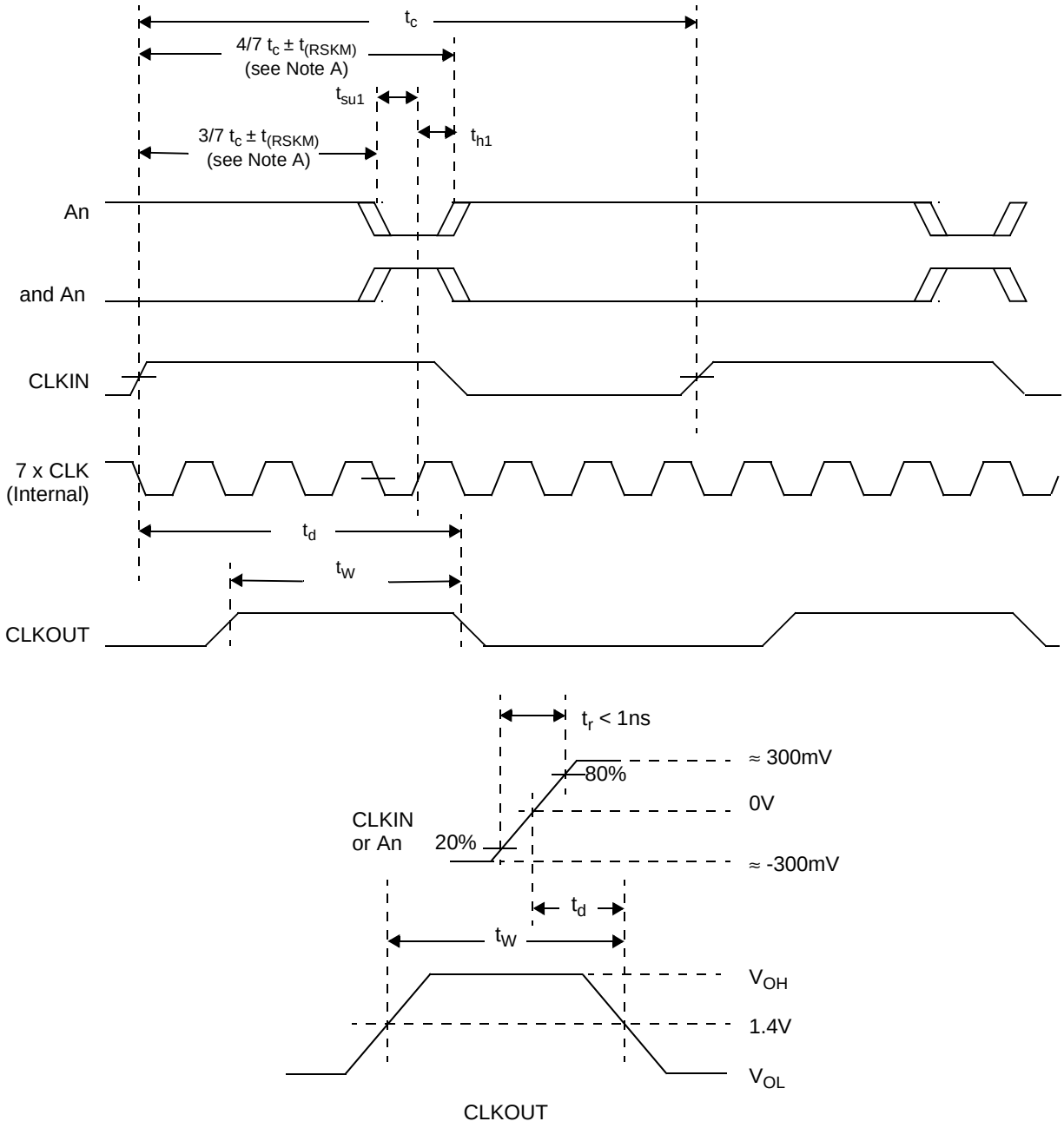
PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure-8 Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

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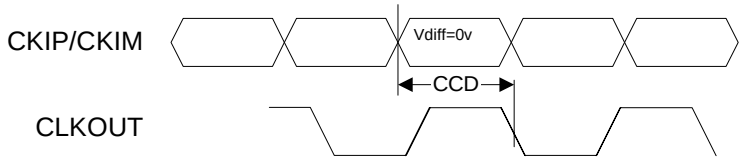

Figure-9 Clock-in to Clock-out Delay

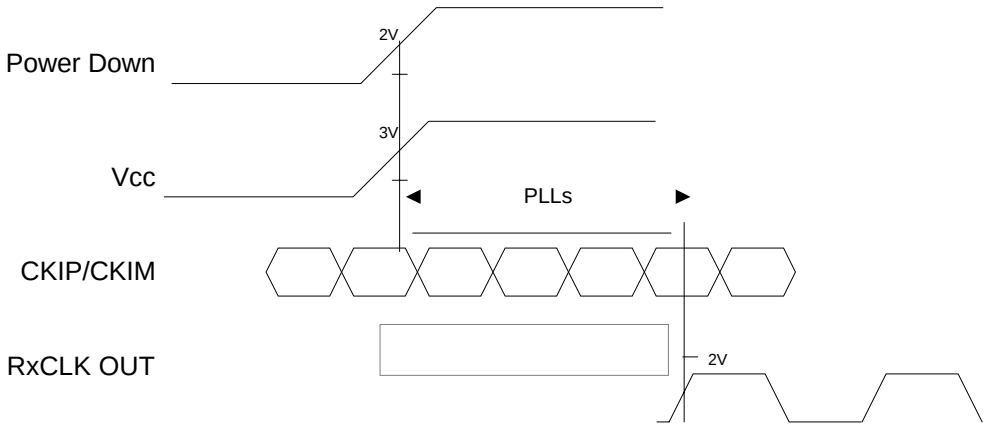

Figure-10 Phase Lock Loop Stable Time

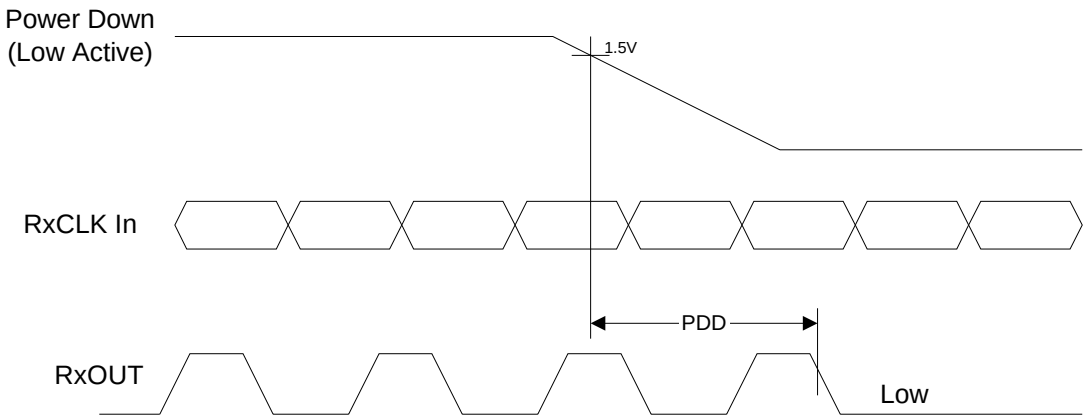

Figure-11 Power Down Delay

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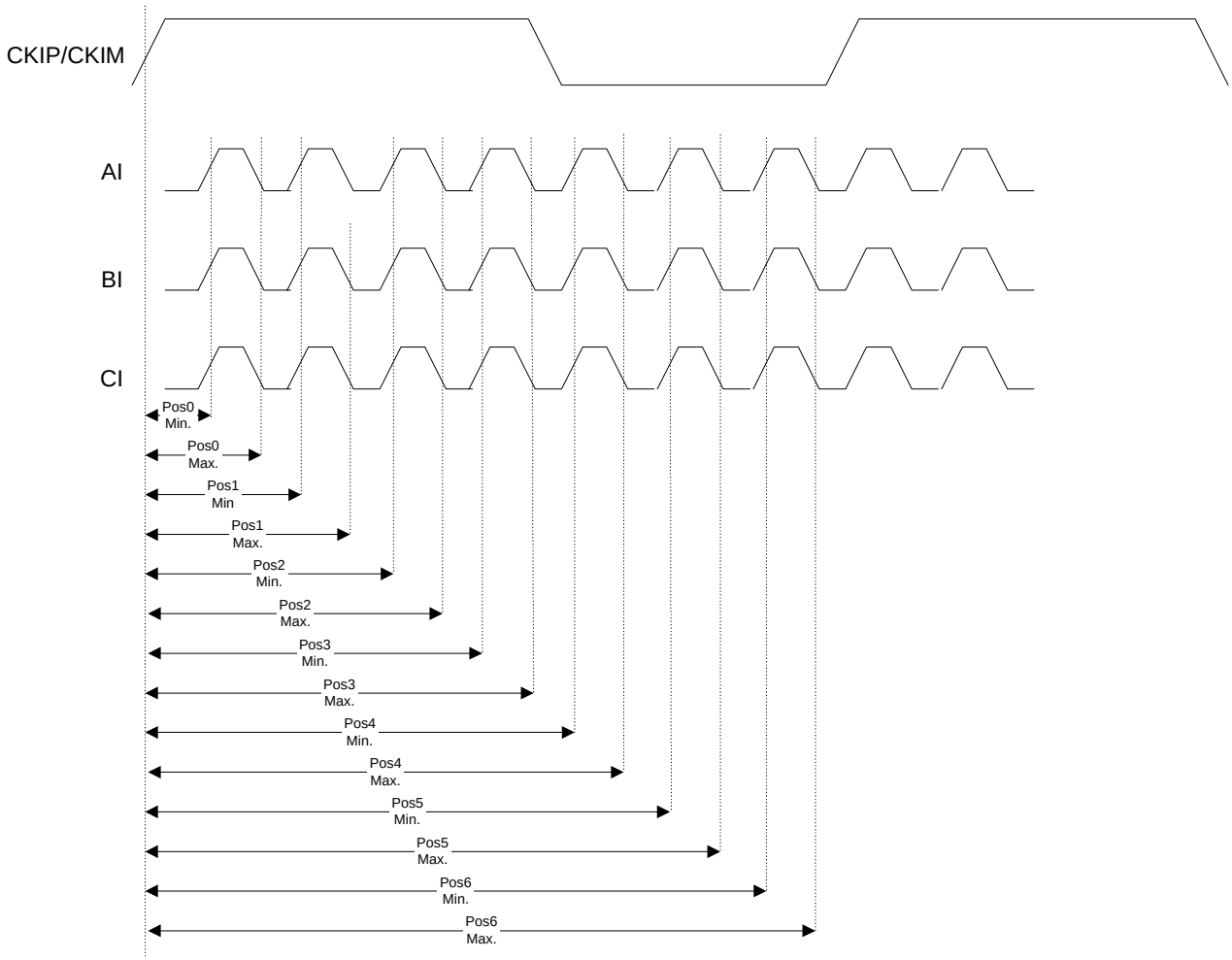

Figure-12 Strobe positions of LVDS inputs

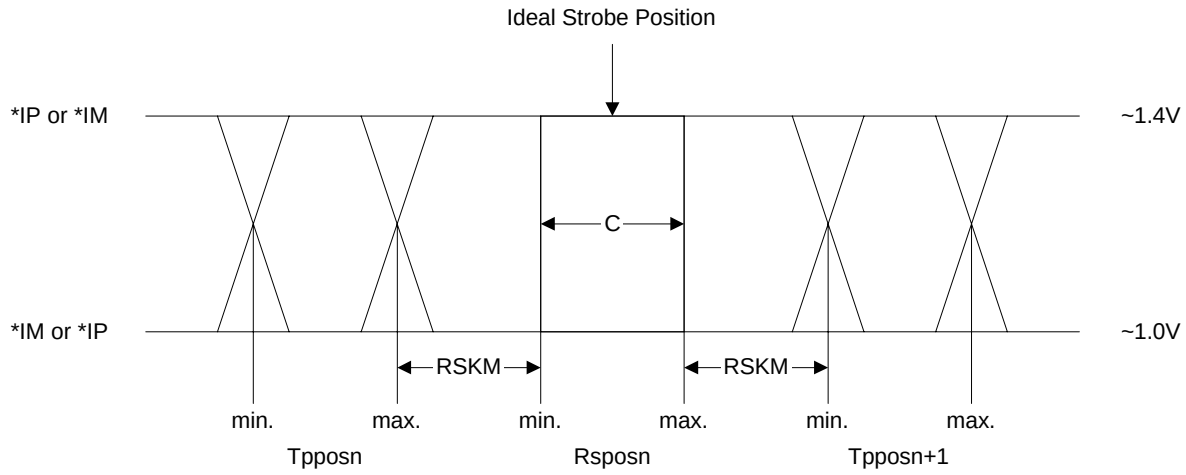

Figure-13 Skew Margin of LVDS data inputs

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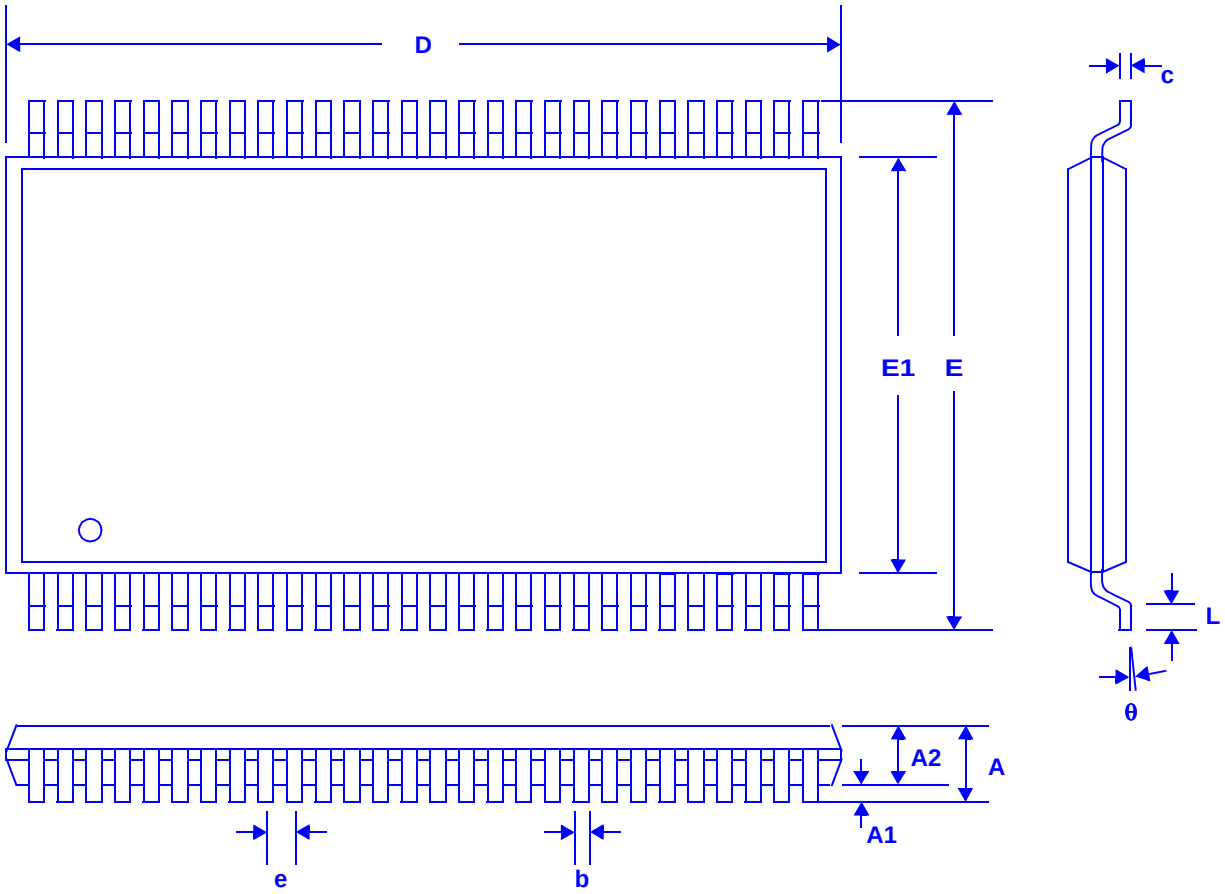
PACKAGE OUTLINE (56-pin TSSOP)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	-	1.20	0.041	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	-	0.90	-	-	0.035	-
b	0.17	0.20	0.27	0.007	0.008	0.010
c	0.09	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	7.80	8.10	8.40	0.307	0.319	0.330
E1	6.00	6.10	6.20	0.236	0.240	0.244
e	-	0.50	-	-	0.0197	-
L	0.50	-	0.75	0.020	-	0.030
θ	0°	-	7°	0°	-	7°