SPSS030A – DECEMBER 2000 – REVISED FEBRUARY 2001

- **Advanced, Catalog Speech Processor for High-Quality Sound, Capable of Unlimited Speech Duration Using External Memory**
- **Operates up to 12.32 MIPS**
- **Supports High-Quality Algorithms Such as MELP (1.0 Kbps – 3.5 Kbps at 8 kHz), CELP (3.0 Kbps – 11.2 kHz at 8 kHz Sampling Rate), ADPCM, Single Channel FM With CELP or MELP**
- **Speed and Pitch Shifting in MELP for Various Voice Effects**
- **Six Level Digital Gain Control**
- **4 User Configurable I/O's**
- **Very Low-Power Operation, Ideal for Hand-Held Devices**
- **Low-Voltage Operation, Sustainable by Three (3) Batteries**
- **Three Reduced Power Standby Modes, Less Than 10 μA in Deep-Sleep Mode**
- **Resistor-Trimmed Oscillator or 32.768-kHz Crystal Reference Oscillator**
- **Direct Speaker Drive (32 Ω) (PDM)**
- **Interrupt Driven, 4- or 8-Bit Parallel Data Transfer Protocol**
- **Available in Die Form or 64-Pin PM Package**

description

The MSP53C691 is a standard slave synthesizer from Texas Instruments that accepts compressed speech data from other microprocessors/microcontrollers and converts it to speech. This allows the TI MSP53C691 to be used with a master microprocessor/microcontroller in various speech-related products such as security systems, learning aids, games, and toys. High quality, low bit-rate coders, easy interface with the master microcontroller, digital gain control, low power sleep mode, and low voltage operation makes this device ideal for products requiring long duration speech, less development cycle times, and peripheral device control through the slave device.

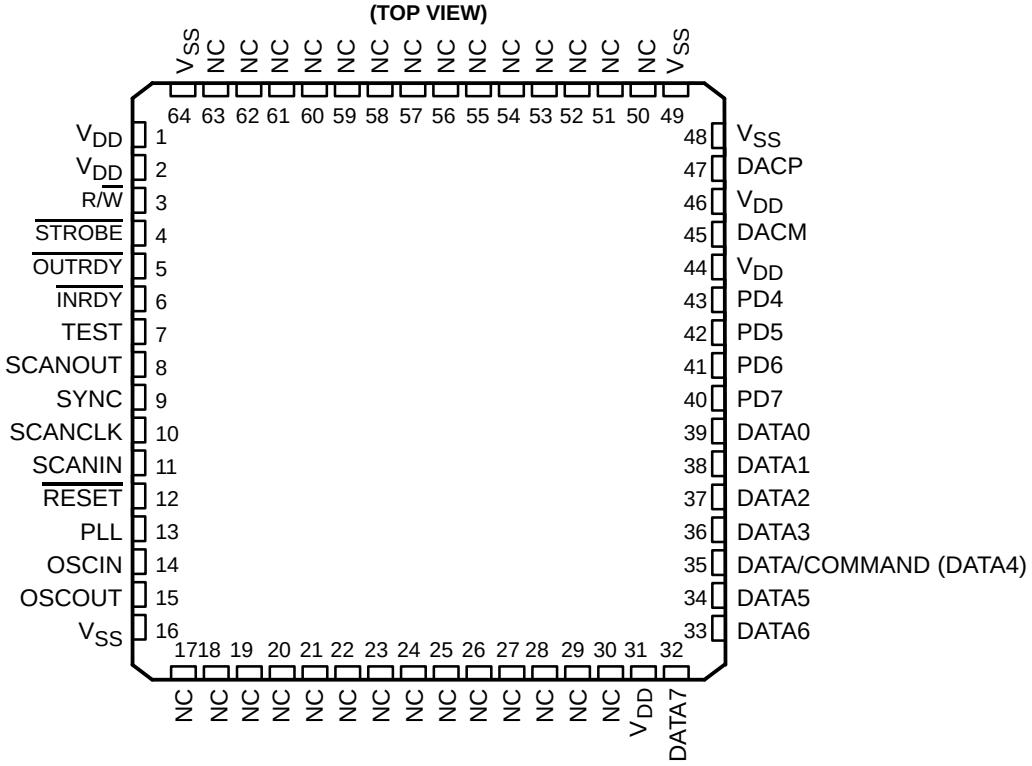
This device supports several speech synthesis algorithms that permit tradeoffs to meet the price performance requirements of various markets. The MSP53C691 implements a unique feature of playing a single channel FM music along with CELP or MELP speech data concurrently. This feature allows the user to speak a certain phrase in MELP or CELP with single channel music in the background.

The MSP53C691 is optimized to support a 4-bit wide data transfer protocol. The device has two status bits and three control bits that control the communication protocol between the master and the slave. The MSP53C691 also has 1 bit (command/data) which differentiates between a command or speech data feeding into the slave. In 4-bit mode, various commands are sent to the slave during speech to perform various tasks.

The MSP53C691 also supports the 8-bit wide data transfer but the support for commands is disabled during speaking-a-phrase. When speaking-a-phrase in 8-bit mode is complete, the MSP53C691 switches back to the 4-bit mode to receive the next command. Switching between 4-bit mode or 8 bit mode is permitted between speech data files.

pin assignments

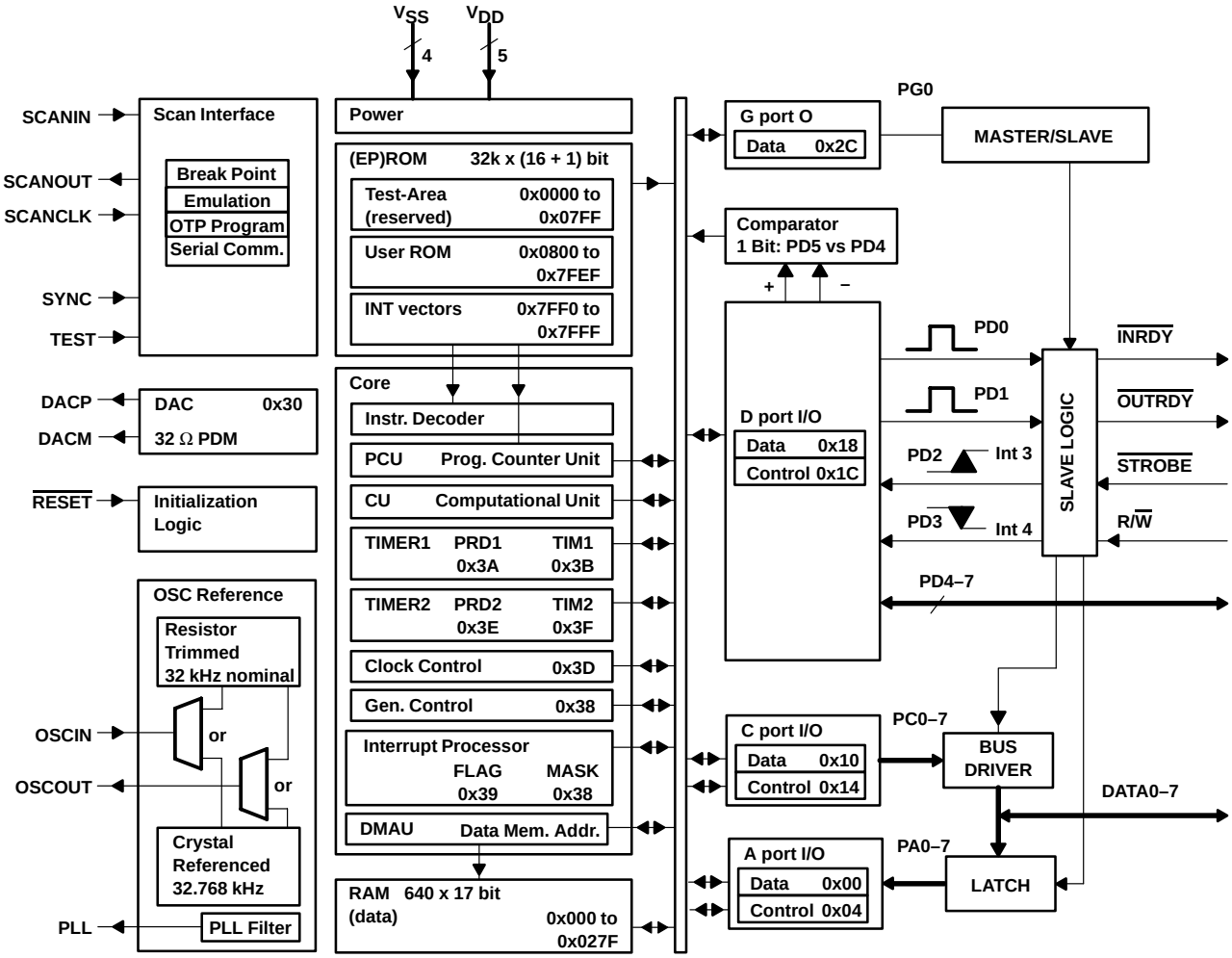
MSP53C691
PM PACKAGE
(TOP VIEW)



NC – No internal connection

NOTE: Pin 35 is DATA4 in 8-bit mode, or DATA/COMMAND in 4-bit mode.

functional block diagram



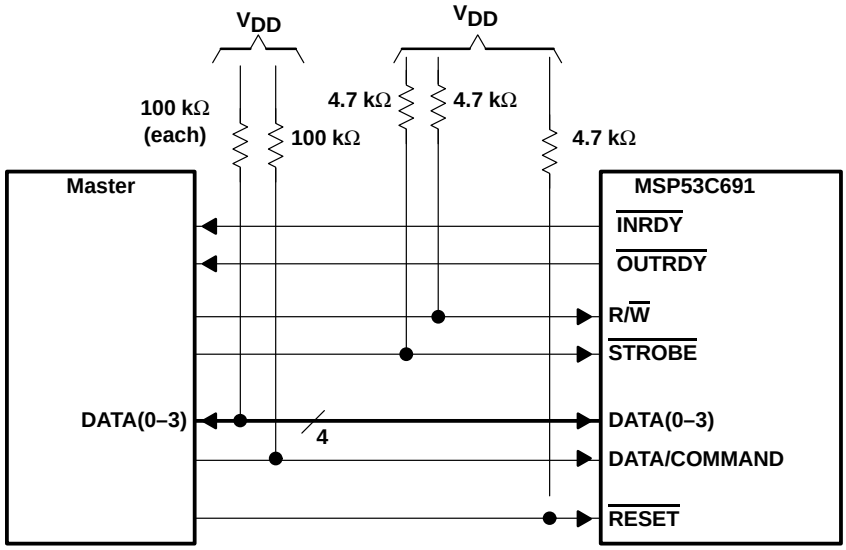
Terminal Functions

NAME	PIN NO.	PAD NO.	I/O	DESCRIPTION
DATA0–DATA3	39–36	25–22	I/O	Data bits 0 through 3 (in 4-bit or 8-bit mode)
DATA4 or DATA/COMMAND	35	21	I/O	Data bit 4 (in 8-bit mode) Data/command control bit (in 4-bit mode). Low signal indicates command and high signal indicates data.
DATA5–DATA7	34–32	20–18	I/O	Data bits 5 through 7 (8-bit mode only) Not used (4-bit mode only)
$\overline{\text{INRDY}}$	6	6	O	An output signal from the slave to the microcontroller. A low signal indicates that the MSP53C691 is ready to accept data or command. A high signal indicates that the MSP53C691 is busy and the microcontroller must not write any data or command to it.
$\overline{\text{OUTRDY}}$	5	5	O	An output signal from the slave to the microcontroller. A low signal indicates that the MSP53C691 is ready to send data or command to the microcontroller.
PD4–PD7	43–40	29–26	I/O	General-purpose I/O bus
R/$\overline{\text{W}}$	3	3	I	An input signal to the slave from the microcontroller. Read/write select signal which is set high for read operations or set low for write operations by the microcontroller.
$\overline{\text{STROBE}}$	4	4	I	An input signal to the slave from the microcontroller. STROBE sequences read or write operations in conjunction with the R/W signal. This signal is pulsed high-low-high for read or write operations sequencing.
Reference Oscillator Signals				
OSCOUT	15	15	O	Output of resistor/crystal oscillator
OSCIN	14	14	I	Input to resistor/crystal oscillator
PLL	13	13	O	Output of phase-lock-loop filter
Scan Port Control Signals				
SCANIN†	11	39	I	Scan port data input
SCANOUT†	8	35	O	Scan port data output
SCANCLK†	10	38	I	Scan port clock
SYNC†	9	37	I	Scan port synchronization
TEST†	7	36	I	C604: test modes
Digital-to-Analog Sound Output				
DACP	47	33	O	Digital-to-analog plus output (+)
DACM	45	31	O	Digital-to-analog minus output(–)
Initialization				
$\overline{\text{RESET}}$	12	12	I	Device initialization
Power Signals‡				
V_{DD}	1, 2, 31, 44, 46‡	1, 2, 17, 30, 32‡	—	Processor power, 5 V nominal supply voltage
V_{SS}	16, 48, 49‡, 64	16, 34‡, 35, 36	—	Ground pin

† All pins must be N.C.

‡ Marked pins are V_{DD} and V_{SS} connections which service the DAC circuitry. These pins tend to sustain a higher current draw. A dedicated decoupling capacitor across these pins is therefore required.

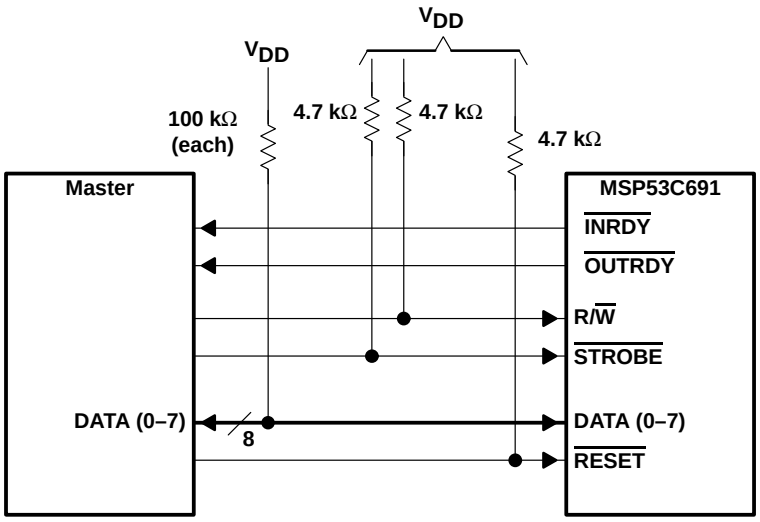
	MSP53C691 (4-bit mode)	MSP53C691 (8-bit mode)
Number of data lines	4	8
Number of control lines	3 (strobe, R/$\overline{W}$, data/command)	2 (strobe, R/$\overline{W}$)
Number of status lines	2 ($\overline{INRDY}$, $\overline{OUTRDY}$)	2 ($\overline{INRDY}$, $\overline{OUTRDY}$)
Number of general-purpose I/O lines	4	4
Support for commands (while speaking)	Yes	No



NOTE:

$\overline{STROBE}$	Active low strobe signal from microcontroller
R/$\overline{W}$	Read/write signal from microcontroller
$\overline{RESET}$	Active low reset signal from microcontroller
DATA0–DATA3	Data bits 0 through 3
PD4–PD7	General-purpose I/O bus
DACP	Output to speaker/amplifier
DACM	Output to speaker/amplifier
DATA/COMMAND	This bit determines if the data sent by the microcontroller is data or command.

Figure 1. MSP53C691 Interfacing Diagram—4-Bit Mode



NOTE:	$\overline{\text{STROBE}}$:	Active low strobe signal from microcontroller
	R/$\overline{\text{W}}$:	Read/write signal from microcontroller
	$\overline{\text{RESET}}$	Active low reset signal from microcontroller.
	$\overline{\text{INRDY}}$:	Active low indicates that the MSP53C691 is ready to accept data.
	$\overline{\text{OUTRDY}}$:	Active low indicates that the MSP53C691 is ready to send data.
	DATA0–DATA7	Data bits 0 through 7
	PD4–PD7	General-purpose I/O bus
	DACP	Output to speaker/amplifier
	DACM	Output to speaker/amplifier

Figure 2. MSP53C691 Interfacing Diagram—8-Bit Mode

read operation by the master

The process for the read operation by the master is the same in either 4-bit or 8-bit mode. The read operation by the master happens when the slave wants to send something to the master. The read process is initiated by the slave by pulling $\overline{\text{OUTRDY}}$ low when it is ready.

The following events take place during the read operation:

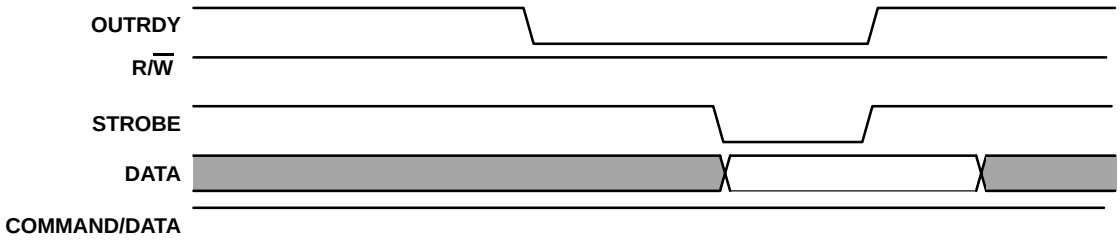
- The MSP53C691 puts the data to be sent to the master on the internal bus.
- The MSP53C691 sets $\overline{\text{OUTRDY}}$ low to indicate that it is ready to send data to the microcontroller.
- The microcontroller sets R/$\overline{\text{W}}$ high to indicate a read operation.
- The microcontroller sets $\overline{\text{STROBE}}$ low. The data is available on the external data-bus at this point.
- The microcontroller reads the data from the bus.
- The microcontroller sets $\overline{\text{STROBE}}$ high. The MSP53C691 also pulls $\overline{\text{OUTRDY}}$ high at the rising edge of $\overline{\text{STROBE}}$.
- The data is taken from the external data-bus after $\overline{\text{STROBE}}$ goes high.

The microcontroller should latch or read in the data while $\overline{\text{STROBE}}$ is low. When the microcontroller sets $\overline{\text{STROBE}}$ high, the MSP53C691 sets $\overline{\text{OUTRDY}}$ high to indicate that the data has been successfully transferred.

Figure 3 shows the sequence of events of the read operation.

read operation by the master (continued)

a) Sequence of events for a single read operation:



b) Read—Two speech data transfer sequences:

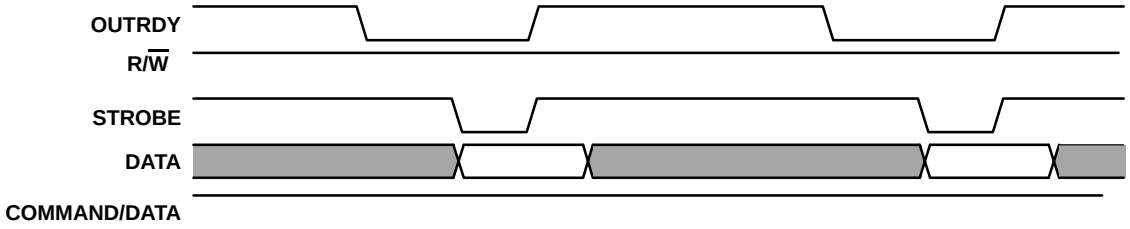


Figure 3. Data Transfer – Read

write operation by the master

The process for the write operation by the master is the same in either 4-bit or 8-bit mode. The write operation by the master happens when the slave is ready to request data or command from the master. The write process is initiated by the slave by pulling $\overline{\text{INRDY}}$ low when the slave is ready to receive data.

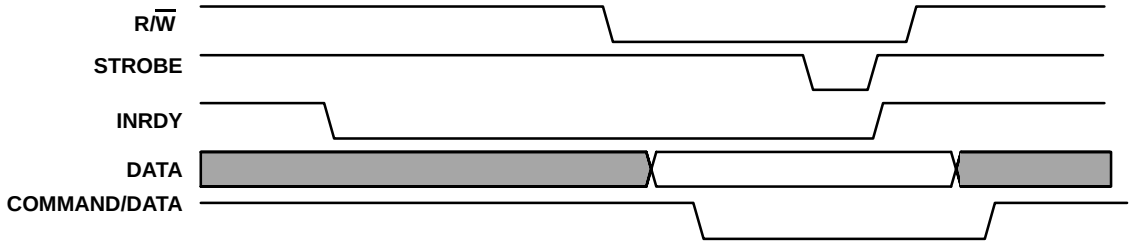
The following events take place during the write operation:

- The MSP53C691 sets $\overline{\text{INRDY}}$ low to indicate that it is ready to receive data from the microcontroller.
- The microcontroller sets R/$\overline{\text{W}}$ low to indicate a write operation.
- The microcontroller puts the data in the external data-bus.
- The microcontroller sets $\overline{\text{STROBE}}$ low after the data is valid.
- The microcontroller sets $\overline{\text{STROBE}}$ high after a minimum of 300 ns. The MSP53C691 also pulls $\overline{\text{INRDY}}$ high at the rising edge of $\overline{\text{STROBE}}$.
- The data is latched in the MSP53C691 at the rising edge of $\overline{\text{STROBE}}$.

write operation by the master (continued)

When the microcontroller sets $\overline{\text{STROBE}}$ high, the MSP53C691 sets $\overline{\text{INRDY}}$ high to indicate that the MSP53C691 is not ready to receive any more data.

a) Sequence of events for a single write operation



b) Write—Two speech data transfer sequences

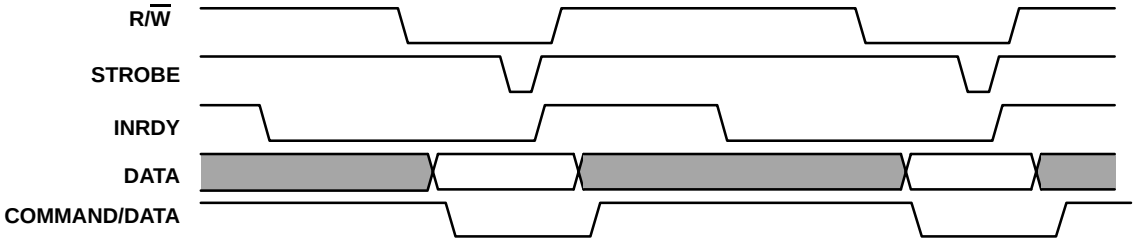


Figure 4. Data Transfer – Write

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Supply current, I_{DD} (see Note 2) . . . . . 35 mA
Input voltage range, V_I (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1) . . . . . –0.3 V to V_{DD} + 0.3 V
Storage temperature range, T_A . . . . . –30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltages are measured with respect to V_{SS} .
2. The total supply current includes the current out of all the I/O pins as well as the operating current of the device.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD} (with respect to V_{SS})		3	5.2	V
CPU clock rate, $f_{(CPU)}$ (as programmed)		64	12,320	kHz
Load resistance between DACP and DACM, $R_{(DAC)}$		32		Ω
Operating free-air temperature, T_A	Device functionality	0	70	°C

timing requirements

		MIN	MAX	UNIT
$t_{(RESET)}$	Reset pulsed low, while ’C691 has power applied	100		ns
t_{w1}	Pulse width required prior to a negative transition at pin (PD3 or PD5 interrupt)	2		$1/F_{CPU}$
t_{w2}	Pulse width required prior to a positive transition at pin (PD2 or PD4 interrupt)	2		$1/F_{CPU}$

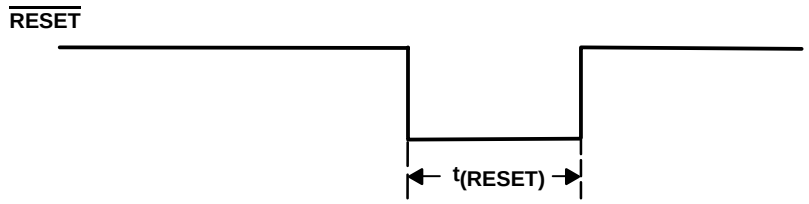


Figure 5. Initialization Timing Diagram

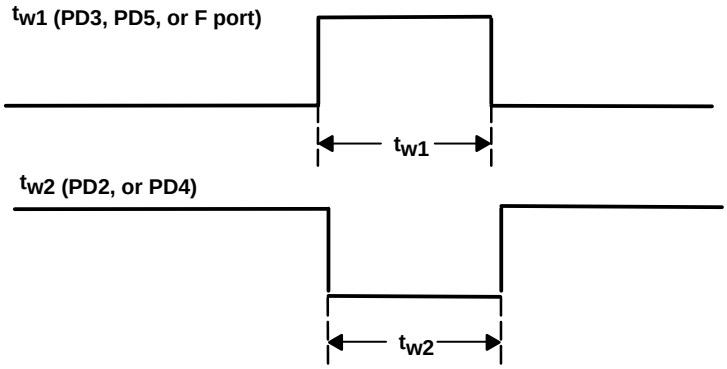


Figure 6. MSP53C691 External Interrupt Pin Pulse Width Requirements t_{w1} and t_{w2}

dc electrical characteristics over recommended operating free-air temperature range, T_A = 0°C – 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$\overline{\text{RESET}}$	Threshold changes	V_{DD} = 3 V	Positive going threshold		2.4		V
			Negative going threshold		1.8		
			Hysteresis		0.6		
		V_{DD} = 5.2 V	Positive going threshold		3.3		V
			Negative going threshold		2.9		
			Hysteresis		0.4		
V_{IH}	High-level input voltage	V_{DD} = 3 V		2		3	V
		V_{DD} = 4.5 V		3		4.5	
		V_{DD} = 5.2 V		3.5		5.2	
V_{IL}	Low-level input voltage	V_{DD} = 3 V		0		1	V
		V_{DD} = 4.5 V		0		1.5	
		V_{DD} = 5.2 V		0		1.7	
I_{OH}§	High-level output current per pin of I/O port	V_{DD} = 4.5 V	V_{OH} = 4 V			–2	mA
I_{OL}§	Low-level output current per pin of I/O port		V_{OL} = 0.5 V			5	mA
I_{OH} (DAC)	High-level output DAC current		V_{OH} = 4 V			–10	mA
I_{OL} (DAC)	Low-level output DAC current		V_{OL} = 0.5 V			20	mA
I_{lkg}	Input leakage current	Excludes OSC_{IN}				1	µA
$I_{(STANDBY)}$	Standby current	RESET is low			0.05	10	µA
I_{DD}	Operating current	V_{DD} = 4.5 V,	F_{CLOCK} = 12.32 MHz		15		mA
$I_{(SLEEP-deep)}$	Supply current	V_{DD} = 4.5 V,	DAC off, ARM set, OSC disabled		0.05	10	µA
$I_{(SLEEP-mid)}$		V_{DD} = 4.5 V,	DAC off, ARM set, OSC enabled		40	60	
$I_{(SLEEP-light)}$		V_{DD} = 4.5 V,	DAC off, ARM clear, OSC enabled		60	100	
V_{IO}	Input offset voltage	V_{DD} = 4.5 V,	Vref = 1 to 4.25 V		25	50	mV
$R_{(PULLUP)}$	F port pullup resistance	V_{DD} = 5 V		70	150		kΩ
$\Delta f_{(RTO-trim)}$	Trim deviation	$R_{(RTO)}$ = 470 kΩ, V_{DD} = 4.5 V, T_A = 25°C, $f_{(RTO)}$ = 8.192 MHz (PLL setting = 7 Ch)‡			±1%	±3%	
$\Delta f_{(RTO-volt)}$	Voltage deviation	R_{RTO} = 470 kΩ, V_{DD} = 3.5 to 5.2 V, T_A = 25°C, $f_{(RTO)}$ = 8.192 MHz (PLL setting = 7 Ch)‡				±1.5	%/V
$\Delta f_{(RTO-temp)}$	Temperature deviation	$R_{(RTO)}$ = 470 kΩ, V_{DD} = 4.5 V, T_A = 0 to 70°C, $f_{(RTO)}$ = 8.192 MHz (PLL setting = 7 Ch)‡			±0.03		%/°C
$\Delta f_{(RTO-res)}$	Resistance deviation	V_{DD} = 4.5 V,	T_A = 25°C, R_{OSC} = 470 kΩ at ±1%, $f_{(RTO)}$ = 8.192 MHz (PLL setting = 7 Ch)‡		±1		%/R

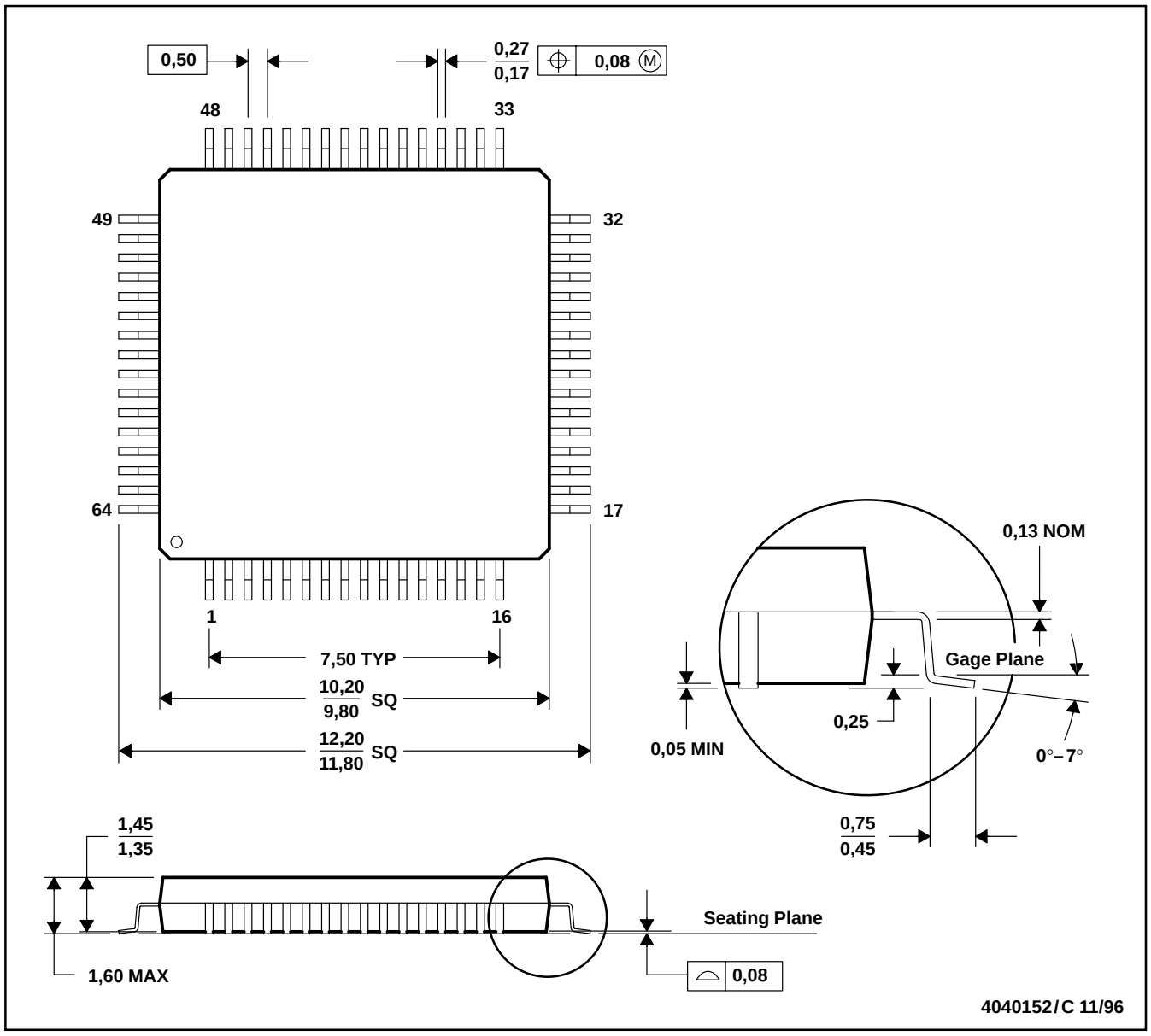
† Typical voltage and current measurements taken at 25°C,
‡ The best trim value is selected at nominal temperature and voltage but the deviation due to the trim error is ignored.
§ This parameter cannot exceed 15 mA total per internal V_{DD} pin. Port C and port D share 1 internal V_{DD}. Ports A and G0 are used internally.

external component absolute values

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$R_{(RTO)}$	RTO external resistance	T_A = 25°C,	1% tolerance		470	kΩ
$C_{(PLL)}$	PLL external capacitance	T_A = 25°C,	10% tolerance		3300	pF

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PACKAGING INFORMATION

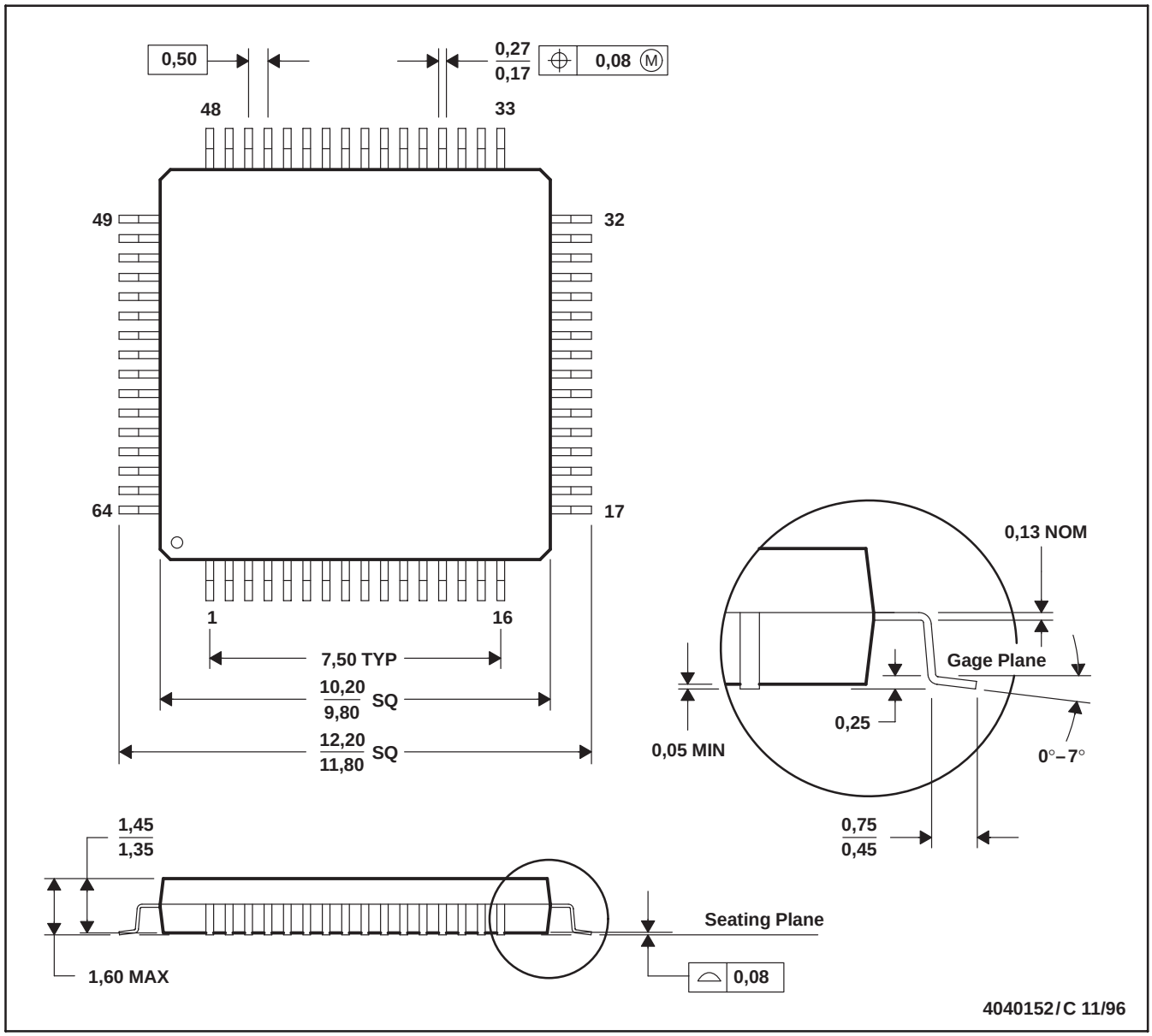
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP53C691PM	OBSOLETE	LQFP	PM	64		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



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