REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14									

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE: 6 SEPTEMBER 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, FAST CMOS, 8-BIT NONINVERTING BUS INTERFACE LATCH, TTL COMPATIBLE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88675

SHEET 1 OF 14

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E964

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88675	01	K	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT845A	8-bit noninverting bus interface latch, TTL compatible
02	54FCT845B	8-bit noninverting bus interface latch, TTL compatible

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
Input voltage range	-0.5 V dc to V_{CC} +0.5 V dc
Output voltage range	-0.5 V dc to V_{CC} +0.5 V dc
DC input diode current (I_{IK})	±20 mA
DC output diode current (I_{OK})	±50 mA
DC output current	±100 mA
Maximum power dissipation (P_D) 2/	500 mW
Thermal resistance, junction-to-case (θ_{JC}):	
Cases K, L, and 3	See MIL-M-38510, appendix C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1/ All voltages referenced to GND.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum logic low voltage (V_{IL})	0.8 V dc
Minimum logic high voltage (V_{IH})	2.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum setup time, data to LE (t_s):	
Device type 01	2.5 ns
Device type 02	2.5 ns
Minimum hold time, data to LE (t_h):	
Device type 01	3.0 ns
Device type 02	2.5 ns
Maximum preset recovery time, low to high (t_{rem}):	
Device type 01	17.0 ns
Device type 02	13.0 ns
Maximum clear recovery time, low to high (t_{rem}):	
Device type 01	17.0 ns
Device type 02	10.0 ns
Minimum LE pulse width, high (t_w):	
Device type 01	6.0 ns
Device type 02	4.0 ns
Minimum preset pulse width, low (t_w):	
Device type 01	9.0 ns
Device type 02	4.0 ns
Minimum clear pulse width, low (t_w):	
Device type 01	9.0 ns
Device type 02	4.0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Truth table. The truth table shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuits. The switching waveforms and test circuits shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ± 10 % unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 0.8 V or 2.0 V	I_{OH} = -300 µA	All	1,2,3	4.3		V
			I_{OH} = -12 mA	All	1,2,3	2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IN} = 0.8 V or 2.0 V	I_{OL} = 300 µA	All	1,2,3		0.2	
			I_{OL} = 32 mA	All	1,2,3		0.5	
Clamp diode voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1		-1.2	
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1,2,3		5	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		All	1,2,3		-5	
Short circuit current	I_{OS}	V_{CC} = 5.5 V 1/		All	1,2,3	-60		mA
Offstate output current	I_{OZ}	V_{CC} = 5.5 V, V_O = 5.5 V or GND		All	1,2,3		±10	µA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V V_{CC} = 5.5 V, $f_{CP} = f_I$ = 0 MHz		All	1,2,3		1.5	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ± 10 % unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Quiescent power supply current (TTL inputs)	I_{CCT}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/	All	1,2,3		2.0	mA
Dynamic supply current	I_{CCD}	V_{CC} = 5.5 V, Outputs open, $\overline{OE}$ = GND One bit toggling, 50 percent duty cycle, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	All	3/		250	µA/MHz
Total power supply current 4/	I_{CC}	V_{CC} = 5.5 V, Outputs open, One bit toggling f_I = 10 MHz, $\overline{OE}$ = Gnd, 50 percent duty cycle, LE = 5.5 V $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	All	1,2,3		4.0	mA
		V_{IN} = 3.4 V or V_{IN} = GND	All	1,2,3		5.0	
Functional tests		See 4.3.1d	All	7,8			
Input capacitance	C_{IN}	See 4.3.1c	All	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c	All	4		12	
Propagation delay time D_i to Y_i (LE = high)	t_{PLH}, t_{PHL}	C_L = 50 pF ±10%, R_L = 500Ω ±5%	01	9,10,11		11.0	ns
			02			7.5	
Propagation delay time LE to Y_i	t_{PLH}, t_{PHL}	See figure 4.	01	9,10,11		16.0	
			02			10.5	
Propagation delay time $\overline{PRE}$ to Y_i	t_{PLH}		01	9,10,11		14.0	
			02			10.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ± 10 % unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time $\overline{CLR}$ to Y_i	t_{PHL}	C_L = 50 pF ±10% r_L = 500Ω ±5% See figure 4	01	9,10,11		15.0	ns
			02			11.0	
Output enable time $\overline{OE}$ (high to low) to Y_i	t_{PZH}, t_{PZL}		01	9,10,11		15.0	
			02			8.5	
Output disable time $\overline{OE}$ (low to high) to Y_i	t_{PHZ}, t_{PLZ}		01	9,10,11		12.0	
			02			7.5	

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ In accordance with TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power calculations.

4/ $I_{CC} = I_{CCQ} + (I_{CCT} \times D_H \times N_T) + (I_{CCD} \times (f_{CP}/2 + (f_I \times N_I)))$
where D_H = 50% duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
f_I = Input frequency in MHz
f_{CP} = Clock frequency
N_I = Number of inputs at f_I

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only initially and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 tests shall verify the truth table on figure 3.

Device types	01 and 02	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	$\overline{OE1}$	NC
2	$\overline{OE2}$	$\overline{OE1}$
3	D_0	$\overline{OE2}$
4	D_1	D_0
5	D_2	D_1
6	D_3	D_2
7	D_4	D_3
8	D_5	NC
9	D_6	D_4
10	D_7	D_5
11	$\overline{CLR}$	D_6
12	GND	D_7
13	LE	$\overline{CLR}$
14	$\overline{PRE}$	GND
15	Y_7	NC
16	Y_6	LE
17	Y_5	$\overline{PRE}$
18	Y_4	Y_7
19	Y_3	Y_6
20	Y_2	Y_5
21	Y_1	Y_4
22	Y_0	NC
23	$\overline{OE3}$	Y_3
24	V_{CC}	Y_2
25	---	Y_1
26	---	Y_0
27	---	$\overline{OE3}$
28	---	V_{CC}

NC = No connect

FIGURE 1. Terminal connections.

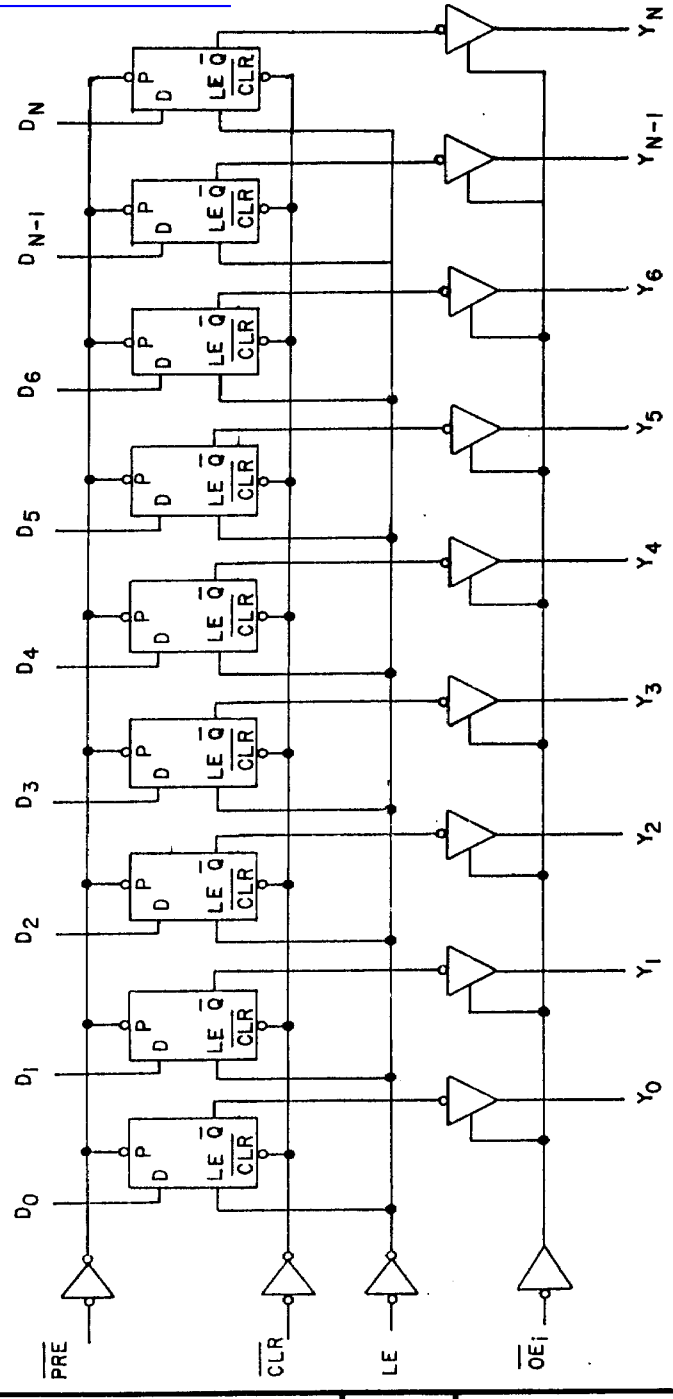


FIGURE 2. Logic diagram.

$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (high Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (high Z)
H	L	H	L	X	H	Z	Latched (high Z)

H = High
L = Low
NC = No change

X = Don't care
Z = High impedance

FIGURE 3. Truth table.

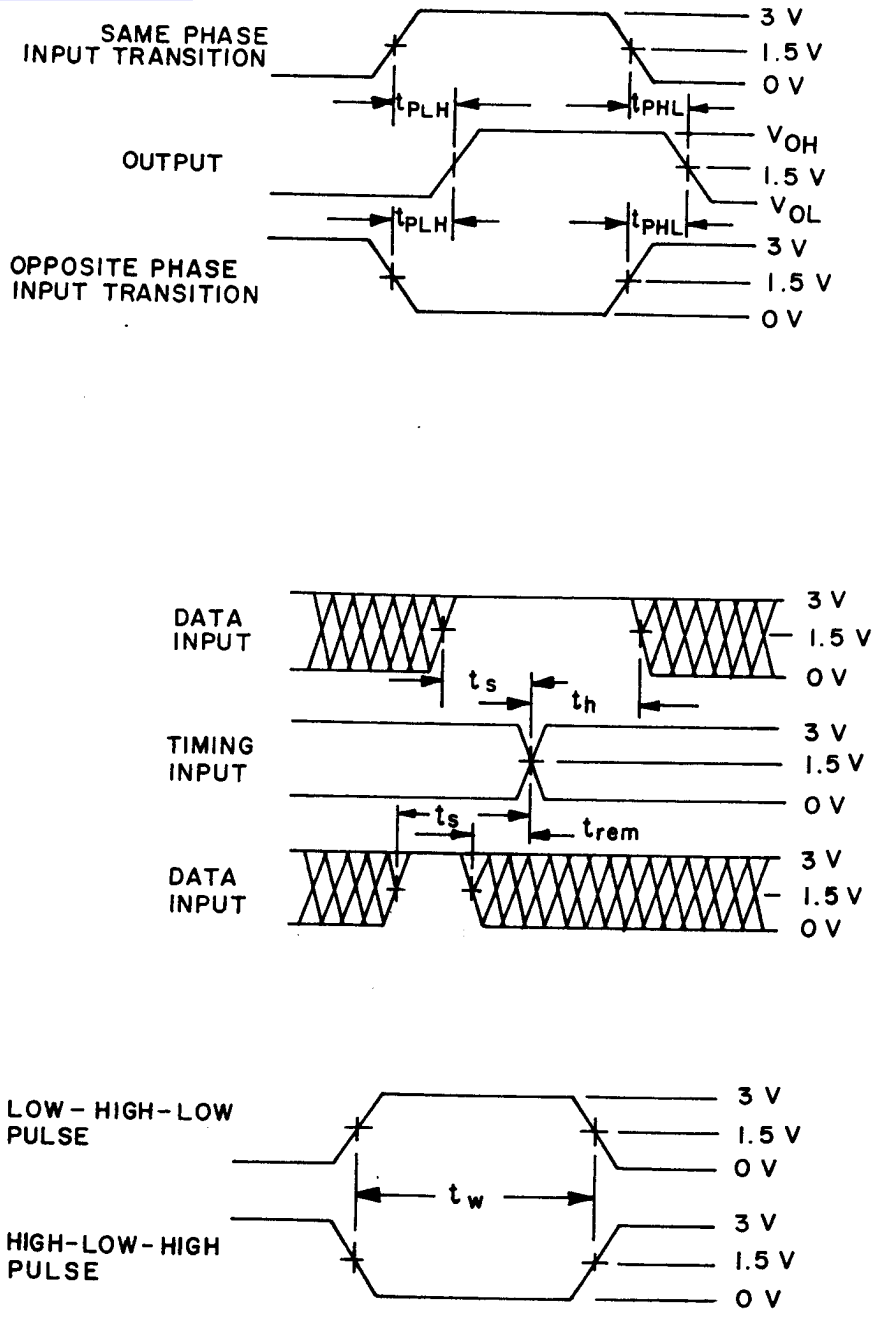
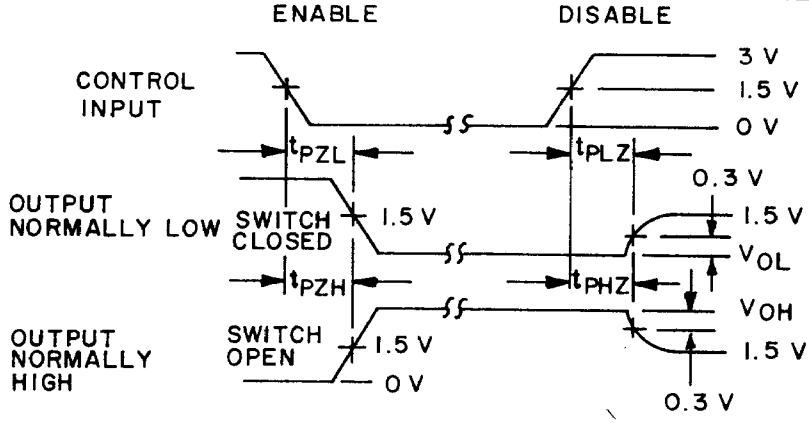
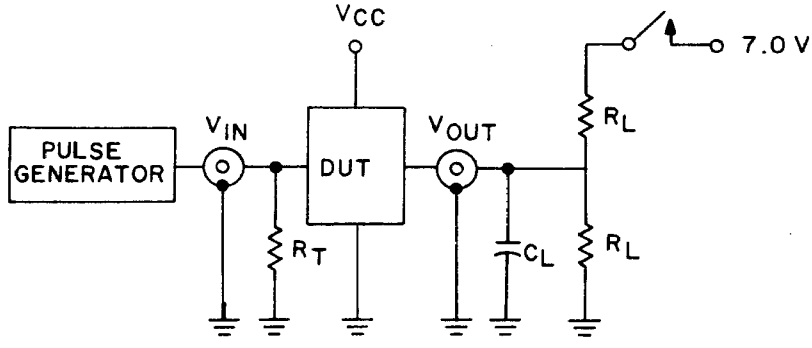


FIGURE 4. Switching waveforms and test circuits.



NOTES:
1. Diagram shown for input control enable-low and input control disable-high.
2. Input: $t_r = t_f = 2.5$ ns (10% to 90%) unless otherwise specified.



SWITCH POSITION

Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
All other	Open

Definitions:
R_L = Load resistor.
C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of pulse generators.

FIGURE 4. Switching waveforms and test circuits - Continued.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test (method 5004)	1*,2,3,7, 8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8867501KX	61772	IDT54FCT845AEB
5962-8867501LX	61772	IDT54FCT845ADB
5962-88675013X	61772	IDT54FCT845ALB
5962-8867502KX	61772	IDT54FCT845BEB
5962-8867502LX	61772	IDT54FCT845BDB
5962-88675023X	61772	IDT54FCT845BLB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 3236 Scott Boulevard Santa Clara, CA 95054

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