REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	~~Updated boilerplate to include class~~ N. Added case outline X. Editorial changes throughout. – tmh	98-01-27	Monica L. Poelking
B	Changes made in accordance with nor 5962-R043-99.	99-03-04	Monica L. Poelking
C	Added Junction Temperature to paragraph 1.3. Made technical change to supply current in table I. – LTG	00-01-28	Monica L. Poelking

REV	A	A	A	A	A	A	A													
SHEET	35	36	37	38	39	40	41													
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																
REV	C	A	C	C	A	C	A	A	A	A	A	A	A	A		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
97-08-04

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

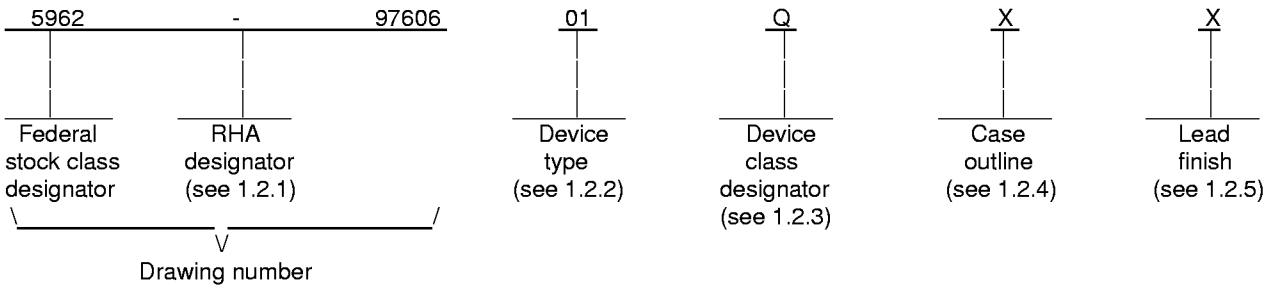
SIZE	CAGE CODE	
A	67268	5962-97606

SHEET 1 OF 41

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320LC31	Digital signal processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	132	Plastic quad flatpack

1/ Items which have been subjected to a passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCVI inspections, and are encapsulated in plastic.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to +7.0 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to +7.0 V dc
Continuous power dissipation (P_D) 3/	3.15 W
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J):	
Die code 9	+125°C
Case outline X	+150°C
Thermal resistance, junction to case (1_{JC}):	
Case X	9.8°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+3.13 V dc to +3.47 V dc
Supply voltage range (CVSS, etc.)(V_{SS})	0 V dc nominal
High-level input voltage range (V_{IH}) (except $\overline{RESET}$) 4/	+1.8 V dc to V_{DD} + 0.3 V dc
for $\overline{RESET}$	+2.2 V dc to V_{DD} + 0.3 V dc
Low-level input voltage range (V_{IL}) 4/	-0.3 V dc to 0.6 V dc
Maximum high-level output current (I_{OH})	-300 µA
Maximum low-level output current (I_{OL})	+2 mA
CLKIN high level input voltage (V_{TH}) 4/	+2.5 V dc to V_{DD} to +0.3 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Actual operating power is less. This value was obtained under specially produced worst-case test conditions which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible.
4/ Maximum V_{IH} , minimum V_{IL} and maximum V_{TH} are characterized but not tested.
5/ Values will be added when they become available.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2 herein.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3 herein.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4 herein.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 95 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified	V_{DD}	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage 3006	V_{OH}	I_{OH} = -300 µA	3.13 V	1, 2, 3	2.0		V
Low level output voltage 3007 2/	V_{OL}	I_{OL} = 2 Ma	3.13 V	1, 2, 3		0.4	
Three-state current 3021	I_Z		3.13 V	1, 2, 3	-20	20	µA
Input current 3010	I_I	For input under test $V_{IN} = V_{SS}$ to V_{DD}	3.13 V to 3.47 V	1, 2, 3	-10	+10	
Input current with internal pull-ups 3010 3/	I_{IP}		3.13 V to 3.47 V	1, 2, 3	-600	+10	
Input current, (X2/CLKIN) 3010	I_{IC}	V_I = 0.0 V to V_{DD} max	3.13 V to 3.47 V	1, 2, 3	-50	+50	
Supply current 4/ 3005	I_{CC}	$T_A = 25°C$, f_x = 40 MHz	3.47 V	1, 2, 3		400	mA
Input capacitance 3012	C_{IN}	$T_C = +25°C$, See 4.4.1b	3.3 V	4		15	pF
Output capacitance 3012	C_{OUT}		3.3 V	4		20	
X2/CLKIN capacitance 3012	C_X		3.3 V	4		25	
Functional testing 3014		See 4.4.1d		7, 8	L	H	
Fall time, CLKIN 5/	t_{f1}	See figure 4		9,10,11		5	ns
Pulse duration, CLKIN low	t_{w1}	t_{C1} = 25 ns			9		
Pulse duration, CLKIN high	t_{w2}	t_{C1} = 25 ns			9		
Rise time, CLKIN 5/	t_{r1}					5	
Cycle time, CLKIN	t_{c1}				25	303	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Fall time, H1/H3	t_{f2}	See figure 4	9,10,11		3	ns
Pulse duration, H1/H3 low	t_{w3}	P = t_{C1}		P-5		
Pulse duration, H1/H3 high	t_{w4}	P = t_{C1}		P-6		
Rise time, H1/H3	t_{r2}				3	
Delay time, from H1(H3) low to H3(H1) high 6/	t_{d1}			0	4	
Cycle time, H1/H3	t_{c2}			50	606	
Delay time, from H1 low to $\overline{\text{STRB}}$ low 6/	t_{d2}	Memory $\overline{\text{STRB}}$ = 0 See figure 4		0	6	
Delay time, from H1 low to $\overline{\text{STRB}}$ high 6/	t_{d3}			0	6	
Delay time, from H1 high to R/$\overline{\text{W}}$ low 6/	t_{d4}			0	9	
Delay time, from H1 low to A valid 6/	t_{d6}			0	11	
Setup time, D valid before H1 low (read)	t_{su1}			14		
Hold time, D after H1 low (read) 6/	t_{h1}			0		
Setup time, $\overline{\text{RDY}}$ before H1 high	t_{su3}			8		
Hold time, $\overline{\text{RDY}}$ after H1 high	t_{h2}			0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions -55°C ≤ T_C ≤ +125°C 1/ +3.13 V ≤ V_{DD} ≤ +3.47 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Delay time, H1 high to R/W high (write)	t_{d8}	See figure 4 Memory ($\overline{STRB}$ = 0)	9,10,11		9	ns
Valid time, D after H1 low (write)	t_{v1}				17	
Hold time, D after H1 high (write) 3/	t_{h3}			0		
Delay time, form H1 high to A valid on back-to-back write cycles	t_{d9}				15	
Delay time, from $\overline{RDY}$ to A valid 5/	t_{d11}				7	
Delay time, H3 high to XF0 low	t_{d17}	Timing for XF0 and XF1 ;when executing LDFI or LDII See figure 4			13	
Set-up time, XF1 valid after H1 low	t_{su7}			10		
Hold time,XF1 after H1 low	t_{h7}			0		
Delay time, from H3 high to XF0 high	t_{d18}	Timing for XF0 when executing a STFI or STII See figure 4			13	
Delay time, from H3 high to XF0 low	t_{d19}	Timing for XF0 and XF1 when executing a SIGI See figure 4			13	
Delay time, from H3 high to XF0 high	t_{d20}				13	
Set-up time, XF1 valid before H1 low	t_{su8}			10		
Hold time, XF1 after H1 low	t_{h8}			0		
Valid time, H3 high to XF	t_{v3}	Timing for loading XF register when conformed as an output pin See figure 4			13	
Hold time, XF after H3 high 5/	t_{h9}	Change of XF from output to input mode See figure 4			13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time, XF before H1 low	t_{su9}	Change of XF from output to input mode See figure 4	9,10,11	10		ns
Hold time, XF after H1 low	t_{h10}			0		
Delay time, from H3 high to XF switching from input to output	t_{d21}	Change of XF from input to output mode See figure 4			17	
Setup time, for $\overline{\text{RESET}}$ before CLKIN low 5/	t_{su10}	$\overline{\text{RESET}}$ timing See figure 4		10	P	
Delay time, from CLKIN high to H1 high	t_{d22}			2	14	
Delay time, from CLKIN high to H1 low	t_{d23}			2	14	
Setup time, $\overline{\text{RESET}}$ high before H1 low and after 10 H1 clock cycles 6/	t_{su11}			9		
Delay time, from CLKIN high to H3 low	t_{d24}			2	14	
Delay time, from CLKIN high to H3 high	t_{d25}			2	14	
Disable time, from H1 high to D high - Z 5/	t_{dis1}				13	
Disable time, from H3 high to A high - Z 5/	t_{dis2}				9	
Delay time, from H3 high to control signals high 5/	t_{d26}				9	
Delay time, from H1 high to $\overline{\text{R/W}}$ high 5/	t_{d27}				9	
Delay time, from H1 high to $\overline{\text{IACK}}$ high 5/	t_{d28}				9	
Disable time, from $\overline{\text{RESET}}$ low to asynchronously reset signals (high - Z) 5/	t_{dis3}				21	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Setup time, $\overline{INT}$ (3-0) before H1 low	t_{su12}	$\overline{INT}$(3-0) response timing See figure 4		9,10,11	15		ns
Pulse duration, to guarantee one interrupt seen 5/ 6/ 8/	t_{w5}				P	2P 6/	
Delay time, from H1 high to $\overline{IACK}$ low	t_{d29}	$\overline{IACK}$ timing See figure 4				9	
Delay time, from H1 high to $\overline{IACK}$ high during first cycle of $\overline{IACK}$ instruction data read	t_{d30}					9	
Delay time, from H1 high to internal CLKX/R	t_{d31}	Data rate mode See figure 4				19	
Cycle time, CLKX/R	t_{c3}		CLKX/R ext 6/		t_{c2} x 2.6		
			CLKX/R int 5/		t_{c2} x 2	t_{c2} x 2^{32}	
Pulse width, CLKX/R	t_{w6}		CLKX/R ext 6/			t_{c2}+ 10	
			CLKX/R int		$(t_{c3}/2)-5$	$(t_{c3}/2)+5$	
Rise time, CLKX/R 5/	t_{r3}					7	
Fall time, CLKX/R 5/	t_{f3}	Fixed data rate mode See figure 4				7	
Delay time, from CLKX to DX valid	t_{d32}		CLKX ext			30	
			CLKX int			17	
Setup time, DR before CLKR low	t_{su13}		CLKR ext		9		
			CLKR int		21		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Hold time, DR from CLKR low	t_{h11}	Fixed data rate mode See figure 4	CLKR ext	9,10,11	9		ns
			CLKR int 6/		0		
Delay time, from CLKX to internal FSX high/low	t_{d33}		CLKX ext			27	
			CLKX int			15	
Setup time, FSR before CLKR low	t_{su14}		CLKR ext		9		
			CLKR int		9		
Hold time, FSX/R from CLKX/R low	t_{h12}		CLKX/R ext		9		
			CLKX/R int 6/		0		
Setup time, external FSX before CLKX	t_{su15}		CLKX ext 5/		$-(t_{c2}- 8)$	$(t_{c3}/2- 10)$	
			CLKX int 5/		$-(t_{c2}-21)$	$t_{c3}/2$	
Delay time, from CLKX to first DX bit, FSX precedes CLKX high	t_{d34}	Variable rate data mode	CLKX ext			18	
			CLKX int			17	
Delay time, from FSX to first DX bit, CLKX precedes FSX	t_{d35}	See figure 4				30	
Delay time, from CLKX high to DX high-Z following last data bit 5/	t_{d36}					17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions $-55°C \le T_C \le +125°C$ 1/ $+3.13\ V \le V_{DD} \le +3.47\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Setup time, $\overline{HOLD}$ valid before H1 low	t_{su16}	$\overline{HOLD}$/ $\overline{HOLDA}$ timing See figure 4	9,10,11	13		ns
$\overline{HOLDA}$ valid after H1 low 6/	t_{v4}	See figure 4		0	9	
Pulse width, $\overline{HOLD}$ low	t_{w7}			2		H1 cycles
Pulse width, low 6/	t_{w8}			t_{c2}-5		ns
Delay time, from H1 low to $\overline{STRB}$ high for a $\overline{HOLD}$ 5/ 6/	t_{d37}			0	9	
Disable time, from H1 low to $\overline{STRB}$ high-Z state 5/ 6/	t_{dis4}			0	9	
Enable time, from H1 low to $\overline{STRB}$ active 5/ 6/	t_{en1}	$\overline{HOLD}$/ $\overline{HOLDA}$ timing See figure 4		0	9	
Disable time, from H1 low to R/$\overline{W}$ high-Z state 5/ 6/	t_{dis5}			0	9	
Enable time, from H1 low to R/$\overline{W}$ active 5/ 6/	t_{en2}			0	9	
Disable time, from H1 low to address high-Z state 5/ 6/	t_{dis6}	See figure 4		0	10	
Enable time, from H1 low to address valid 5/ 6/	t_{en3}			0	13	
Disable time, from H1 high to data high-Z state 5/ 6/	t_{dis7}			0	9	
Setup time, general purpose input before H1 low	t_{su17}	Peripheral pin general General purpose I/O timing		10		
Hold time, general-purpose input after H1 low	t_{h13}	See figure 4		0		
Delay time, general purpose output after H1 high	t_{d38}				13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test conditions -55°C ≤ T_C ≤ +125°C 1/ +3.13 V ≤ V_{DD} ≤ +3.47 V unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Setup time, TCLK ext before H1 low	t_{su18}	Timer pin timing See figure 4		9,10,11	10		ns
Hold time, TCLK ext after H1 low	t_{h14}				0		
Delay time, TCLK int valid after H1 high	t_{d38}					9	
Cycle time, TCLK	t_c		External		t_{c2} x 2.6		
			Internal		t_{c2}x 2	t_{c2} x 2^{32}	
Pulse width, TCLK high/low	t_w		External		t_{c2}+ 10		
			Internal		t_{c4}/2-15	t_{c4}/2+5	
Hold time, peripheral pin after H1 high 5/	t_{h15}	Change of peripheral pin from general purpose output to input mode See figure 4				13	
Setup time, peripheral pin before H1 low	t_{su19}				9		
Hold time, peripheral pin after H1 low	t_{h16}				0		
Delay time, from H1 high to peripheral pin switching from input to output	t_{d40}	Change of peripheral pin from general purpose input to output mode See figure 4				13	
Disable time, $\overline{SHZ}$ low to all O, IO high-Z 5/ 6/	t_{dis8}	$\overline{SHZ}$ [P = t_c (Cl)] pin timing See figure 4			0	2P	

1/ Unless otherwise specified, 3.13 V ≤ V_{DD} ≤ 3.47 V. All other test conditions shall be worst case conditions unless otherwise specified.
2/ This parameter is guaranteed but not tested for XA12-XA0.
3/ Pins with internal pull-up devices: INT (0-3), MC/MP, RSV (0-10). Although RSV (0-10) have internal pull-up devices, external pull-ups should be used on each pin.
4/ Actual operating current will be less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the primary bus at the maximum rate possible.
5/ Maximum limit is guaranteed if not tested to the limits specified in table I.
6/ Minimum limit is guaranteed if not tested to the limits specified in table I.
7/ This value is frequency dependent and can be calculated by (delay H_1 low to H_1 high) - (t_{d6}) - (t_{su3}).
8/ Interrupt pulse width must be at least 1 P wide to guarantee it will be seen. It must be less than 2 P wide to guarantee it will be responded to only once. The recommended pulse width is 1.5 P. P = one H1 cycle.

Case X

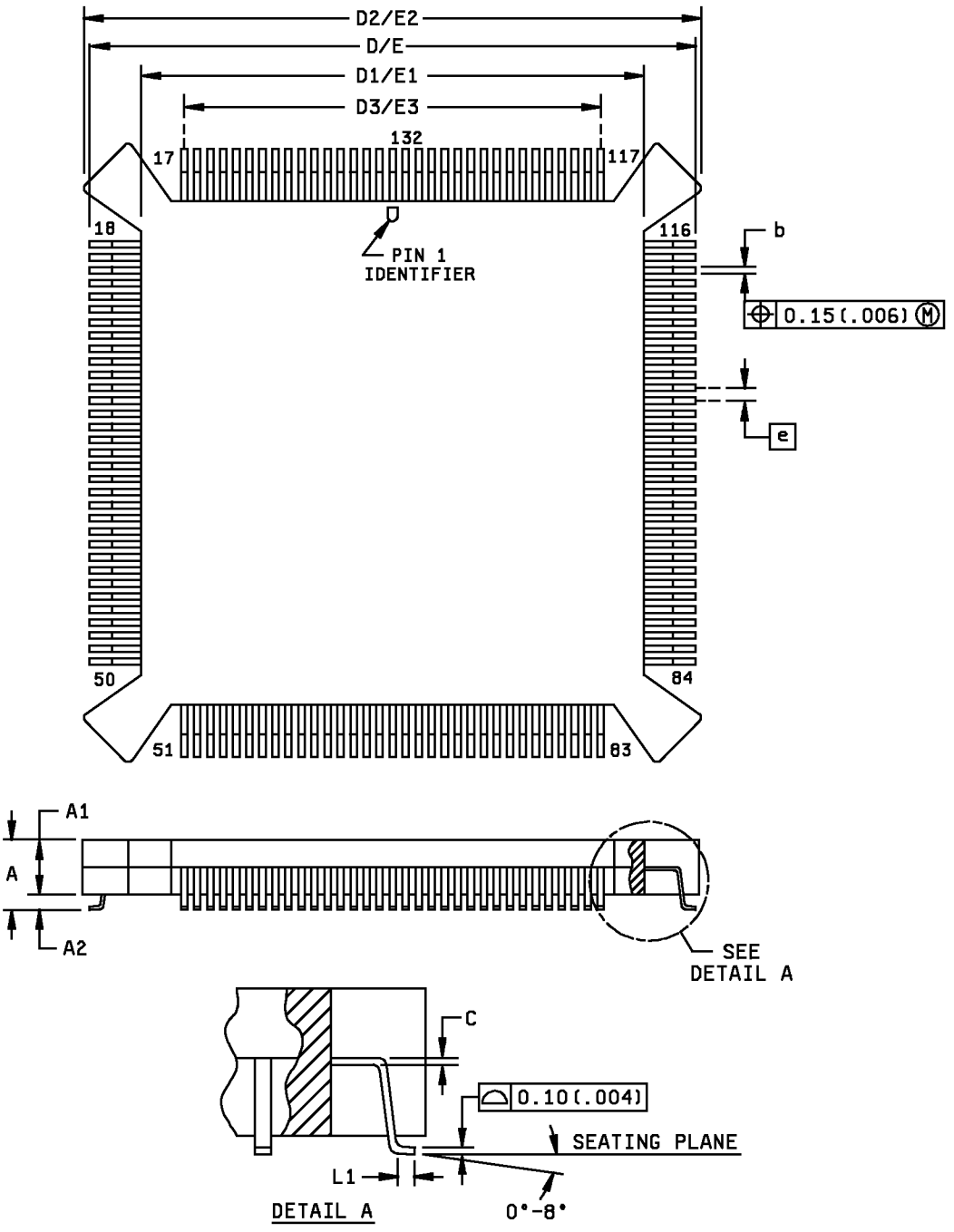


FIGURE 1. Case outline.

Case X				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		4.57		.180
A1	3.30	3.81	.130	.150
A2	0.51		.020	
b	0.20	0.30	.008	.012
c	0.16 BSC		.006 BSC	
D/E	27.18	27.69	1.070	1.090
D1/E1	23.72	24.54	.934	.966
D2/E2	27.64	28.25	1.088	1.112
D3/E3	20.32 BSC		.800 BSC	
e	0.635 BSC		.025 BSC	
L1	0.91	1.17	.036	.046

FIGURE 1. Case outline - Continued.

Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A21	34	D30	67	D9	100	$\overline{INT0}$
2	A20	35	V_{SS}	68	D8	101	V_{SS}
3	V_{SS}	36	V_{SS}	69	V_{SS}	102	V_{SS}
4	V_{SS}	37	V_{SS}	70	V_{SS}	103	$\overline{INT1}$
5	A19	38	D29	71	V_{SS}	104	V_{DD}
6	V_{DD}	39	D28	72	D7	105	V_{DD}
7	A18	40	V_{DD}	73	D6	106	$\overline{INT2}$
8	A17	41	D27	74	V_{DD}	107	$\overline{INT3}$
9	A16	42	V_{SS}	75	D5	108	DR0
10	A15	43	D26	76	D4	109	V_{SS}
11	A14	44	D25	77	D3	110	FSR0
12	A13	45	D24	78	D2	111	CLKR0
13	A12	46	D23	79	D1	112	CLKX0
14	A11	47	D22	80	D0	113	V_{SS}
15	V_{DD}	48	D21	81	H1	114	FSX0
16	A10	49	V_{DD}	82	H3	115	V_{DD}
17	V_{SS}	50	D20	83	V_{DD}	116	DX0
18	A9	51	V_{SS}	84	V_{SS}	117	V_{SS}
19	V_{SS}	52	D19	85	V_{SS}	118	$\overline{SHZ}$
20	A8	53	D18	86	V_{SS}	119	V_{SS}
21	A7	54	D17	87	X2/CLKIN	120	TLCK0
22	A6	55	D16	88	X1	121	V_{DD}
23	A5	56	D15	89	$\overline{HOLDA}$	122	TLCK1
24	V_{DD}	57	V_{SS}	90	$\overline{HOLD}$	123	EMU3
25	A4	58	D14	91	V_{DD}	124	EMU0
26	A3	59	V_{DD}	92	$\overline{RDY}$	125	EMU1
27	A2	60	D13	93	$\overline{STRB}$	126	EMU2
28	A1	61	V_{SS}	94	R/$\overline{W}$	127	MCBL/$\overline{MP}$
29	A0	62	D12	95	$\overline{RESET}$	128	V_{SS}
30	V_{SS}	63	D11	96	XF0	129	A23
31	D31	64	D10	97	V_{DD}	130	A22
32	V_{DD}	65	V_{DD}	98	XF1	131	V_{DD}
33	V_{DD}	66	V_{DD}	99	$\overline{IACK}$	132	V_{DD}

FIGURE 2. Terminal connections.

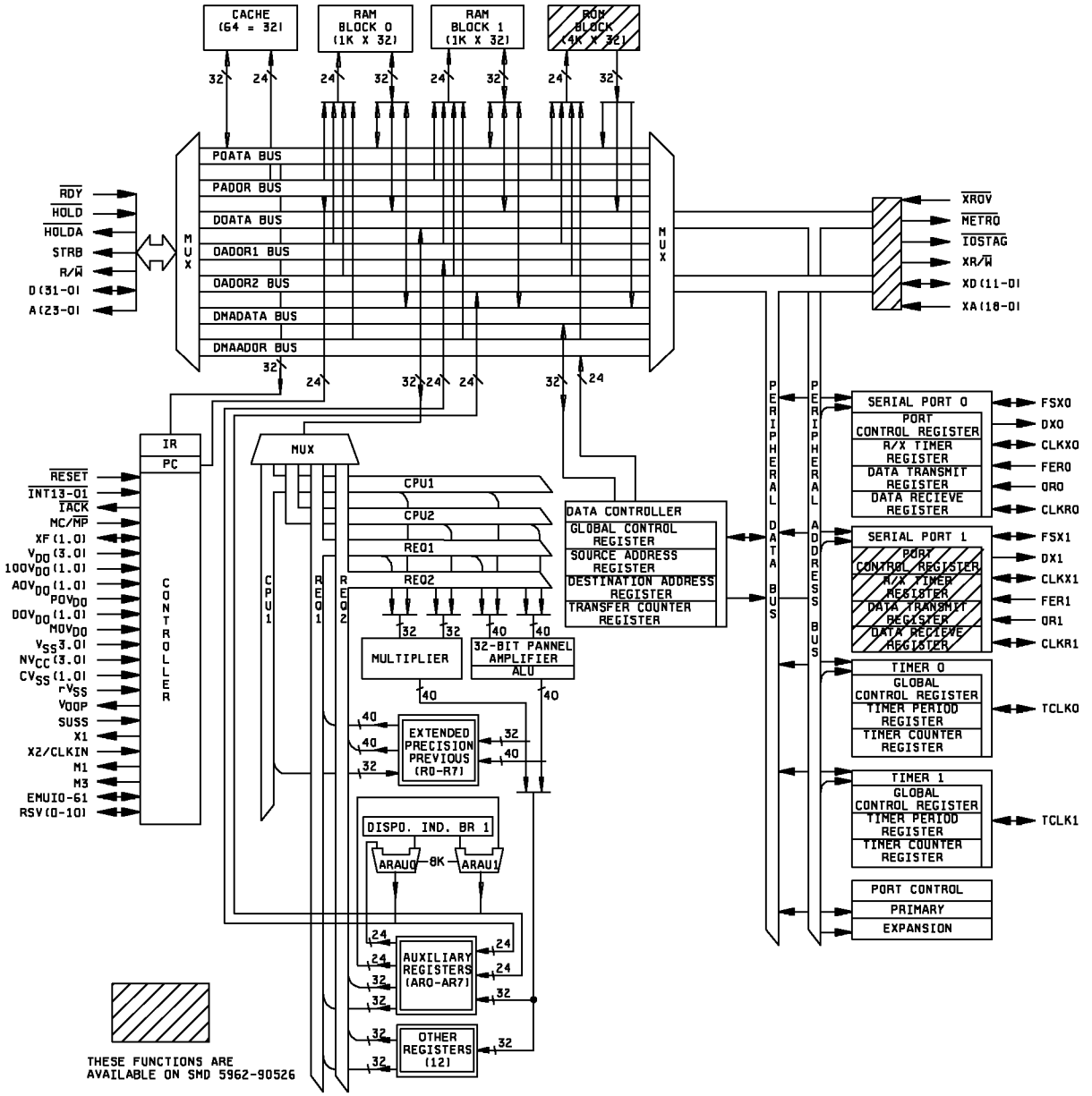
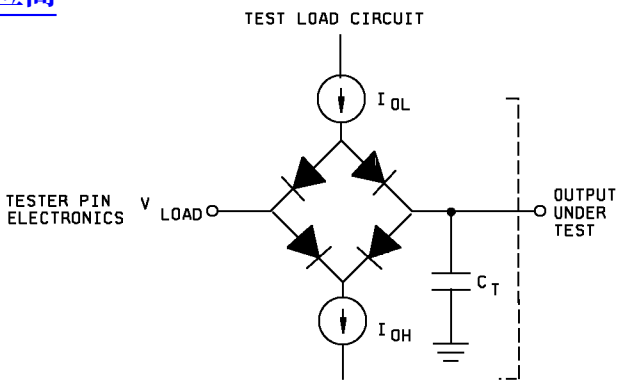


FIGURE 3. Block diagram.



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} =1.54 V to emulate 50 Ω
C_T = 80 pF typical load circuit capacitance.

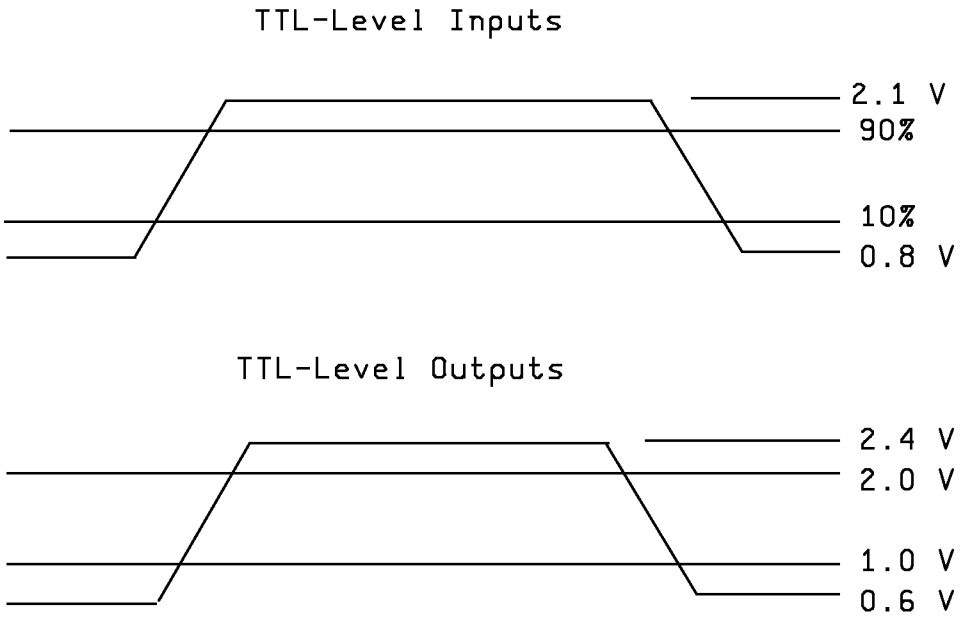


FIGURE 4. Switching waveforms and test circuit.

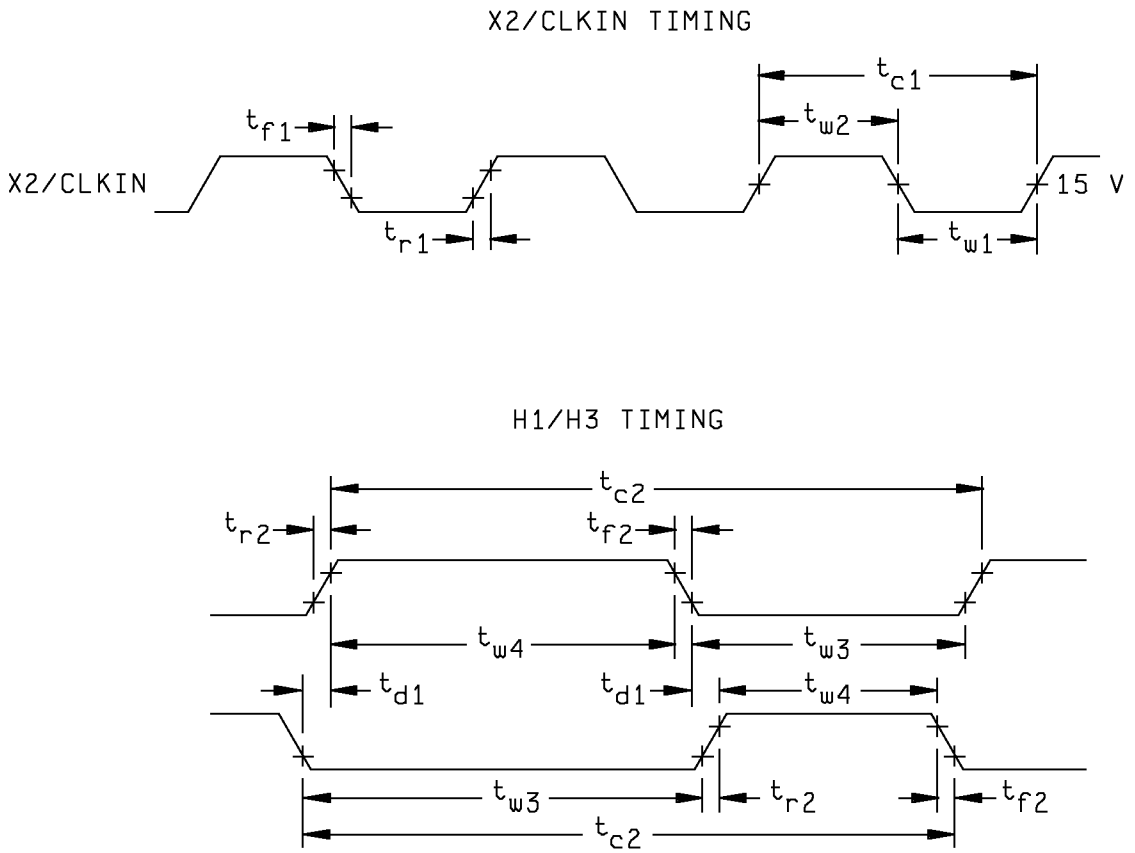


FIGURE 4. Switching waveforms and test circuit - Continued.

Memory ((M)$\overline{\text{STRB}}$ = 0) Read

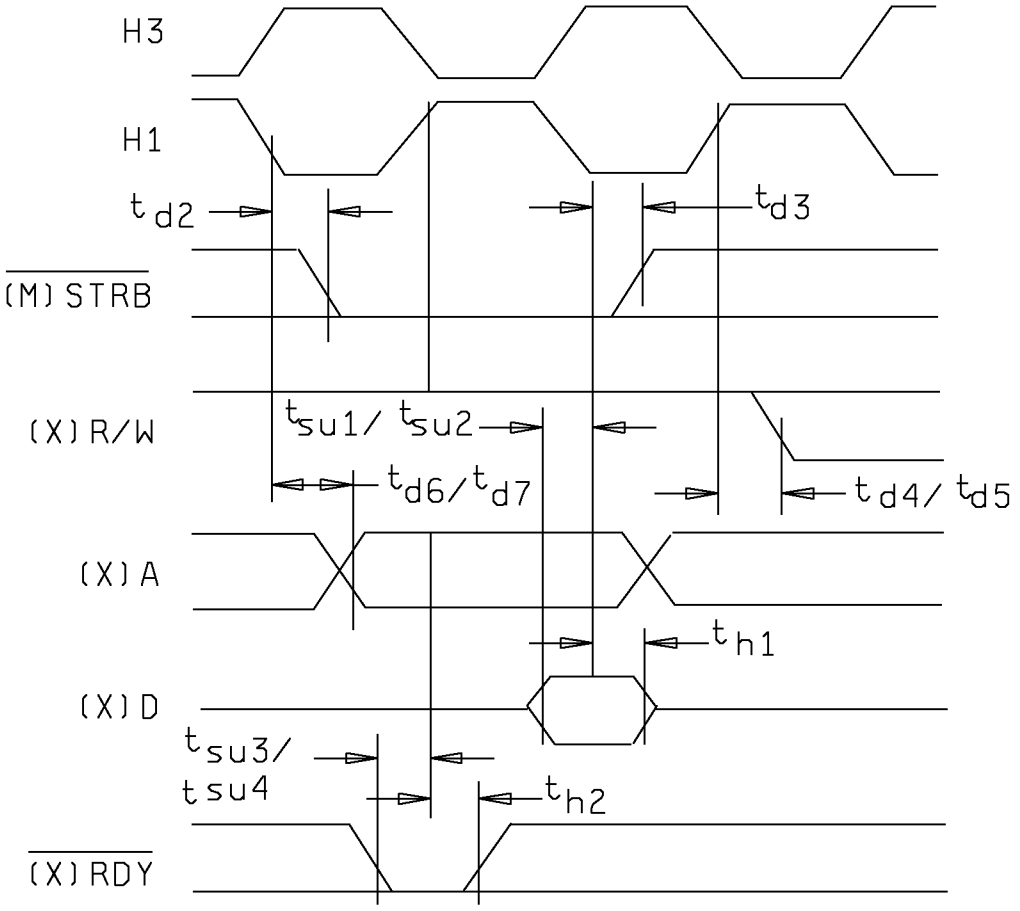
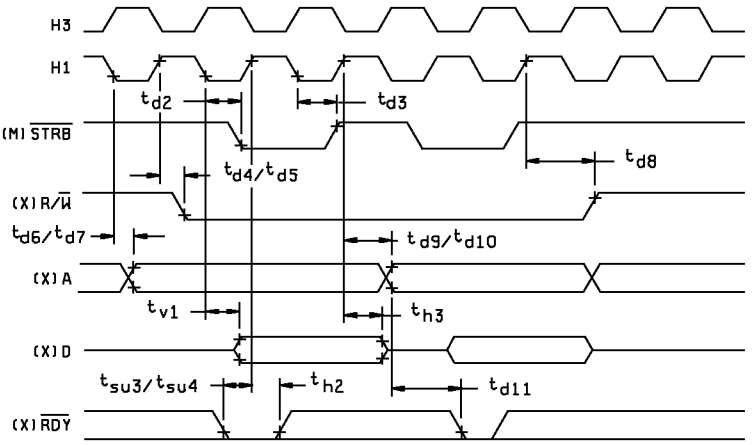


FIGURE 4. Switching waveforms and test circuit - Continued.

Memory ((M)$\overline{\text{STRB}}$ = 0) Write



Memory ((IO)$\overline{\text{STRB}}$ = 0) Read

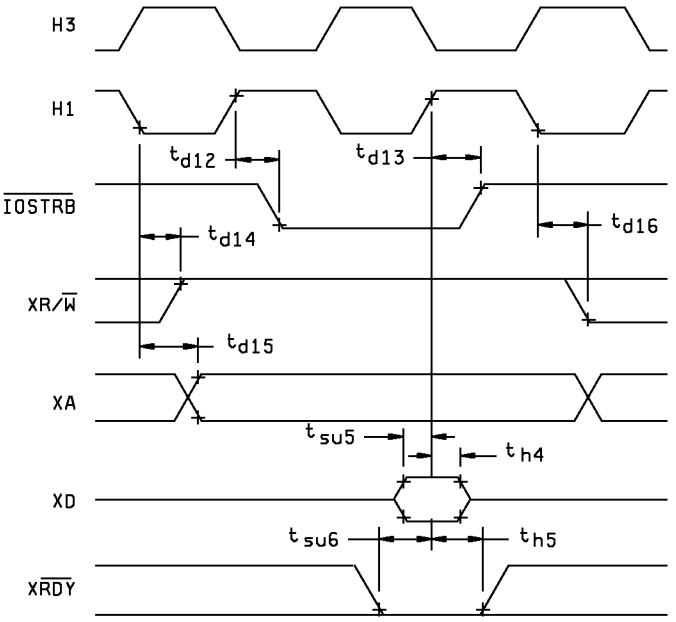
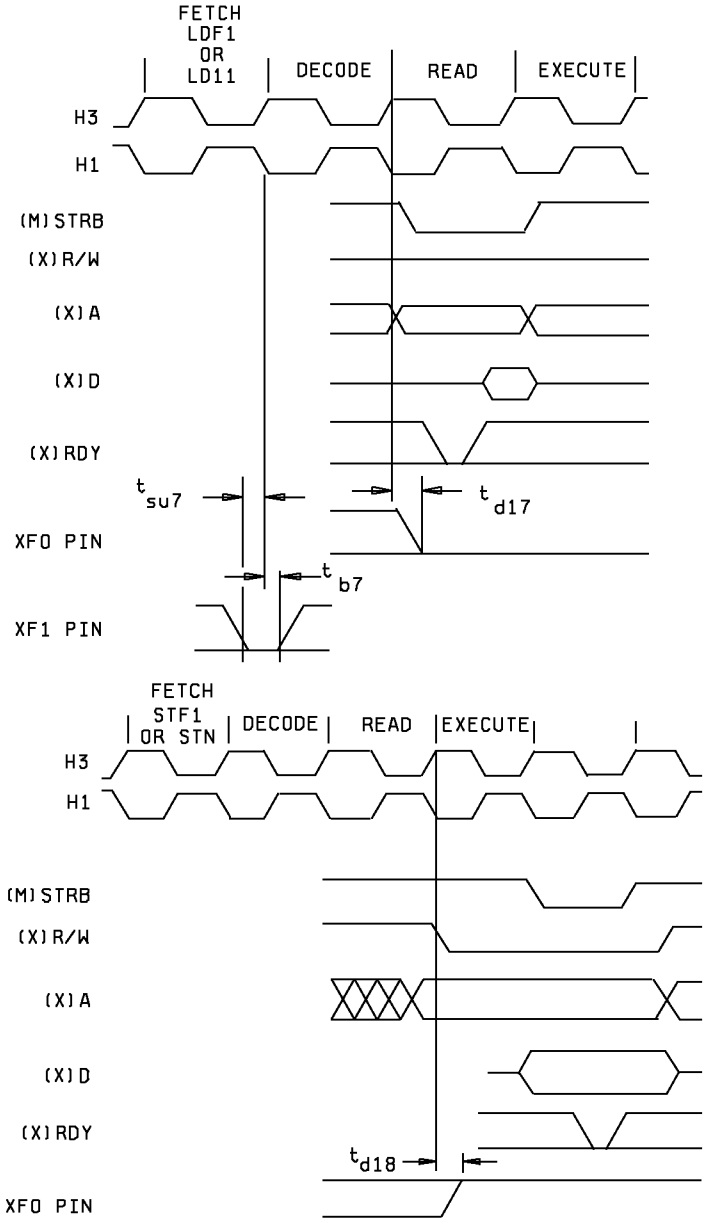


FIGURE 4. Switching waveforms and test circuit - Continued.

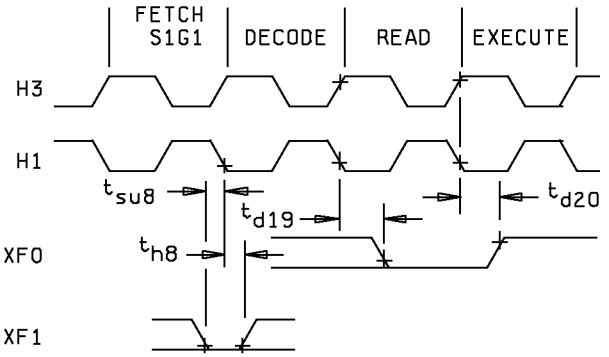
tTiming XF0 and XF1 when executing LDF1 or LDII



Timing for SF0 when executing a STF1 or STII

FIGURE 4. Switching waveforms and test circuit - Continued.

Timing for XF0 and XF1 when executing SIGI



Timing for loading XF register when configured as an output pin

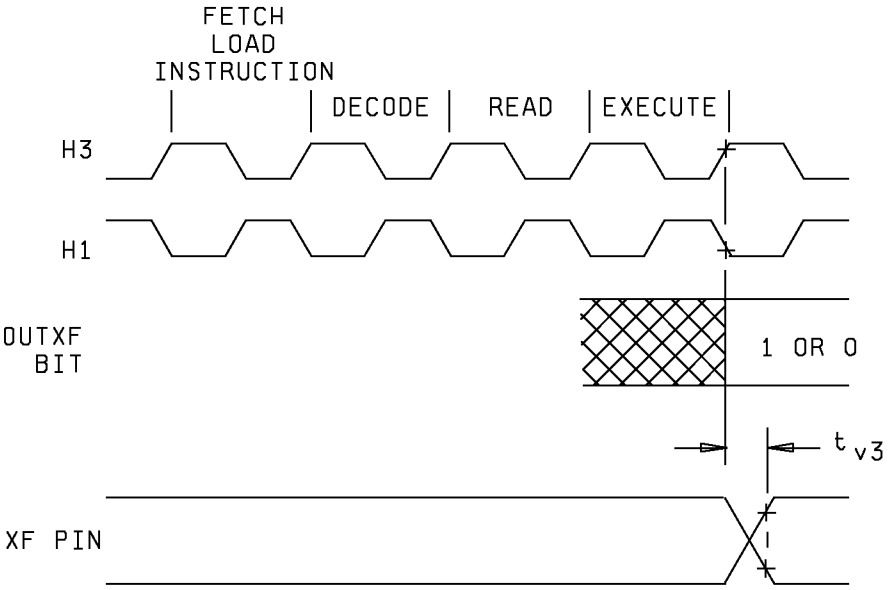
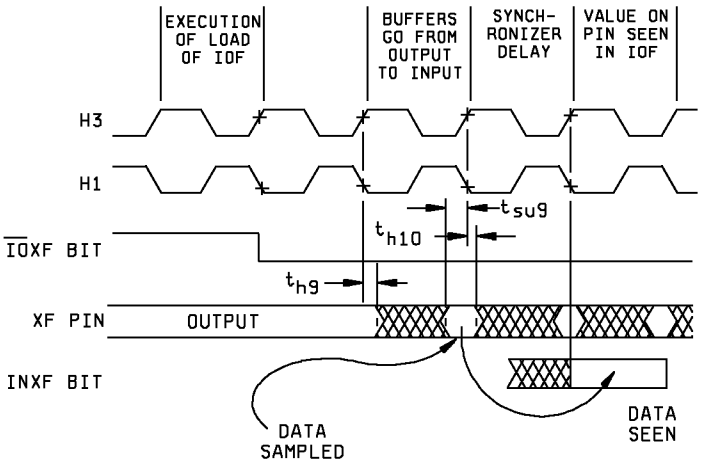


FIGURE 4. Switching waveforms and test circuit - Continued.

Change of XF from output to input mode



Change of XF from input to output mode

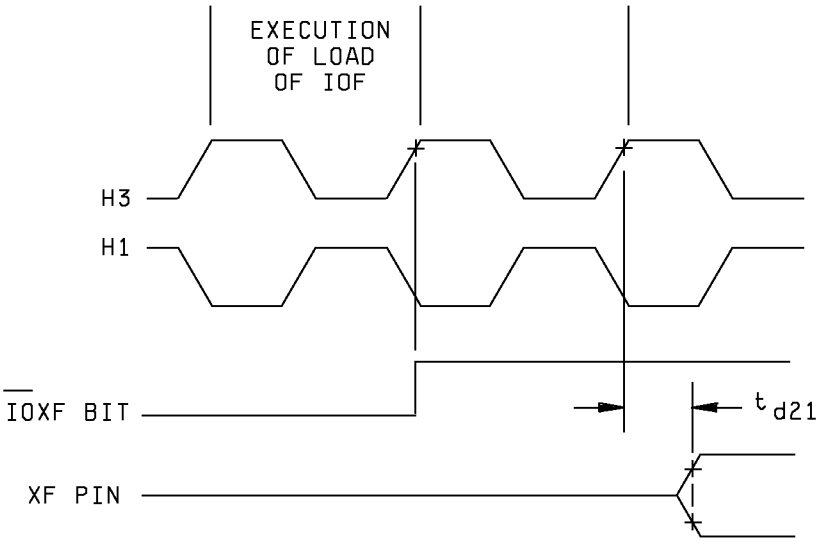
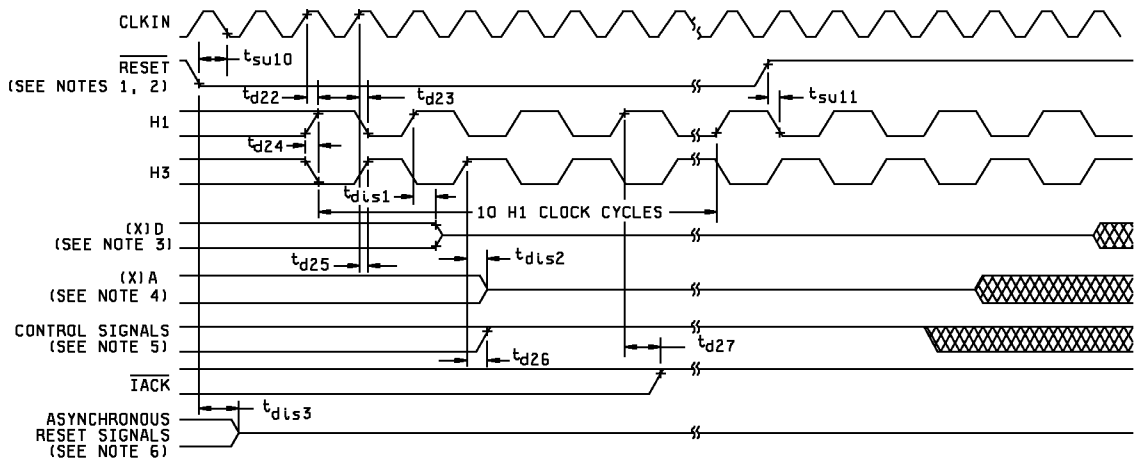


FIGURE 4. Switching waveforms and test circuit - Continued.

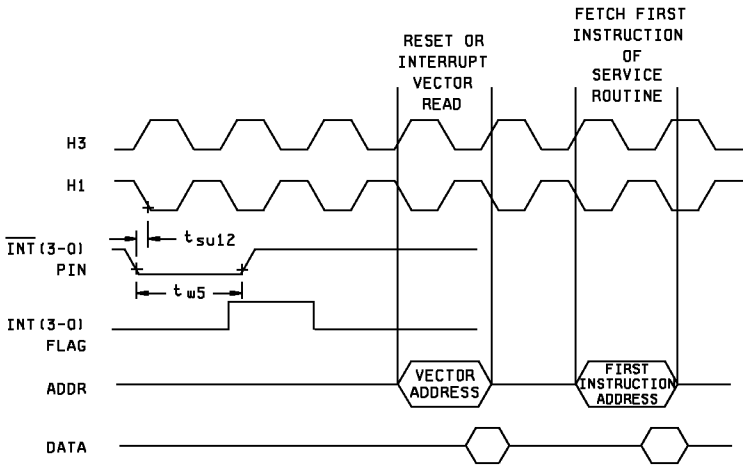


NOTES:

1. RESET is asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.
2. Note that the R/W outputs are placed in a high impedance state during reset and can be provided with a resistive pull-up, nominally 20 KΩ, if desirable spurious writes could be caused when these outputs go low.
3. (X)D includes D(31-0) and XD(31-0).
4. (X)A includes A(23-0), XA(12-0).
5. Control signals include STRB, MSTRB, and IOSTRB.
6. Asynchronously reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, AND TCLK1.

FIGURE 4. Switching waveforms and test circuit - Continued.

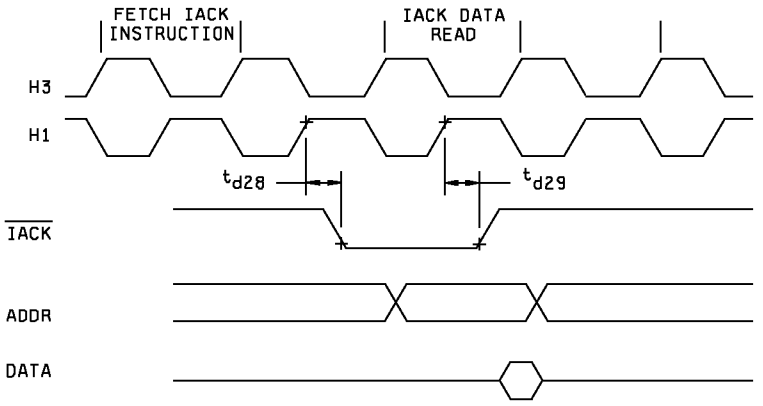
$\overline{\text{INT}}$(3-0) response timing



NOTES:

7. Interrupt pulse width must be at least 1P wide to guarantee it will be seen. It must be less than 2p wide to guarantee it will responded to only once. The recommended pulse width is 1.5 P.
8. $\overline{\text{INT}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

$\overline{\text{IACK}}$ timing

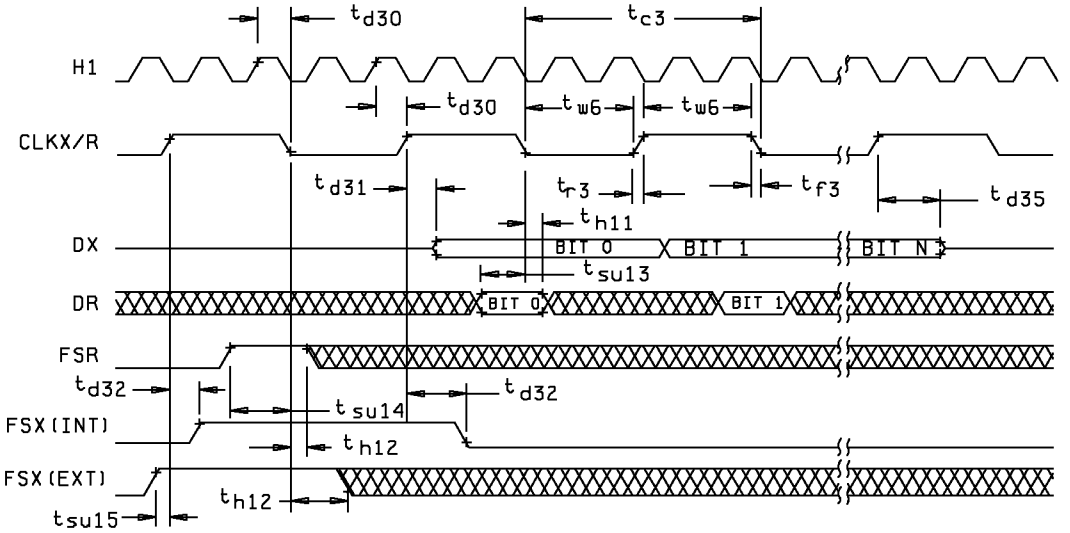


NOTE:

9. The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is therefore extended if the bus cycle utilized wait states.

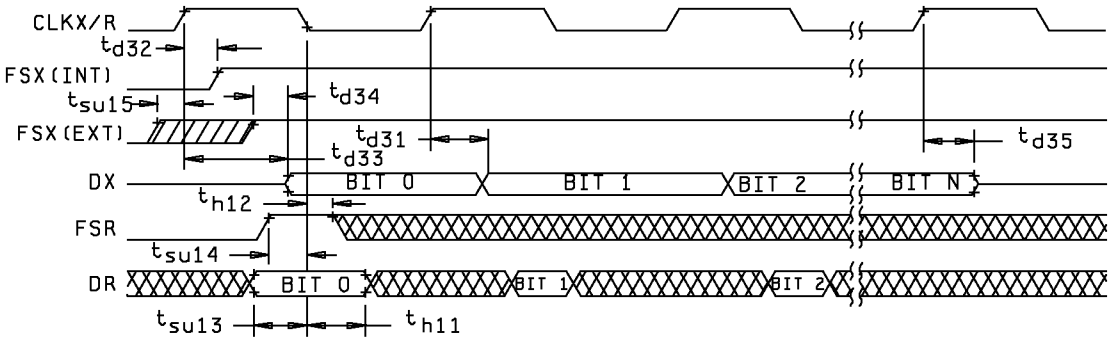
FIGURE 4. Switching waveforms and test circuit - Continued.

Fixed data rate mode



NOTES:
10. Timings diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0
11. These timings are valid for all serial port modes, including handshake, except where otherwise indicated.

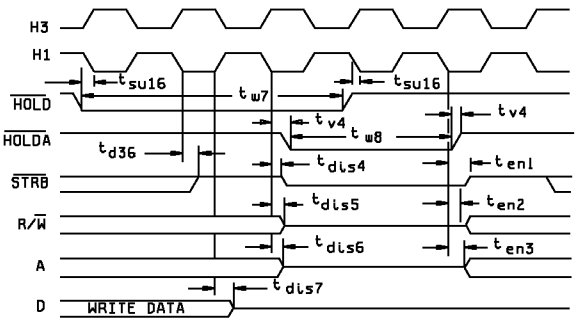
Variable data rate mode



NOTES:
12. Timing diagrams show operation with CLKXP = XLKRP = FSXP = FSRP = 0
13. Timings not expressly specified for variable data rate mode are the same as those for fixed data rate mode.
14. Timings are valid for all serial port modes, includes handshake mode, except where otherwise indicated.

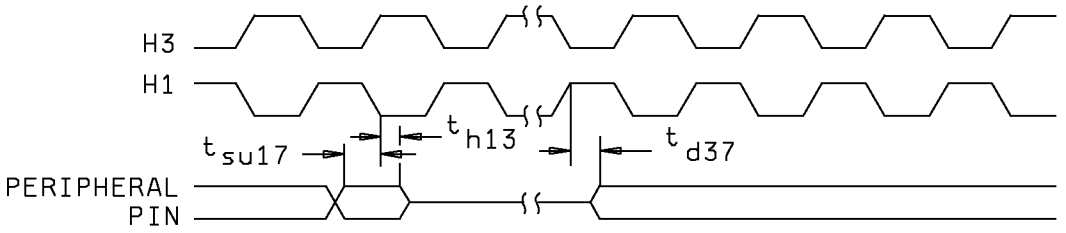
FIGURE 4. Switching waveforms and test circuit - Continued.

HOLD/HOLDA timing



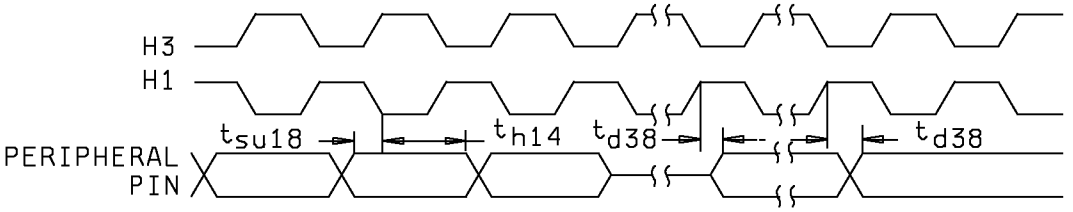
NOTE:
15: HOLD is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown will occur; otherwise, an additional delay of one clock cycle may occur.

Peripheral pin general-purpose I/O timing



NOTE:
16. Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1 FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

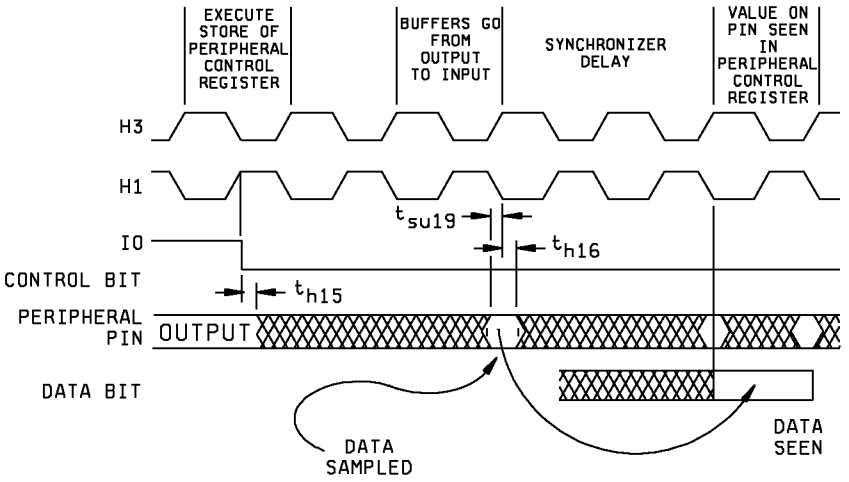
Timer pin timings



NOTE:
17. Period and polarity of valid logic level are specified by contents of internal control registers.

FIGURE 4. Switching waveforms and test circuit - Continued.

Change of peripheral pin from general purpose output to input mode



Change of peripheral pin from general-purpose input to output mode

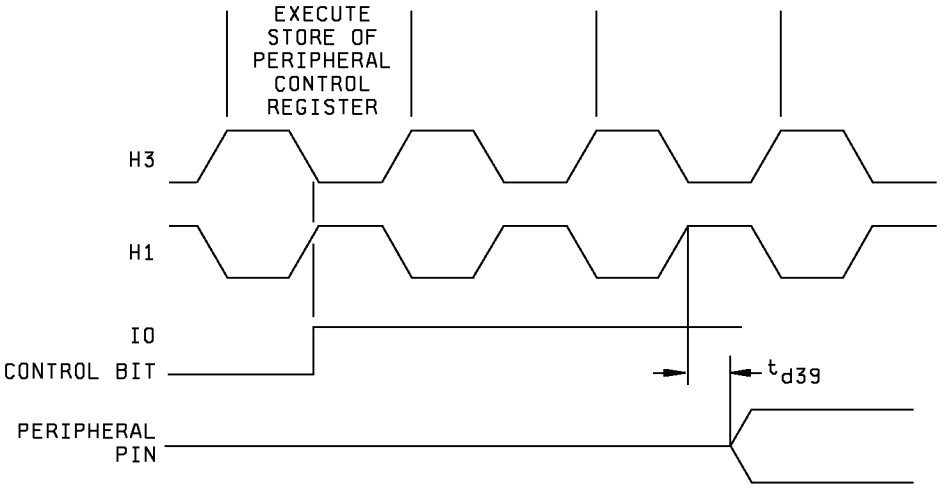


FIGURE 4. Switching waveforms and test circuit - Continued.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Terminal description.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
PRIMARY-BUS INTERFACE			
D31–D0	I/O/Z	32-bit data port	S H R
A23–A0	O/Z	24-bit address port	S H R
R/$\overline{W}$	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S H R
$\overline{STRB}$	O/Z	External-access strobe	S H
$\overline{RDY}$	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.	
$\overline{HOLD}$	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed, A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	

See footnotes at end of table.

TABLE III. Terminal description - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
$\overline{\text{HOLDA}}$	O/Z	Hold acknowledge. $\overline{\text{HOLDA}}$ is generated in response to a logic low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23–A0, D31–D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic high of $\overline{\text{HOLD}}$ or the NOHOLD bit of the primary-bus-control register is set.	S
CONTROL SIGNALS			
$\overline{\text{RESET}}$	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector.	
$\overline{\text{INT3}}$–$\overline{\text{INT0}}$	I	External interrupts	
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge. $\overline{\text{IACK}}$ is generated by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S
MCBL/$\overline{\text{MP}}$	I	Microcomputer boot-loader/microprocessor mode-select	
$\overline{\text{SHZ}}$	I	Shutdown high-impedance. When active, $\overline{\text{SHZ}}$ shuts down the device and places all pins in the high-impedance state. SHZ is used for board-level testing to ensure that no dual-drive conditions occur. Caution: A low on $\overline{\text{SHZ}}$ corrupts the device memory and register contents. Reset the device with SHZ high to restore it to a known operating condition.	
XF1, XF0	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R
SERIAL PORT 0 SIGNALS			
CLKR0	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S R
CLKX0	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DR0	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S R
DX0	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSR0	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S R
FSX0	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S R

See footnotes at end of table.

TABLE III. Terminal description - Continued.

Terminal name	Type 1/	Description	Conditions when signal is Z type 2/
TIMER SIGNALS			
TCLK0	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses, As an output, TCLK0 outputs pulses generated by timer 0.	S
TCLK1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses, As an output, TCLK1 outputs pulses generated by timer 1.	S
SUPPLY AND OSCILLATOR SIGNALS			
H1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
V_{DD}	I	3.3-V supply for the device. All must be connected to a common supply plane. 3/	
V_{SS}	I	Ground. All grounds must be connected to a common ground plane.	
X1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	I	Internal-oscillator input from a crystal or a clock.	
RESERVED 4/			
EMU2–EMU0	I	Reserved for emulation. Use pullup resistors to V_{DD}	
EMU3	O/Z	Reserved for emulation	S

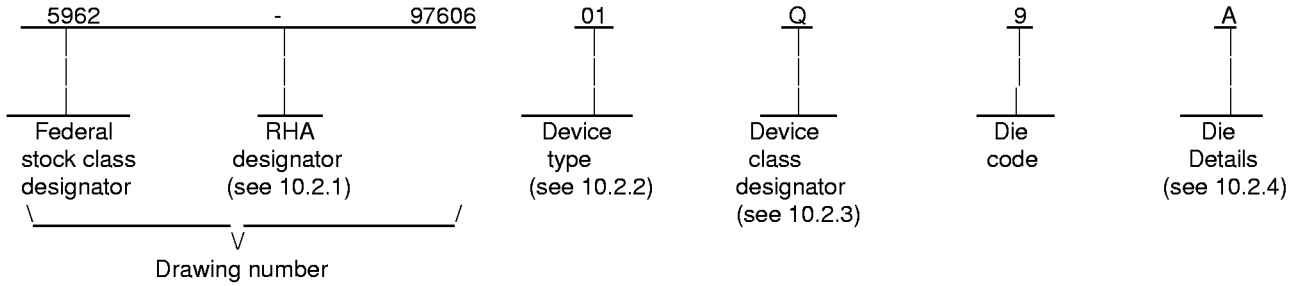
1/ I = input, O = output, Z = high-impedance state.
2/ S = SHZ active, H = HOLD active, R = RESET active.
3/ Recommended decoupling capacitor value is 0.1 : F.
4/ Follow the connections specified for the reserved pins. Use 18-kS – 22-kS pullup resistors for best results. All V_{DD} supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

 Appendix A forms a part of SMD 5962-97606

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320LC31	Digital signal processor, 40 MHz

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4. Die Details. The die details designation shall be a unique letter which designates the die~~s~~ physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

10.2.4.3. Interface materials.

Die type	Figure number
01	A-1

10.2.4.4. Assembly related information.

Die type	Figure number
01	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMDs).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer=s Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer=s QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figures A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer=s identification and the PIN listed in 10.2 herein. The certification mark shall be a AQML@or AQ@as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer=s product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer=s Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

6.0 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die physical dimensions.
Die size: 296 mils x 317 mils.
Die thickness: 19 mils.

Interface materials.
Top metallization: Ti/TiW/AlSiCu.5 500A/3KA/4.5KA
Backside metallization: Silicon

Glassivation.
Type: Ox/N
Thickness: 3kA/ kA

Substrate: Silicon

Assembly related information.
Substrate potential: Biased to Ground
Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
1	0.00	0.00	A9	41	1786.32	-7219.80	D14
2	0.00	-224.46	DVSS	42	1974.78	-7219.80	DVDD
3	0.00	-426.24	A8	43	2162.16	-7219.80	D13
4	0.00	-650.70	A7	44	2350.62	-7219.80	IVSS
5	0.00	-875.16	A6	45	2538.00	-7219.80	D12
6	0.00	-1099.62	A5	46	2748.06	-7219.80	D11
7	0.00	-1302.48	AVDD	47	2958.12	-7219.80	D10
8	0.00	-1504.26	A4	48	3150.90	-7219.80	VDDL
9	0.00	-1728.72	A3	49	3313.26	-7219.80	VDDL
10	0.00	-1953.18	A2	50	3499.38	-7219.80	D9
11	0.00	-2177.64	A1	51	3709.44	-7219.80	D8
12	0.00	-2402.10	A0	52	3897.90	-7219.80	DVSS
13	0.00	-2604.96	CVSS	53	4068.00	-7219.80	VSSL
14	0.00	-2828.34	D31	54	4230.36	-7219.80	VSSL
15	0.00	-3100.32	VDDL	55	4416.48	-7219.80	D7
16	0.00	-3262.68	VDDL	56	4626.54	-7219.80	D6
17	0.00	-3463.20	D30	57	4815.00	-7219.80	DVDD
18	0.00	-3670.38	VSSL	58	5002.38	-7219.80	D5
19	0.00	-3832.74	VSSL	59	5212.44	-7219.80	D4
20	0.00	-4011.66	DVSS	60	5422.50	-7219.80	D3
21	0.00	-4256.64	D29	61	5632.56	-7219.80	D2
22	0.00	-4481.10	D28	62	5842.62	-7219.80	D1
23	0.00	-4669.56	DVDD	63	6052.68	-7219.80	D0
24	0.00	-4950.54	D27	64	6262.74	-7219.80	H1
25	0.00	-5153.40	IVSS	65	6472.80	-7219.80	H3
26	0.00	-5333.58	D26	66	6646.86	-7219.80	DVDD
27	0.00	-5536.44	D25	67	7136.64	-6714.54	DVSS
28	0.00	-5739.30	D24	68	7136.64	-6555.96	CVSS
29	0.00	-5942.16	D23	69	7136.64	-6402.42	IVSS
30	0.00	-6145.02	D22	70	7136.64	-6241.86	X2
31	0.00	-6347.88	D21	71	7136.64	-6072.30	X1
32	0.00	-6522.48	DVDD	72	7136.64	-5780.16	$\overline{\text{HOLDA}}$
33	0.00	-6699.46	D20	73	7136.64	-5574.60	$\overline{\text{HOLD}}$
34	396.72	-7219.80	DVSS	74	7136.64	-5392.62	CVDD
35	577.44	-7219.80	D19	75	7136.64	-5116.14	$\overline{\text{RDY}}$
36	780.30	-7219.80	D18	76	7136.64	-4898.16	$\overline{\text{STRB}}$
37	990.36	-7219.80	D17	77	7136.64	-4673.70	$\overline{\text{RW}}$
38	1200.42	-7219.80	D16	78	7136.64	-4453.74	$\overline{\text{RESET}}$
39	1410.48	-7219.80	D15	79	7136.64	-4235.76	XF0
40	1598.94	-7219.80	CVSS	80	7136.64	-4032.90	CVDD

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

PAD	X CENTER	Y CENTER	PAD NAME	PAD	X CENTER	Y CENTER	PAD NAME
81	7136.64	-3809.52	XF1	107	5248.08	452.52	C0
82	7136.64	-3585.06	$\overline{\text{IACK}}$	108	5063.40	452.52	C1
83	7136.64	-3365.10	$\overline{\text{INT0}}$	109	4878.72	452.52	SCANIN
84	7136.64	-3168.72	DVSS	110	4694.04	452.52	$\overline{\text{INT2}}$
85	7136.64	-2988.54	VSSL	111	4526.46	452.52	CVSS
86	7136.64	-2791.26	$\overline{\text{INT1}}$	112	4324.68	452.52	A23
87	7136.64	-2590.56	VDDL	113	4129.02	452.52	A22
88	7136.64	-2428.20	VDDL	114	3862.62	452.52	VDDL
89	7136.64	-2232.18	$\overline{\text{INT2}}$	115	3700.26	452.52	VDDL
90	7136.64	-2018.70	$\overline{\text{INT3}}$	116	3421.98	452.52	A21
91	7136.64	-1750.32	DR0	117	3226.50	452.52	A20
92	7136.64	-1547.46	CVSS	118	3052.44	452.52	VSSL
93	7136.64	-1345.68	FSR0	119	2901.06	452.52	DVSS
94	7136.64	-1121.22	CLKR0	120	2728.08	452.52	A19
95	7136.64	-896.76	CLKX0	121	2554.02	452.52	AVDD
96	7136.64	-693.90	IVSS	122	2381.04	452.52	A18
97	7136.64	-492.12	FSX0	123	2185.38	452.52	A17
98	7136.64	-289.26	PVDD	124	1989.72	452.52	A16
99	7136.64	-15.48	DX0	125	1794.06	452.52	A15
100	6705.00	452.52	SUBSTRATE	126	1598.40	452.52	A14
101	6480.90	452.52	MCS	127	1316.34	452.52	A13
102	6298.92	452.52	DVSS	128	1120.68	452.52	A12
103	6125.94	452.52	TCLK0	129	925.02	452.52	A11
104	5951.88	452.52	PVDD	130	750.96	452.52	AVDD
105	5721.30	452.52	TCLK1	131	577.98	452.52	A10
106	5439.24	452.52	SCANOUT	132	403.92	452.52	CVSS

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

查询"5962-9760601NXB"供应商

DATE: 00-01-28

Approved sources of supply for SMD 5962-97606 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9760601Q9A	01295	SMJ320LC31KGDM40B
5962-9760601NXB	01295	SMQ320LC31PQM40

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448