



LA74303FN — Monolithic Linear IC

Audio Interface for DSC

Overview

The LA74303FN is a SPEAKER AMP and MIC AMP built-in audio interface for DSC.

Functions

- Three-wire type SERIAL communication, MIC AMP
- MIC power supply incorporated (with built-in pull-up resistor), ALC AMP
- PB input method: Compatible with analog or digital ($\Delta\Sigma$) signal input
- 3rd order LPF(compatible with REC/PB changeover, $f_c=4\text{kHz}$ or 11kHz selectable)
- SPEAKER AMP (compatible with BEEP input MIX)
- Electronic VOLUME (compatible with SERIAL communication control)
- LINE output (with SERIAL MUTE), compatible with STANDBY control

Specifications

Maximum Ratings at $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CCA\text{ max}}$		5.0	V
Maximum supply voltage 2	$V_{CCSP\text{ max}}$		5.0	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 85^\circ\text{C}^*$	500	mW
Operating temperature	T_{opr}		-15 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Substrate mounting condition (30mm × 50mm × 0.8mm: glass epoxy) 2S2P

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

LA74303FN

Operating Conditions: $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CCA}		3.0	V
	V_{CCSP}		3.3	V
Allowable operating voltage range	V_{CCA}		2.7 to 3.6	V
	V_{CCSP}	Take care not to exceed Pd max.	2.7 to 3.6	V

Electrical Characteristics at $T_a=25^{\circ}\text{C}$, $V_{CCA}=3.0\text{V}$, $V_{CCSP}=3.3\text{V}$, $f=1\text{kHz}$, with the VREF capacitance charging circuit in the OFF MODE

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current						
V _{CCA} current dissipation at no signal 1	I _{CCA1}	V _{CCA} =3.0V	7	9.4	11.8	mA
V _{CCA} current dissipation at no signal 2	I _{CCA2}	V _{CCA} =3.0V: REC BLOCK (MIC/ALC/REC AMP) POWER SAVE MODE	5	6.7	8.4	mA
V _{CCA} current dissipation at no signal 3	I _{CCA3}	V _{CCA} =3.0V: LINE AMP POWER SAVE MODE	6.5	8.7	10.9	mA
V _{CCA} standby current dissipation	I _{CCAS}	V _{CCA} =3.0V: during standby control (4PIN=0V application)			1	μA
Current dissipation at no signal 5	I _{CCSP1}	V _{CCSP} =3.3V: SPK POWER ON MODE	1.2	2.5	5	mA
Current dissipation at no signal 6	I _{CCSP2}	V _{CCSP} =3.3V: SPK POWER SAVE MODE		0.05	0.1	mA
V _{CCSP} standby current dissipation	I _{CCSPS}	V _{CCSP} =3.3V: during standby control (4PIN=0V application)		5.5	10	μA
REC output system						
REC reference output LEVEL	VOR	ALC IN, V _{IN} =-49dBV	-16.5	-15.5	-14.5	dBV
REC reference output distortion	HDR	ALC IN, V _{IN} =-49dBV, THD: from 2nd to 5th harmonic		0.05	0.1	%
ALC characteristics 1	ALM1	ALC IN, V _{IN} =-33dBV (standard+16dB)	-11	-8	-5	dBV
ALC distortion 1	ALMD1	ALC IN, V _{IN} =-33dBV (standard+16dB), THD: from 2nd to 5th harmonic		0.15	0.5	%
ALC characteristics 2	ALM2	ALC IN, V _{IN} =-17dBV (standard+32dB)	-11	-8	-5	dBV
ALC distortion 2	ALMD2	ALC IN, V _{IN} =-17dBV (standard+32dB), THD: from 2nd to 5th harmonic		0.2	1	%
ALC IN max input level	VINRMX	ALC IN LEVEL at which REC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-10	dBV
REC output noise voltage	VNOR	ALC IN, no input, JIS-A Filter		-77	-68	dBV
REC output frequency characteristics 1	FEQR1	ALC IN, V _{IN} =-33dBV, comparison of f=4kHz/1kHz	-5	-3.5	-2	dB
REC output frequency characteristics 2	FEQR2	ALC IN, V _{IN} =-33dBV, comparison of f=22kHz/1kHz		-33	-25	dB
REC output frequency characteristics 3	FEQR3	ALC IN, V _{IN} =-33dBV, comparison of f=100kHz/1kHz		-60	-55	dB
LINE output system						
LINE reference output LEVEL	VOL	PB IN, V _{IN} =-15dBV	-12	-11	-10	dBV
LINE reference output distortion rate	HDL	PB IN, V _{IN} =-15dBV, THD: from 2nd to 5th harmonic		0.1	0.2	%
LINE reference output noise voltage	VNOL	PB IN, no input, JIS-A Filter		-85	-77	dBV
PB IN max input LEVEL	VINPMX	PB IN LEVEL at which LINE output THD (from 2nd to 5th harmonic) becomes 3% or less.			-5	dBV
LINE output frequency characteristics 1	FEQP1	PB IN, V _{IN} =-8dBV, comparison of f=4kHz/1kHz	-5	-3.5	-2	dB
LINE output frequency characteristics 2	FEQP2	PB IN, V _{IN} =-8dBV, comparison of f=22kHz/1kHz		-33	-25	dB
LINE output frequency characteristics 3	FEQP3	PB IN, V _{IN} =-8dBV, comparison of f=100kHz/1kHz		-65	-60	dB

Continued on next page.

LA74303FN

Continued from preceding page.

[查询"LA74303FN"供应商](#)

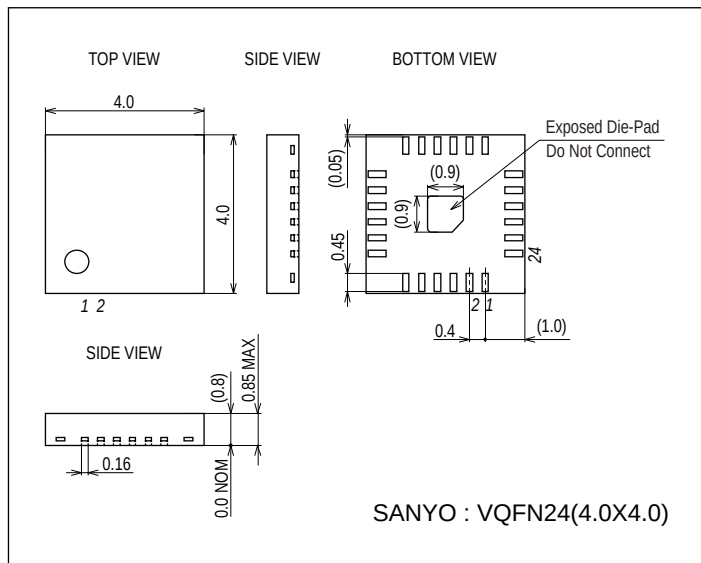
查询 LA/43031N 供应商

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SP output system (SP load = as measured at both ends of 8Ω)						
SP reference output LEVEL1 (Vol.MAX)	VOSP1	PB IN, V _{IN} =-15dBV, Vol=MAX (Serial DATA=31)	-5	-2	1	dBV
SP reference output distortion	THDSP	PB IN, V _{IN} =-15dBV, Vol=MAX, THD: from 2nd to 5th harmonic		0.4	1	%
SP reference output LEVEL2 (Vol.TYP)	VOSP2	PB IN, V _{IN} =-15dBV, Vol=TYP (Serial DATA=17)	-19	-13	-7	dBV
SP reference output LEVEL3 (Vol.MIN)	VOSP3	PB IN, V _{IN} =-15dBV, Vol=MIN (Serial DATA=0), JIS-A Filter		-80	-70	dBV
SP reference output noise voltage	VNOSP	PB IN, no input, Vol=MAX, JIS-A Filter		-76	-70	dBV
SP maximum ratings output	VOMSP	PB IN, Vol=MAX, LEVEL at which THD=10%	200	340		mW
MIC output system						
MIC voltage gain	VGMIC	MIC IN, V _{IN} =-39dBV	19	20	21	dB
MIC output distortion	HDMIC	MIC IN, V _{IN} =-39dBV, THD: from 2nd to 5th harmonic		0.02	0.1	%
MIC output noise voltage	VNOMIC	MIC IN, no input, JIS-A Filter		-94	-83	dBV
MIC IN max input level	VINMMX	MIC IN LEVEL at which the MIC output THD (from 2nd to 5th harmonic) becomes 3% or less.			-22	dBV
MIC V _{CC} output voltage	VMIC	At 6.2kΩ load	1.5	1.7	1.9	V
Control system						
Serial CLOCK frequency	FCLK			1.25	1.5	MHz
Serial input LOW level	SERLO		0		0.7	V
Serial input HIGH level	SERHI		2.3		3.5	V

Package Dimensions

unit : mm (typ)

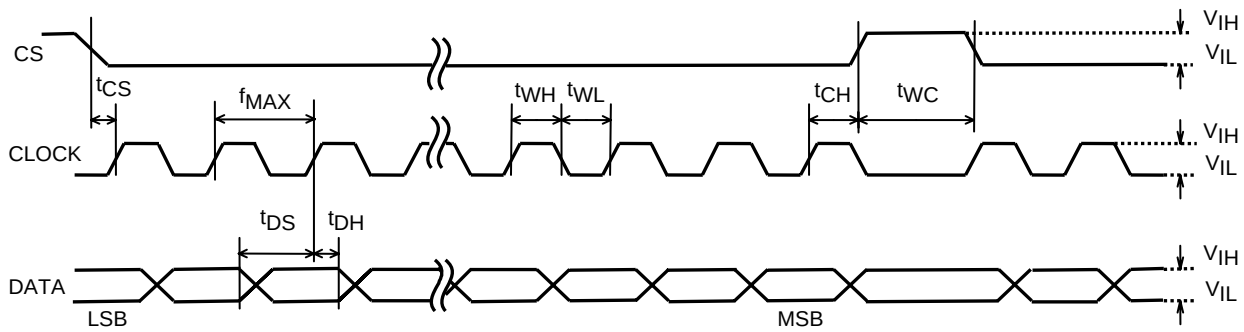
3364



Description of the Content of Serial Communication

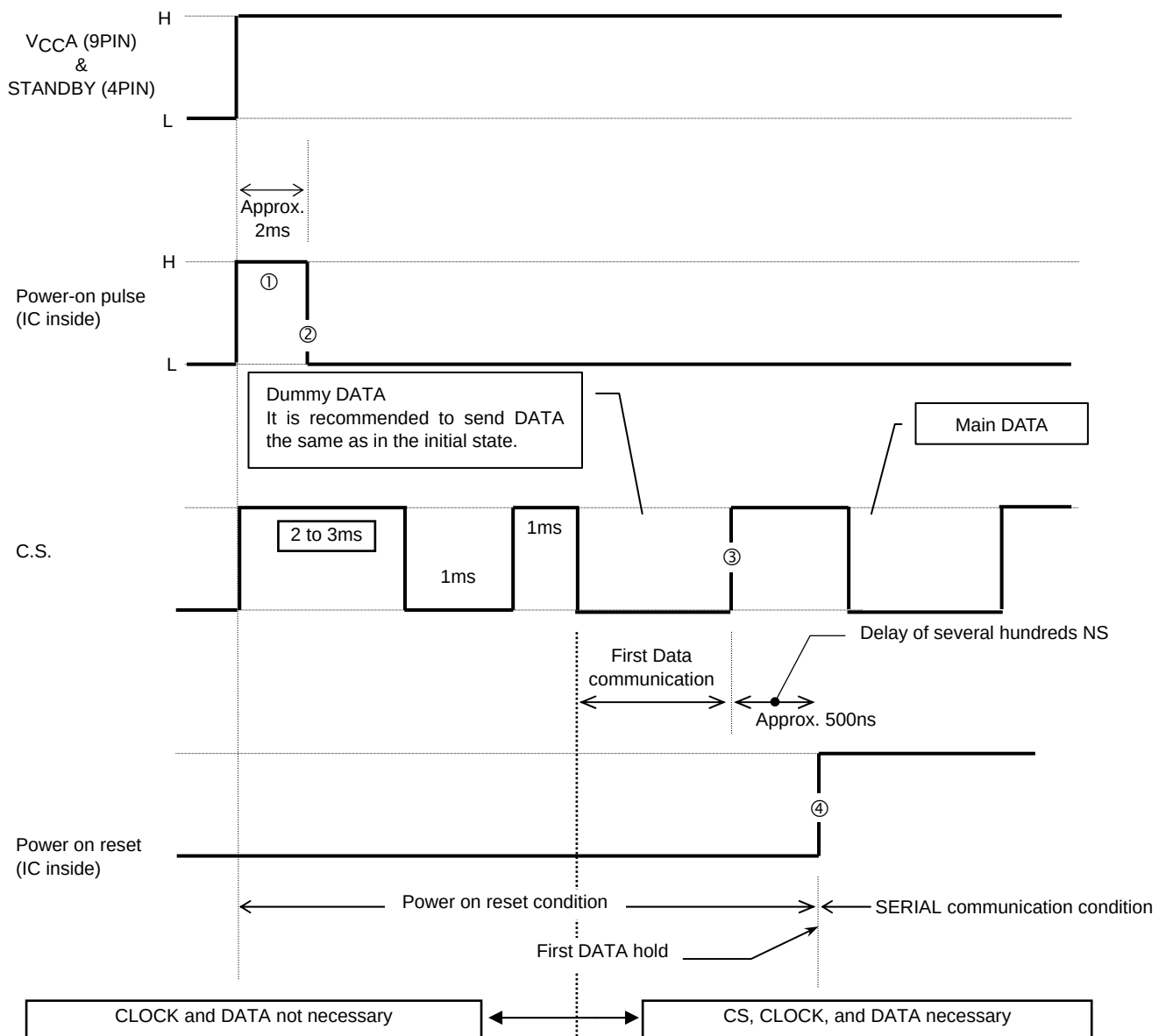
DATA No.	Parameter	Default
0	DUMMY	0
1	LPF Cut-off frequency SW	0:11kHz, 1:4kHz
2	VREF capacitor charging circuit control SW	0:ON, 1:OFF
3	MIC AMP POWER SW	0:ON, 1:OFF
4	ALC AMP POWER SW	0:ON, 1:OFF
5	LPF1 MODE SW	0:PB MODE1, 1:REC MODE
6	LPF1/LPF2 selection SW	0:LPF1, 1:LPF2
7	REC BLOCK POWER SW	0:ON, 1:OFF
8	LINE OUT POWER SW	0:ON, 1:OFF
9	LINE MUTE SW	0:ON, 1:OFF
10	SPK POWER SW	0:ON, 1:OFF
11	DATA=1	1 1 1 1 1: VOL MAX
12	DATA=2	to
13	DATA=4	0 0 0 0 0: VOL MIN (MUTE)
14	DATA=8	* EVR setting (the numeral shown in the left is decimal.
15	DATA=16	For characteristics, see P18.)

Serial Transmission Timing



- f_{MAX} (Max clock frequency) 1.5MHz
- t_{WL} (Clock pulse width: Low) 333ns or more
- t_{WH} (Clock pulse width: High) 333ns or more
- t_{CS} (Chip enable setup time) 333ns or more
- t_{CH} (Chip enable hold time) 333ns or more
- t_{DS} (Data setup time) 333ns or more
- t_{DH} (Data hold time) 333ns or more
- t_{WC} (Chip enable pulse width) 333ns or more
- V_{IH} (High voltage lower limit) 2.3V to 3.5V
- V_{IL} (Low voltage upper limit) 0V to 0.7V

POWER ON Condition (SERIAL communication)



The POWER ON RESET state covers a period up to the rise ③ of the second C.S. input after fall ② of POWER ON PULSE ① generated inside IC when the power is applied and the STANDBY control is canceled. ③ is the dummy communication. (It is recommended to send DATA the same as in the initial state.)

Actually, because of delay of several hundreds ns in the IC, the first DATA condition begins in ④ and the normal SERIAL communication condition begins after ④.

Method of Measuring Electric Characteristics at Ta=25°C, VCCA=3.0V, VCCSP=3.3V,
f=1kHz VREF capacitor charging circuit OFF MODE

No.	Symbol	Input		Output	STANDBY pin	Serial control setting																
		Pin	Conditions	Pin																		
Major conditions (for the serial control setting, see the table in the right)					Voltage applied to pin 4	DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW (1.):REC (0.0):PB Analog (0.1):PB Digital		REC P SW	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	
*	0:11kHz 1:4kHz	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF		0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	
*																						
Circuit current																						
1	ICCA1	9	VCCA=3.0V No input	9	3.3V	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
2	ICCA2	9	VCCA=3.0V No input	9	3.3V	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
3	ICCA3	9	VCCA=3.0V No input	9	3.3V	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
4	ICCA5	9	VCCA=3.0V No input	9	0V	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	ICCS1	22	VCCSP=3.3V No input	22	3.3V	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	ICCS2	22	VCCSP=3.3V No input	22	3.3V	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
7	ICCSPS	22	VCCSP=3.3V No input	22	0V	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
REC output system																						
8	VOR	14	VIN=49dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0
9	HDR1	14	VIN=49dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0
10	ALM1	14	VIN=33dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0
11	ALMD1	14	VIN=33dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0
12	ALM2	14	VIN=17dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
13	ALMD2	14	VIN=17dBV f=1kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
14	VINRMX	14	f=1kHz	12&14	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
15	VNOR	14	No input	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
16	FEQR1	14	VIN=33dBV f=4kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
17	FEQR2	14	VIN=33dBV f=22kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0
18	FEQR3	14	VIN=33dBV f=100kHz	12	3.3V	0	1	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0

查询"LA74303FN"供应商

No.	Symbol	Input		Output		STANDBY pin	Serial control setting																																									
		Pin	Conditions	Pin	Major conditions (for the serial control setting, see the table in the right)		0	1	2	3	4	5		6	7	8	LINE P SW	LINE Mute	SPK P SW	EVR1 DATA	12	13	14	15																								
												LPF C SW	CHRG P SW												MIC P SW	ALC P SW	LPF MODESW (1,*):REC	REC P SW	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON	0:OFF 1:ON													
																																				DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:ON 1:OFF	0:OFF 1:ON	0:OFF 1:ON
LINE output system																																																
19	VOL1	10	VIN=15dBV f=1kHz	5	400 to 20kHz LPF used	3.3V	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	0	0	0																							
20	HDL	10	VIN=15dBV f=1kHz	5	400 to 20kHz LPF used THD: from 2nd to 5th harmonic	3.3V	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	0	0	0	0																							
21	VNOL	10	No input	5	JIS-A FILTER used	3.3V	0	1	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0																							
22	VINPMX	10	f=1kHz	5	400 to 20kHz LPF used Pin 10 level at which pin 5 becomes THD = 3% (from 2nd to 5th harmonic)	3.3V	0	1	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0																							
23	FEQP1	10	VIN=8dBV f=4kHz	5	f=4kHz/1kHz level ratio	3.3V	0	1	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0																							
24	FEQP2	10	VIN=8dBV f=22kHz	5	f=22kHz/1kHz level ratio	3.3V	0	1	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0																							
25	FEQP3	10	VIN=8dBV f=100kHz	5	f=100kHz/1kHz level ratio	3.3V	0	1	1	1	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0																							
SPK output system (both ends of SPK: measured with 8Ω)																																																
26	VOSP1	10	VIN=15dBV f=1kHz	21 23	400 to 20kHz LPF used Vol.=MAX	3.3V	0	1	1	1	1	1	0	0	1	1	0	1	0	1	1	1	1	1	1																							
27	THDSP	10	VIN=15dBV f=1kHz	21 23	400 to 20kHz LPF used Vol.=MAX, THD: from 2nd to 5th harmonic	3.3V	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1	1	1	1																							
28	VOSP2	10	VIN=15dBV f=1kHz	21 23	400 to 20kHz LPF used Vol.=TYP	3.3V	0	1	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	1	1																							
29	VOSP3	10	VIN=15dBV f=1kHz	21 23	JIS-A FILTER used Vol.=MIN	3.3V	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0																							
30	VNOSP	10	No input	21 23	JIS-A FILTER used Vol.=MAX	3.3V	0	1	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1																							
31	VOSSP	10	f=1kHz	21 23	400 to 20kHz LPF used Level at which V _{OH} =MAX and THD=10% (from 2nd to 5th harmonic)	3.3V	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1	1	1	1																							
MIC output system																																																
32	VGMIC	17	VIN=39dBV f=1kHz	15	400 to 20kHz LPF used	3.3V	0	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0																							
33	HDMIC	17	VIN=39dBV f=1kHz	15	400 to 20kHz LPF used THD: from 2nd to 5th harmonic	3.3V	0	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0																							
34	VNMIC	17	No input	15	JIS-A FILTER used	3.3V	0	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0																							
35	VINMMX	17	f=1kHz	15	400 to 20kHz LPF used Pin 17 level at which pin 15 becomes THD = 3% (from 2nd to 5th harmonic)	3.3V	0	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0																							
36	VMIC	17	No input	18	PIN 18: Measurement of output voltage (under 6.2kΩ load)	3.3V	0	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0																							

Description of Pin Functions

Pin No.	Pin Description
1	Speaker input
2	MIX output
3	BEEP input
4	STANDBY control
5	LINE output
6	C.S. input
7	CLOCK input
8	DATA input
9	V _{CCA}
10	PB input
11	A GND
12	REC output
13	ALC detection
14	ALC input
15	MIC output
16	MIC GND
17	MIC input
18	INT power supply for MIC
19	Ripple rejection for VREFL
20	SPK GND
21	Speaker positive-phase output
22	V _{CCSP}
23	Speaker negative-phase output
24	SPK GND

LA74303FN Internal Equivalent Diagram and Recommended Circuit Diagram

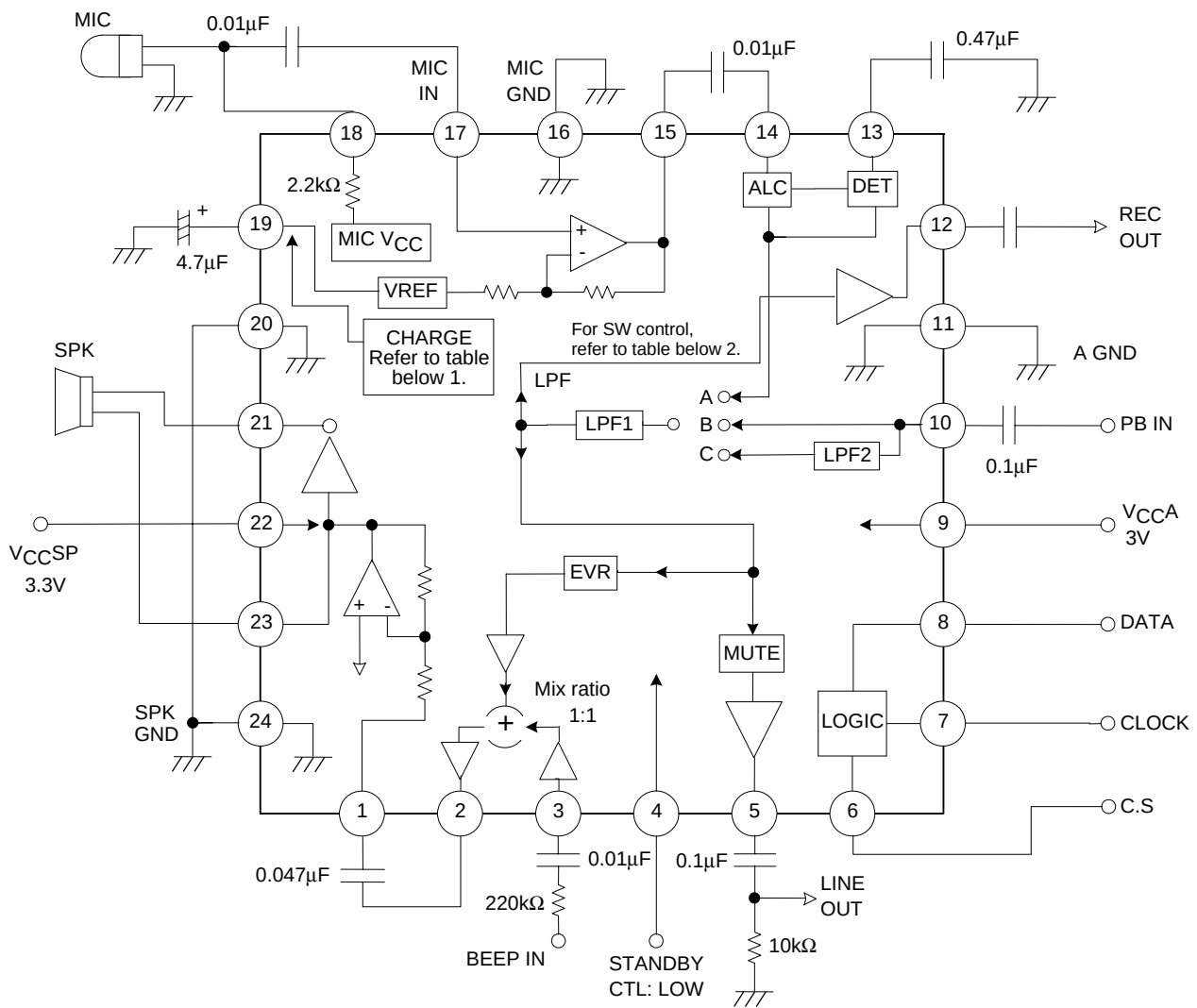


Table 1: Logic of external capacitor charging circuit

SERIAL	No.2
ON	0
OFF	1

Initially "ON"

Table 2: LPF SW control logic

SERIAL	No.5	No.6
A	1	*
B	0	0
C	0	1

*) Don't care.

LA74303FN

Table of Input/Output Forms of LA74303FN

Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
1	SP IN	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Speaker input pin	
23	SPK OUT-	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Pin for output of speaker reversed phase	
2	MIX OUT	1.58V	At PB reference input Output level = -8dBV	EVR output pin	
3	BEEP IN	1.64V	Maximum input level = -8dBV		
4	STANDBY L			STANDBY control pin 2V or more: STANDBY canceled	
5	LINE OUT	1.52V	At PB reference input Output level = -11dBV	LINE output pin	
6	CS			CS input pin	
7	CLOCK			CLOCK input pin	
8	DATA			DATA input pin	

Continued on next page.

LA74303FN

Continued from preceding page.

LA74303FN 供应商

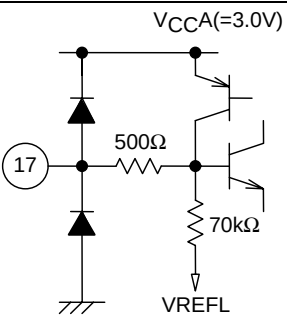
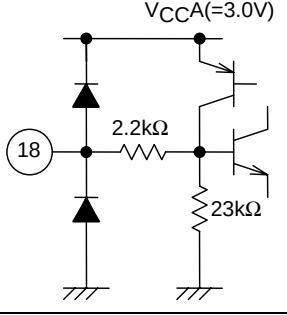
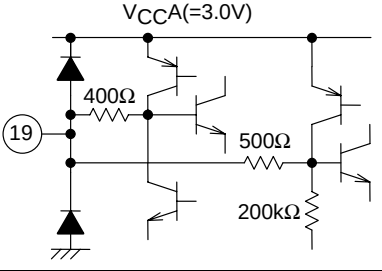
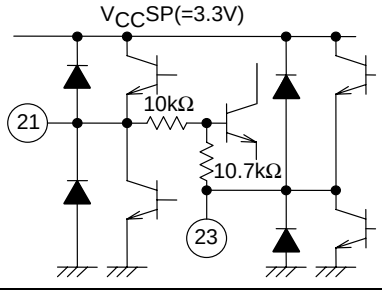
Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
9	V _{CCA}	3.0V		Power pin for analog signal part	
10	PB IN	1.64V	Reference input level =-15dBV Maximum input level = -5dBV In analog input mode = 3.465Vpp In $\Delta\Sigma$ input mode	PB input pin	
11	A GND	0V		GND pin for analog signal part	
12	REC OUT	1.50V	At PB reference input Output level = -15dBV	REC output pin	
13	ALC DET			ALC detection pin	
14	ALC IN	1.64V	At MIC reference input Output level = -49dBV Max input level =-10dBV	ALC input pin	
15	MIC OUT	1.6V	At MIC reference input Output level = -49dBV	MIC output pin	

Continued on next page.

LA74303FN

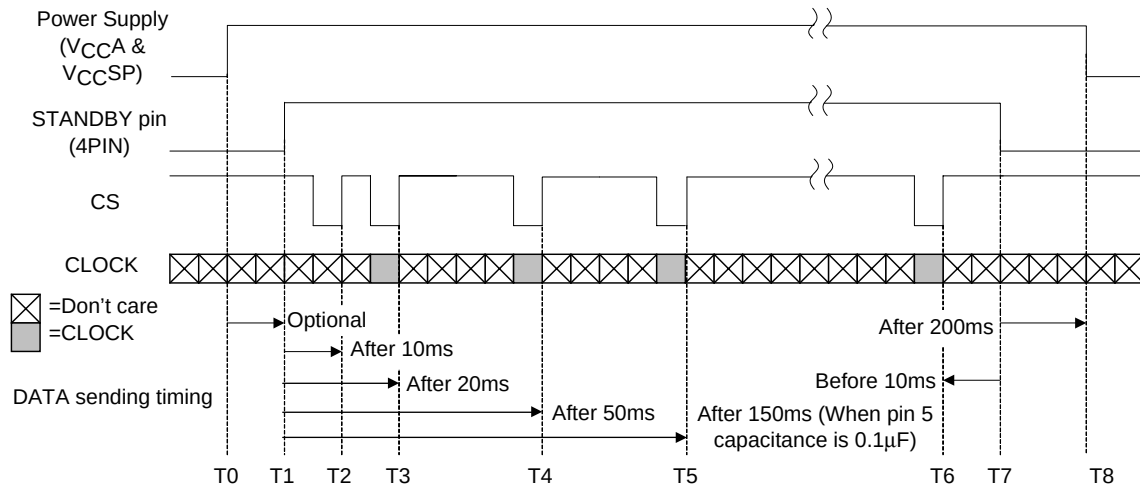
Continued from preceding page.

查询LA74303FN 供应商

Pin No.	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
16	MIC GND	0V		For MIC Amp blocking GND pin	
17	MIC IN	1.64V	Reference input level =-69dBV Maximum input level =-30dBV	MIC input pin	
18	MIC V _{CC}	2.30V		MIC power pin	
19	VREFL	2.30V		MIC V _{CC} and VREFL ripple rejection pin	
20 24	SP GND	0V		Speaker GND pin	
21	SPK OUT+	1.27V	At PB reference input Output level = -8dBV (EVR MAX)	Speaker positive-phase output pin	
22	V _{CC} SP	3.3V		Speaker power pin	

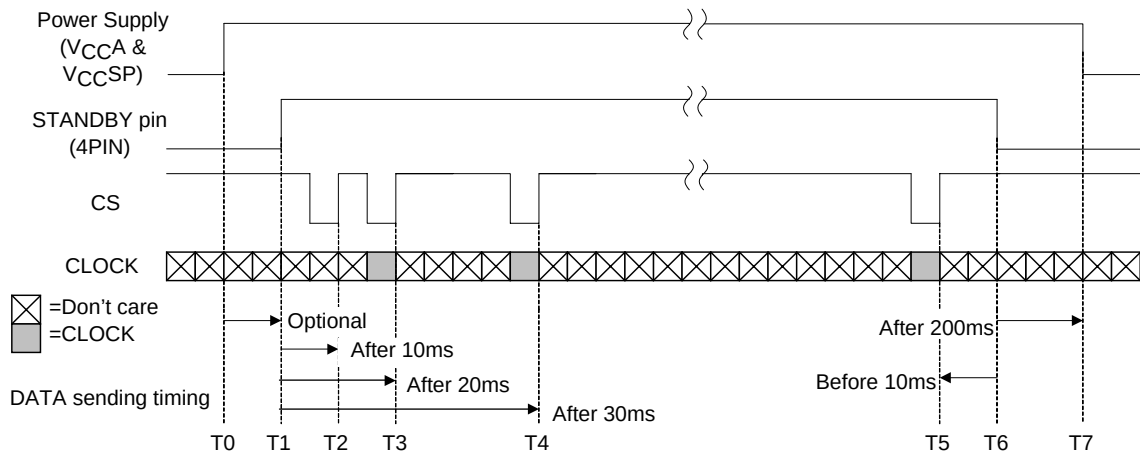
POP Sound Avoiding Sequence

① Upon STANDBY cancellation & control (PBMODE)

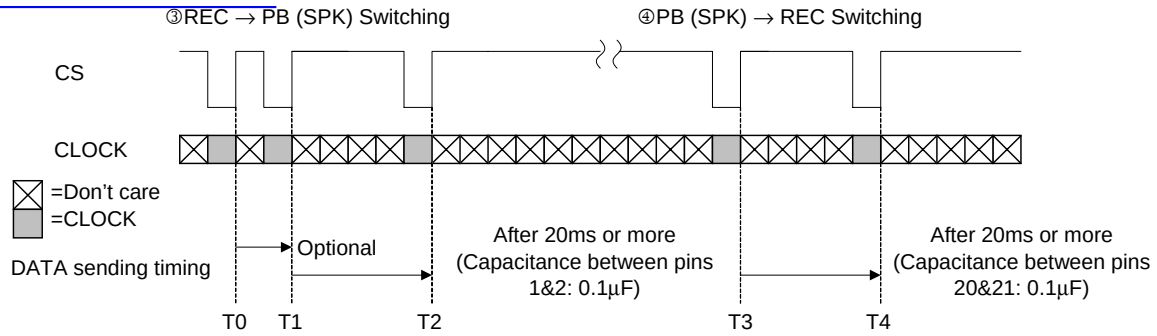


Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW (1, *): REC		REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog		0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital		1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON
T1	Standby cancellation (3.3 V applied to pin 4)	DATA unnecessary															
T2	Dummy communication (only CS)																
T3	VREF charging circuit: OFF	0	0/1	1	1	1	0	0/1	1	1	0	1	0	0	0	0	0
T4	Speaker AMP: ON	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	0
T5	Line AMP: ON	0	0/1	1	1	1	0	0/1	1	0	1	0	0	0	0	0	0
T6	Return to the initial state	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
T7	Standby control (0 V applied to pin 4)	DATA unnecessary															

②Upon STANDBY cancellation & control (RECMODE)

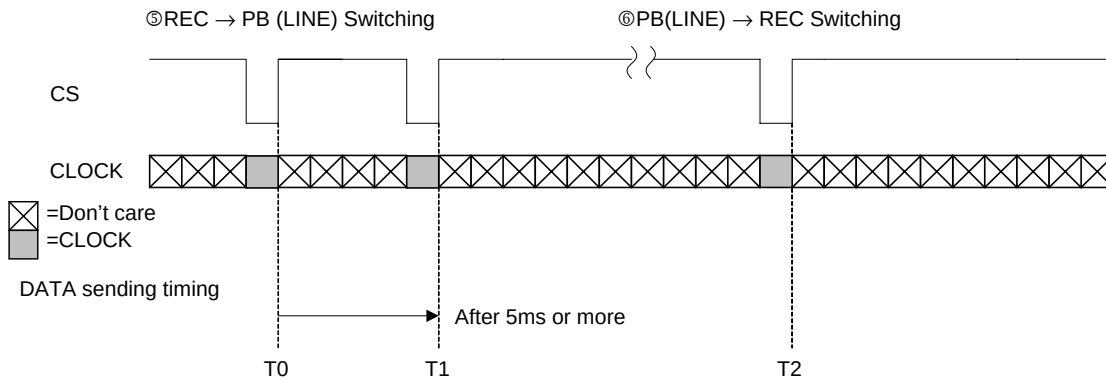


Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			LPF	CHRG	MIC	ALC	LPF MODESW	REC	LINE	LINE	SPK	EVR1	EVR2	EVR4	EVR8	EVR16	
		DMY	C SW	P SW	P SW	P SW	(1, *): REC	P SW	P SW	MUTE	P SW	DATA	DATA	DATA	DATA	DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
	*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON		
T1	Standby cancellation (3.3 V applied to pin 4)	DATA unnecessary															
T2	Dummy communication (only CS)																
T3	Charging circuit & ALC: OFF, LPF: REC	0	0/1	1	0	1	1	0	0	1	0	1	0	0	0	0	
T4	ALC: ON	0	0/1	1	0	0	1	0	0	1	0	1	0	0	0	0	
T5	Return to the initial state	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	
T6	Standby control (0 V applied to pin 4)	DATA unnecessary															



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW (1, *): REC	REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON	
T0	Speaker AMP: OFF	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0
T1	PBMODE: switching EVR: setting	0	0/1	1	1	1	0	0/1	1	1	0	1	a	a	a	a	a
T2	Speaker AMP: ON	0	0/1	1	1	1	0	0/1	1	1	0	0	a	a	a	a	a
T3	RECMODE: switching EVR: MUTE Speaker AMP: OFF	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0
T4	Speaker AMP: ON	0	0/1	1	0	0	1	0/1	0	1	0	0	0	0	0	0	0

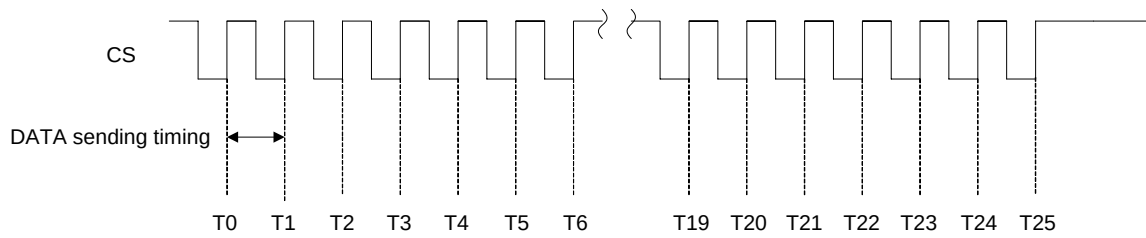
Note) a=EVR in user setting.



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		DMY	LPF C SW	CHRG P SW	MIC P SW	ALC P SW	LPF MODESW (1, *): REC	REC P SW	LINE P SW	LINE MUTE	SPK P SW	EVR1 DATA	EVR2 DATA	EVR4 DATA	EVR8 DATA	EVR16 DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
		*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON	
T0	PBMODE: switching	0	0/1	1	1	1	0	0/1	1	1	0	1	0	0	0	0	0
T1	Line AMP: ON Line MUTE: OFF	0	0/1	1	1	1	0	0/1	1	0	1	1	0	0	0	0	0
T2	RECMODE: switching Line AMP: ON Line MUTE: OFF	0	0/1	1	0	0	1	0/1	0	1	0	1	0	0	0	0	0

[查询"LA74303FN"供应商](#)

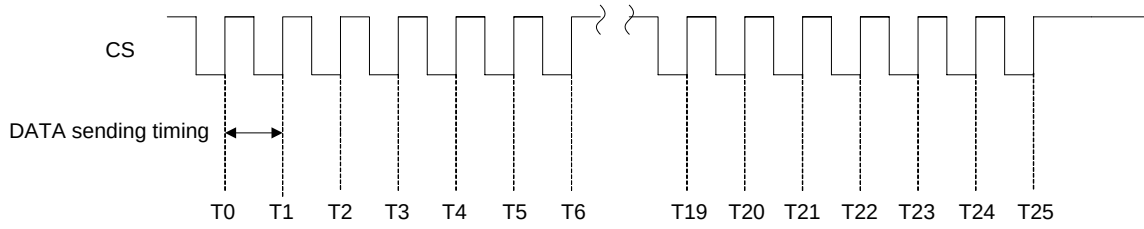
⑦EVR Switching (min → max) 0.25ms/CS



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			LPF	CHRG	MIC	ALC	LPF MODESW	REC	LINE	LINE	SPK	EVR1	EVR2	EVR4	EVR8	EVR16	
		DMY	C SW	P SW	P SW	P SW	(1, *): REC	P SW	P SW	MUTE	P SW	DATA	DATA	DATA	DATA	DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
	*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON		
T0	EVRDATA=0	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	
T1	EVRDATA=7	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	0
T2	EVRDATA=8	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	0
T3	EVRDATA=9	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	0
T4	EVRDATA=10	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	0
T5	EVRDATA=11	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	0
T6	EVRDATA=12	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	0
T7	EVRDATA=13	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	0
T8	EVRDATA=14	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	0
T9	EVRDATA=15	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	0
T10	EVRDATA=16	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	1
T11	EVRDATA=17	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	0	1
T12	EVRDATA=18	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	0	1
T13	EVRDATA=19	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	0	1
T14	EVRDATA=20	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	0	1
T15	EVRDATA=21	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	0	1
T16	EVRDATA=22	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	0	1
T17	EVRDATA=23	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	1
T18	EVRDATA=24	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	1
T19	EVRDATA=25	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	1
T20	EVRDATA=26	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	1
T21	EVRDATA=27	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	1
T22	EVRDATA=28	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	1
T23	EVRDATA=29	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	1
T24	EVRDATA=30	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	1
T25	EVRDATA=31	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	1

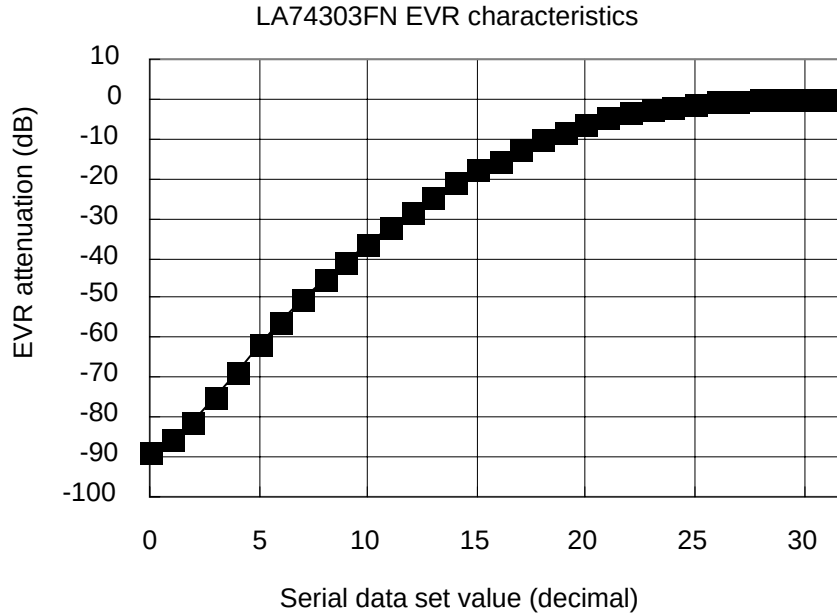
Note) DATA1 to 6 are the mute area of EVR characteristics and jumped due to no generation of POP noise.

⑧EVR Switching (max → min) 0.25ms/CS



Timing	Communication content	Recommended serial control settings															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			LPF	CHRG	MIC	ALC	LPF MODESW	REC	LINE	LINE	SPK	EVR1	EVR2	EVR4	EVR8	EVR16	
		DMY	C SW	P SW	P SW	P SW	(1, *): REC	P SW	P SW	MUTE	P SW	DATA	DATA	DATA	DATA	DATA	
		*	0:11kHz	0:ON	0:ON	0:ON	(0, 0): PB Analog	0:ON	0:ON	0:ON	0:ON	0:OFF	0:OFF	0:OFF	0:OFF	0:OFF	
	*	1:4kHz	1:OFF	1:OFF	1:OFF	(0, 1): PB Digital	1:OFF	1:OFF	1:OFF	1:OFF	1:ON	1:ON	1:ON	1:ON	1:ON		
T0	EVRDATA=31	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	1
T1	EVRDATA=30	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	1
T2	EVRDATA=29	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	1
T3	EVRDATA=28	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	1
T4	EVRDATA=27	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	1
T5	EVRDATA=26	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	1
T6	EVRDATA=25	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	1
T7	EVRDATA=24	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	1
T8	EVRDATA=23	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	1
T9	EVRDATA=22	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	0	1
T10	EVRDATA=21	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	0	1
T11	EVRDATA=20	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	0	1
T12	EVRDATA=19	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	0	1
T13	EVRDATA=18	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	0	1
T14	EVRDATA=17	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	0	1
T15	EVRDATA=16	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	1
T16	EVRDATA=15	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	1	0
T17	EVRDATA=14	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	1	1	0
T18	EVRDATA=13	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	1	1	0
T19	EVRDATA=12	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	1	1	0
T20	EVRDATA=11	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	0	1	0
T21	EVRDATA=10	0	0/1	1	1	1	0	0/1	1	1	0	0	0	1	0	1	0
T22	EVRDATA=9	0	0/1	1	1	1	0	0/1	1	1	0	0	1	0	0	1	0
T23	EVRDATA=8	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	1	0
T24	EVRDATA=7	0	0/1	1	1	1	0	0/1	1	1	0	0	1	1	1	0	0
T25	EVRDATA=0	0	0/1	1	1	1	0	0/1	1	1	0	0	0	0	0	0	0

Note) DATA1 to 6 are the mute area of EVR characteristics and jumped due to no generation of POP noise.



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of May, 2008. Specifications and information herein are subject to change without notice.