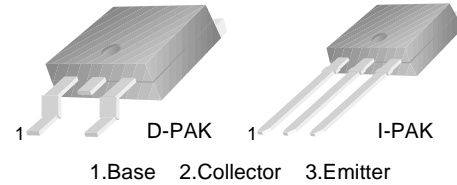




## KSH13003

### High Voltage Power Transistor D-PACK for Surface Mount Applications

- High speed Switching
- Suitable for Switching Regulator Motor Control
- Straight Lead (I.PACK, I Suffix)
- Lead Formed for Surface Mount Applications (No Suffix)



### NPN Epitaxial Silicon Transistor

#### Absolute Maximum Ratings $T_C=25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
$V_{CBO}$	Collector-Base Voltage	700	V
$V_{CEO}$	Collector-Emitter Voltage	400	V
$V_{EBO}$	Emitter-Base Voltage	9	V
$I_C$	Collector Current (DC)	1.5	A
$I_{CP}$	Collector Current (Pulse)	3	A
$I_B$	Base Current	0.75	A
$P_C$	Collector Dissipation ( $T_C=25^{\circ}\text{C}$ )	40	W
$T_J$	Junction Temperature	150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature	- 65 ~ 150	$^{\circ}\text{C}$

#### Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{CEO(sus)}$	* Collector-Emitter Breakdown Voltage	$I_C = 5\text{mA}, I_B = 0$	400			V
$I_{EBO}$	Emitter Cut-off Current	$V_{EB} = 9\text{V}, I_C = 0$			10	$\mu\text{A}$
$h_{FE}$	* DC Current Gain	$V_{CE} = 2\text{V}, I_C = 0.5\text{A}$ $V_{CE} = 2\text{V}, I_C = 1\text{A}$	8 5		40	
$V_{CE(sat)}$	* Collector-Emitter Saturation Voltage	$I_C = 0.5\text{A}, I_B = 0.1\text{A}$ $I_C = 1\text{A}, I_B = 0.25\text{A}$ $I_C = 1.5\text{A}, I_B = 0.5\text{A}$			0.5 1 3	V V V
$V_{BE(sat)}$	* Base-Emitter Saturation Voltage	$I_C = 0.5\text{A}, I_B = 0.1\text{A}$ $I_C = 1\text{A}, I_B = 0.25\text{A}$			1 1.2	V V
$C_{ob}$	Output Capacitance	$V_{CB} = 10\text{V}, f = 0.1\text{MHz}$		21		pF
$f_T$	Current Gain Bandwidth Product	$V_{CE} = 10\text{V}, I_C = 0.1\text{A}$	4			MHz
$t_{ON}$	Turn ON time	$V_{CC} = 125\text{V}, I_C = 1\text{A}$ $I_{B1} = 0.2\text{A}, I_{B2} = -0.2\text{A}$			1.1	$\mu\text{s}$
$t_{STG}$	Storage time				4.0	$\mu\text{s}$
$t_F$	Fall Time				0.7	$\mu\text{s}$

\* Pulse Test: Pulse Width=5ms, Duty Cycle≤10%

# Typical Characteristics

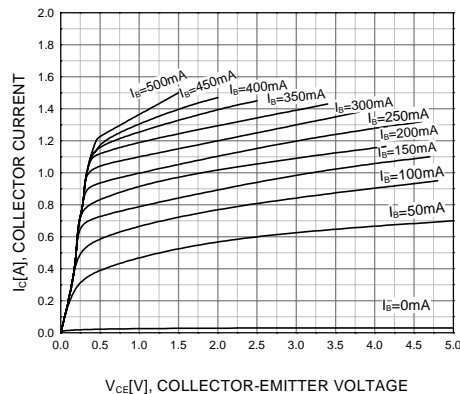


Figure 1. Static Characteristic

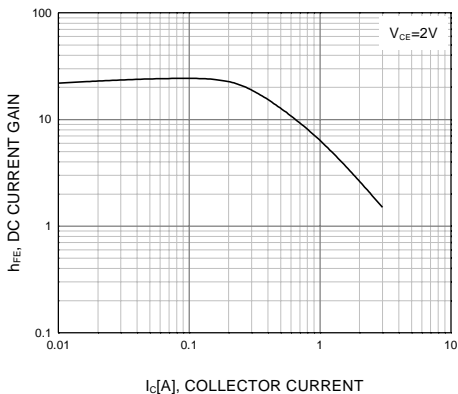


Figure 2. DC current Gain

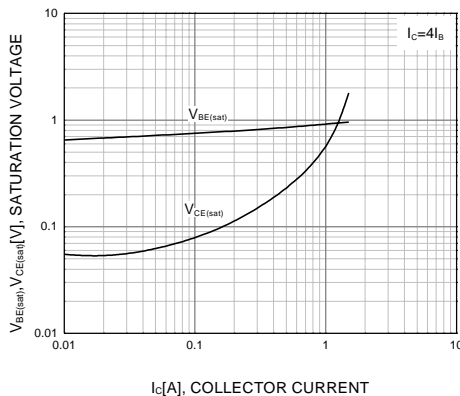


Figure 3. Base-Emitter Saturation Voltage  
Collector-Emitter Saturation Voltage

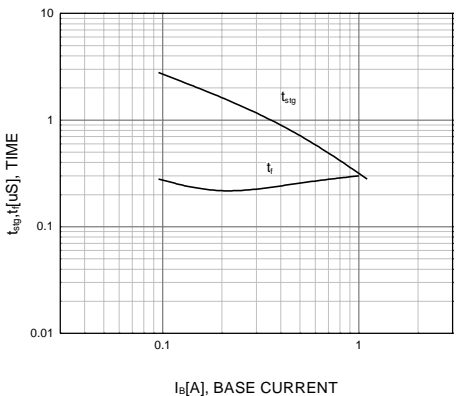


Figure 4. Switching Time

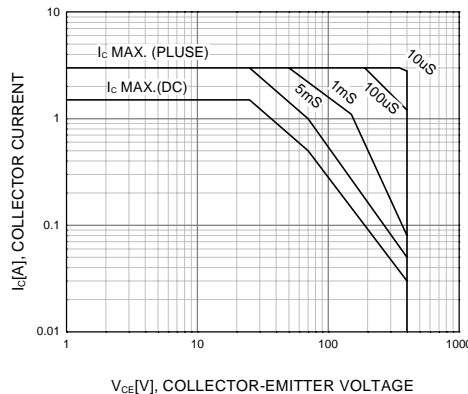


Figure 5. Safe Operating Area

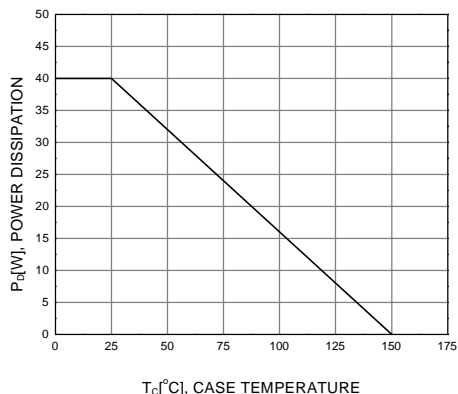
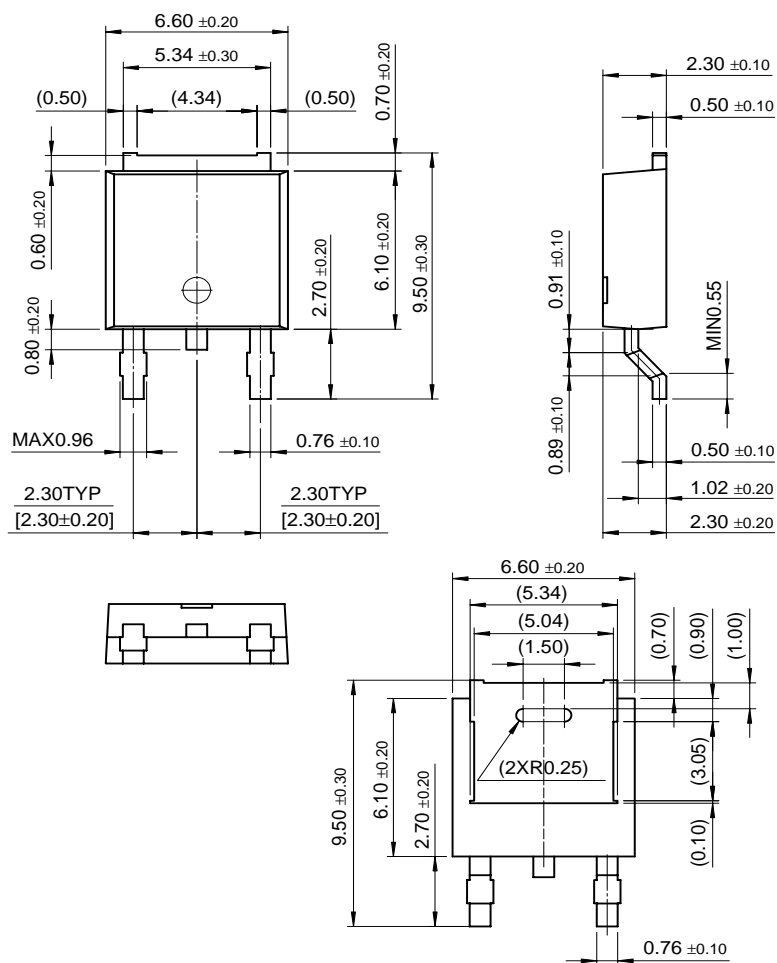


Figure 6. Power Derating

## D-PAK



Rev. A, February 2000

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