National Semiconductor

LM5100A/B/C
LM5101A/B/C

August 31, 2010

3A, 2A and 1A High Voltage High-Side and Low-Side Gate Drivers

General Description

The LM5100A/B/C and LM5101A/B/C High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (LM5100A/B/C) or TTL input thresholds (LM5101A/B/C). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, PSOP-8 pin and the LLP-10 pin packages. The LM5100C and LM5101C are also available in eMSOP-8 package. The LM5101A is also available in LLP-8 pin package.

Features

- Drives both a high-side and low-side N-Channel MOSFETs
- Independent high and low driver logic inputs
- Bootstrap supply voltage up to 118V DC
- Fast propagation times (25 ns typical)
- Drives 1000 pF load with 8 ns rise and fall times
- Excellent propagation delay matching (3 ns typical)
- Supply rail under-voltage lockout
- Low power consumption
- Pin compatible with HIP2100/HIP2101

Typical Applications

- Current Fed push-pull converters
- Half and Full Bridge power converters
- Synchronous buck converters
- Two switch forward power converters
- Forward with Active Clamp converters

Package

- SOIC-8
- PSOP-8
- LLP-8 (4 mm x 4 mm)
- LLP-10 (4 mm x 4 mm)
- eMSOP-8

Simplified Block Diagram

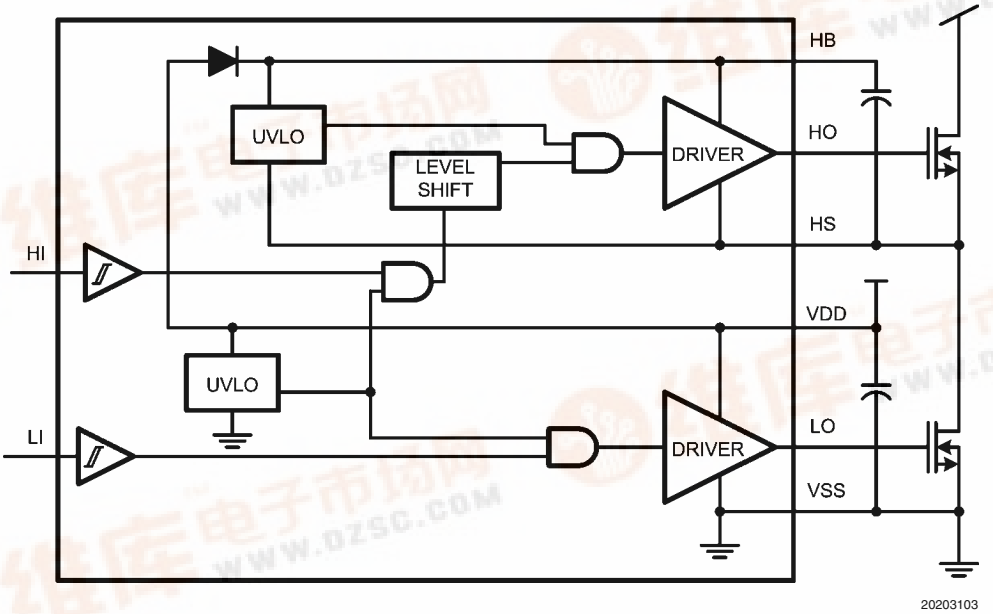
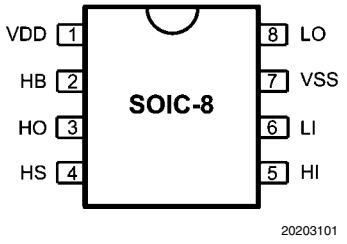


FIGURE 1.

Input/Output Options

Part Number	Input Thresholds	Peak Output Current
LM5100A	CMOS	3A
LM5101A	TTL	3A
LM5100B	CMOS	2A
LM5101B	TTL	2A
LM5100C	CMOS	1A
LM5101C	TTL	1A

Connection Diagrams



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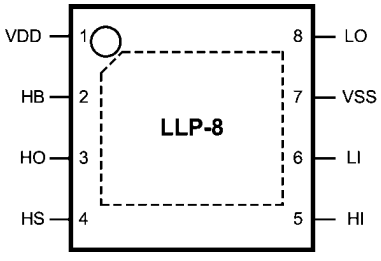

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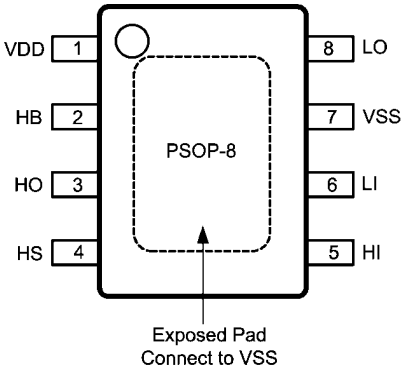

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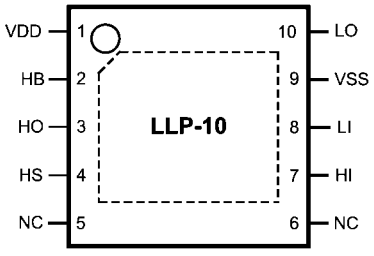

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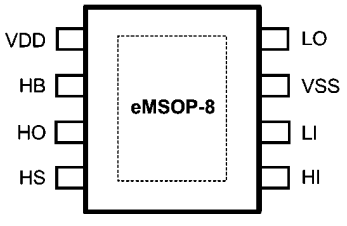

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Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5100A/LM5101AM	SOIC 8	M08A	95 units shipped in anti static rails
LM5100A/LM5101AMX	SOIC 8	M08A	2500 shipped in Tape & Reel
LM5100A/LM5101AMR	PSOP 8	MRA08A	95 units shipped in anti static rails
LM5100A/LM5101AMRX	PSOP 8	MRA08A	2500 shipped in Tape & Reel
LM5100A /LM5101ASD	LLP 10	SDC10A	1000 shipped in Tape & Reel
LM5100A/LM5101ASDX	LLP 10	SDC10A	4500 shipped in Tape & Reel
LM5100B/LM5101BMA	SOIC 8	M08A	95 units shipped in anti static rails
LM5100B/LM5101BMAX	SOIC 8	M08A	2500 shipped in Tape & Reel
LM5100B/LM5101BSD	LLP 10	SDC10A	1000 shipped in Tape & Reel
LM5100B/LM5101BSDX	LLP 10	SDC10A	4500 shipped in Tape & Reel
LM5100C/LM5101CMA	SOIC 8	M08A	95 units shipped in anti static rails
LM5100C/LM5101CMAX	SOIC 8	M08A	2500 shipped in Tape & Reel
LM5100C /LM5101CSD	LLP 10	SDC10A	1000 shipped in Tape & Reel
LM5100C/LM5101CSDX	LLP 10	SDC10A	4500 shipped in Tape & Reel
LM5100C/LM5101CMYE	eMSOP-8	MUY08A	250 shipped in Tape & Reel
LM5100C/LM5101CMY	eMSOP-8	MUY08A	1000 shipped in Tape & Reel
LM5100C/LM5101CMYX	eMSOP-8	MUY08A	3500 shipped in Tape & Reel
LM5101ASD-1	LLP 8	SDC08A	1000 shipped in Tape & Reel
LM5101ASDX-1	LLP 8	SDC08A	4500 shipped in Tape & Reel

Pin Descriptions

Pin #					Name	Description	Application Information
SOIC-8	PSOP-8	LLP-8	LLP-10	eMSOP-8			
1	1	1	1	1	VDD	Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
2	2	2	2	2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
3	3	3	3	3	HO	High-side gate driver output	Connect to the gate of high-side MOSFET with a short, low inductance path.
4	4	4	4	4	HS	High-side MOSFET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
5	5	5	7	5	HI	High-side driver control input	The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
6	6	6	8	6	LI	Low-side driver control input	The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	7	7	9	7	VSS	Ground return	All signals are referenced to this ground.
8	8	8	10	8	LO	Low-side gate driver output	Connect to the gate of the low-side MOSFET with a short, low inductance path.
	EP	EP	EP	EP	EP (LLP and PSOP and eMSOP packages)		Solder to the ground plane under the IC to aid in heat dissipation.

Note: For LLP-8, LLP-10 and eMSOP-8 package, it is recommended that the exposed pad on the bottom of the package is soldered to ground plane on the PC board, and that ground plane should extend out from beneath the IC to help dissipate heat. For LLP-10 package, pins 5 and 6 have no connection.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VDD to VSS	−0.3V to +18V
HB to HS	−0.3V to +18V
LI or HI Input	−0.3V to V_{DD} +0.3V
LO Output	−0.3V to V_{DD} +0.3V
HO Output	V_{HS} −0.3V to V_{HB} +0.3V
HS to VSS (*Note 6*)	−5V to +100V
HB to VSS	118V
Junction Temperature	+150°C
Storage Temperature Range	−55°C to +150°C
ESD Rating HBM (*Note 2*)	2 kV

Recommended Operating Conditions

VDD	+9V to +14V
HS	−1V to 100V
HB	V_{HS} +8V to V_{HS} +14V
HS Slew Rate	< 50 V/ns
Junction Temperature	−40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO (*Note 4*).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current, LM5100A/B/C	LI = HI = 0V		0.1	**0.2**	mA
	VDD Quiescent Current, LM5101A/B/C	LI = HI = 0V		0.25	**0.4**	
I_{DDO}	VDD Operating Current	f = 500 kHz		2.0	**3**	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.06	**0.2**	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.6	**3**	mA
I_{HBS}	HB to VSS Current, Quiescent	HS = HB = 100V		0.1	**10**	µA
I_{HBSO}	HB to VSS Current, Operating	f = 500 kHz		0.4		mA
INPUT PINS						
V_{IL}	Input Voltage Threshold LM5100A/B/C	Rising Edge	**4.5**	5.4	**6.3**	V
V_{IL}	Input Voltage Threshold LM5101A/B/C	Rising Edge	**1.3**	1.8	**2.3**	V
V_{IHYS}	Input Voltage Hysteresis LM5100A/B/C			500		mV
V_{IHYS}	Input Voltage Hysteresis LM5101A/B/C			50		mV
R_I	Input Pulldown Resistance		**100**	200	**400**	kΩ
UNDER VOLTAGE PROTECTION						
V_{DDR}	VDD Rising Threshold		**6.0**	6.9	**7.4**	V
V_{DDH}	VDD Threshold Hysteresis			0.5		V
V_{HBR}	HB Rising Threshold		**5.7**	6.6	**7.1**	V
V_{HBH}	HB Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-Current Forward Voltage	I_{VDD-HB} = 100 µA		0.52	**0.85**	V
V_{DH}	High-Current Forward Voltage	I_{VDD-HB} = 100 mA		0.8	**1**	V
R_D	Dynamic Resistance LM5100A/B/C, LM5101A/B/C	I_{VDD-HB} = 100 mA		1.0	**1.65**	Ω
LO & HO GATE DRIVER						
V_{OL}	Low-Level Output Voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA		0.12	**0.25**	V
	Low-Level Output Voltage LM5100B/LM5101B			0.16	**0.4**	
	Low-Level Output Voltage LM5100C/LM5101C			0.28	**0.65**	
V_{OH}	High-Level Output Voltage LM5100A/LM5101A	I_{HO} = I_{LO} = 100 mA		0.24	**0.45**	V
	High-Level Output Voltage LM5100B/LM5101B	V_{OH} = VDD− LO or		0.28	**0.60**	
	High-Level Output Voltage LM5100C/LM5101C	V_{OH} = HB - HO		0.60	**1.10**	
I_{OHL}	Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		A
	Peak Pullup Current LM5100B/LM5101B			2		
	Peak Pullup Current LM5100C/LM5101C			1		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DLL}	Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		A
	Peak Pulldown Current LM5100B/LM5101B			2		
	Peak Pulldown Current LM5100C/LM5101C			1		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-8		170		°C/W
		LLP-8(*Note 3*)		40		
		LLP-10 (*Note 3*)		40		
		PSOP-8		40		
		eMSOP-8 (*Note 3*)		80		

Switching Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = V_{HB}$ = 12V, $V_{SS} = V_{HS}$ = 0V, No Load on LO or HO (*Note 4*).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	**45**	ns
	LO Turn-Off Propagation Delay LM5101A/B/C			22	**56**	
t_{LPLH}	LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	**45**	ns
	LO Turn-On Propagation Delay LM5101A/B/C			26	**56**	
t_{HPHL}	HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	**45**	ns
	HO Turn-Off Propagation Delay LM5101A/B/C			22	**56**	
t_{HPLH}	LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	**45**	ns
	LO Turn-On Propagation Delay LM5101A/B/C			26	**56**	
t_{MON}	Delay Matching: LO on & HO off LM5100A/B/C			1	**10**	ns
	Delay Matching: LO on & HO off LM5101A/B/C			4	**10**	
t_{MOFF}	Delay Matching: LO off & HO on LM5100A/B/C			1	**10**	ns
	Delay Matching: LO on & HO off LM5101A/B/C			4	**10**	
t_{RC}, t_{FC}	Either Output Rise/Fall Time	C_L = 1000 pF		8		ns
t_R	Output Rise Time (3V to 9V) LM5100A/ LM5101A	C_L = 0.1 µF		430		ns
	Output Rise Time (3V to 9V) LM5100B/ LM5101B			570		
	Output Rise Time (3V to 9V) LM5100C/ LM5101C			990		
t_F	Output Fall Time (3V to 9V) LM5100A/ LM5101A	C_L = 0.1 µF		260		ns
	Output Fall Time (3V to 9V) LM5100B/ LM5101B			430		
	Output Fall Time (3V to 9V) LM5100C/ LM5101C			715		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Reverse Recovery Time	I_F = 100 mA, I_R = 100 mA		37		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000V for HBM and 100V for MM.

Note 3: 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

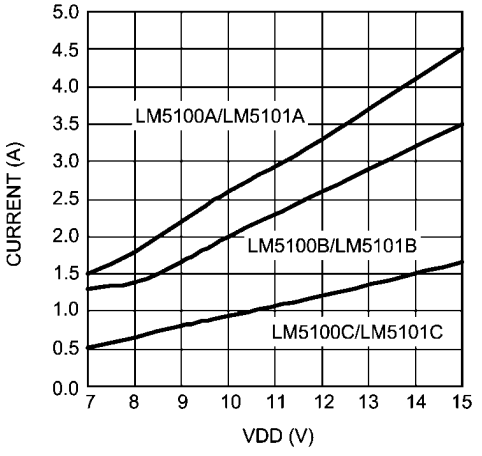
Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating environment.

Note 6: In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed -1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VDD-15V. For example if VDD = 10V, the negative transients at HS must not exceed -5V.

Typical Performance Characteristics

Peak Sourcing Current vs VDD



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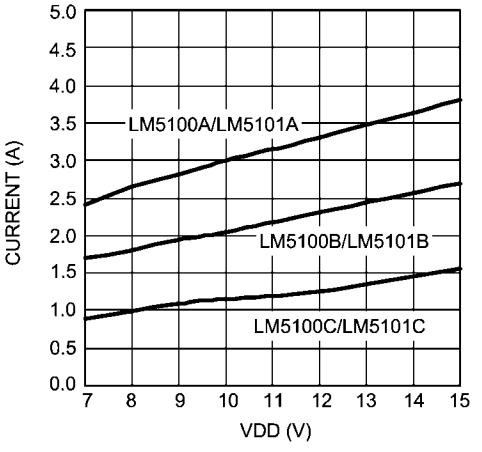
Peak Sinking Current vs VDD



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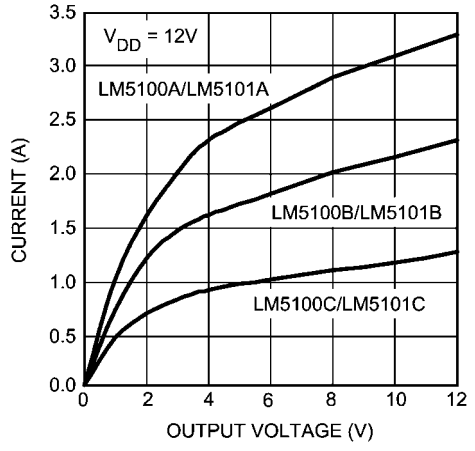
Sink Current vs Output Voltage



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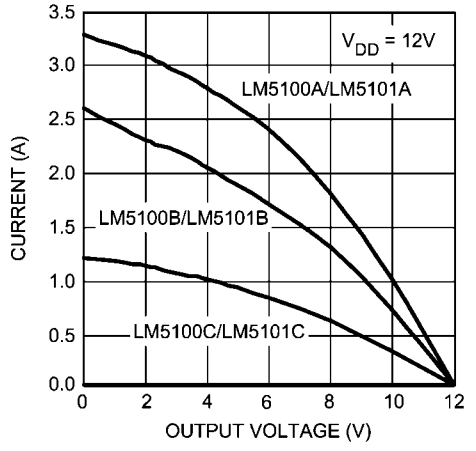
Source Current vs Output Voltage



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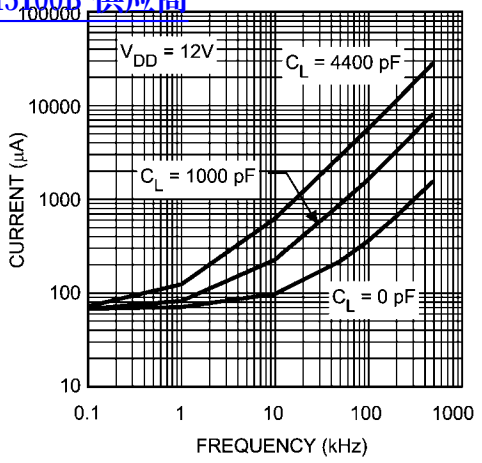
LM5100A/B/C I_{DD} vs Frequency



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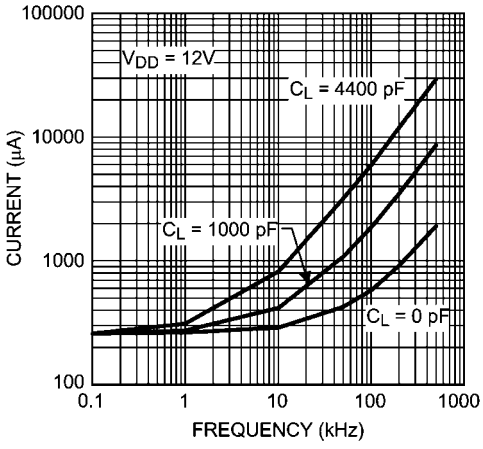
LM5101A/B/C I_{DD} vs Frequency



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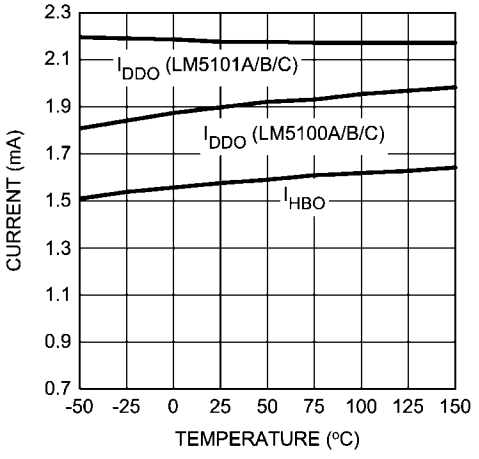
Operating Current vs Temperature



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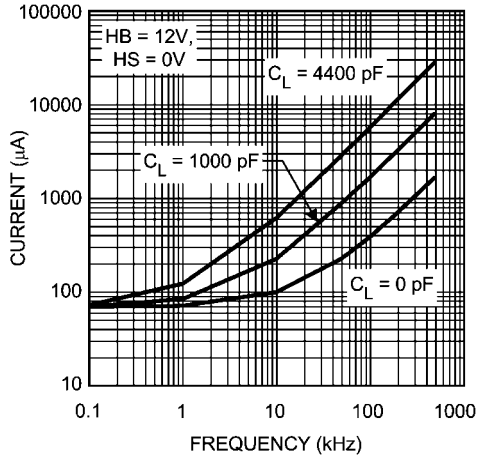
I_{HB} vs Frequency



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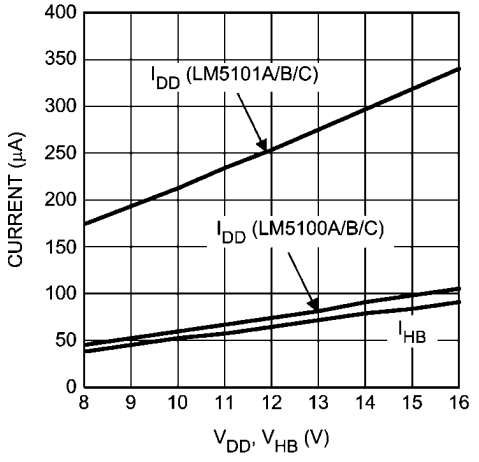
Quiescent Current vs Supply Voltage



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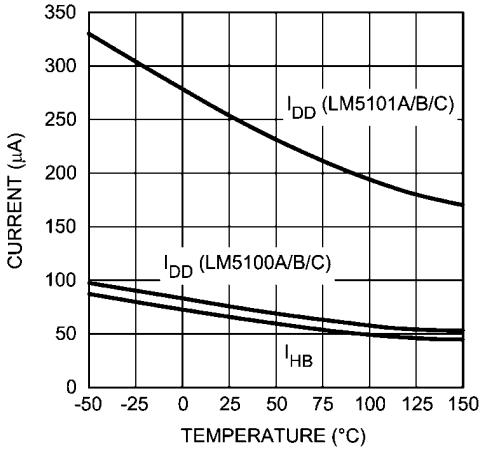
Quiescent Current vs Temperature



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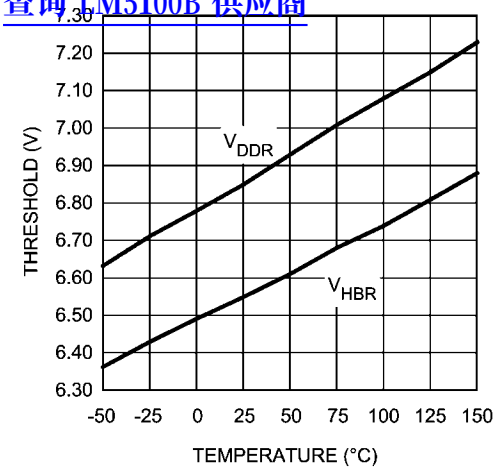
Undervoltage Rising Thresholds vs Temperature



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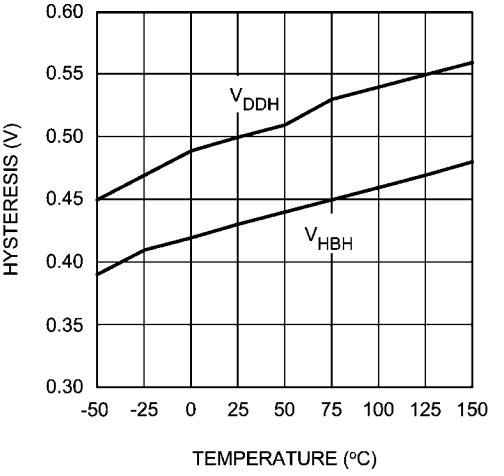
Undervoltage Threshold Hysteresis vs Temperature



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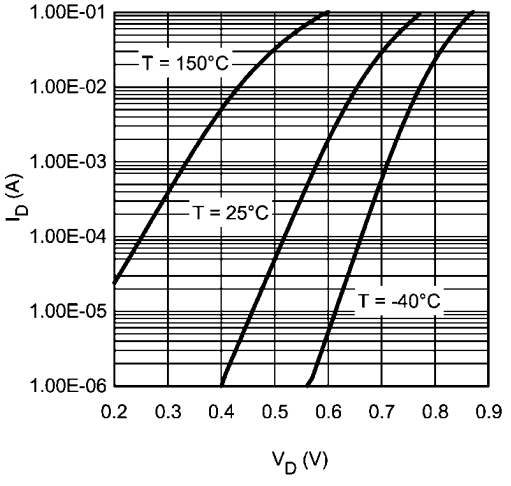
Bootstrap Diode Forward Voltage



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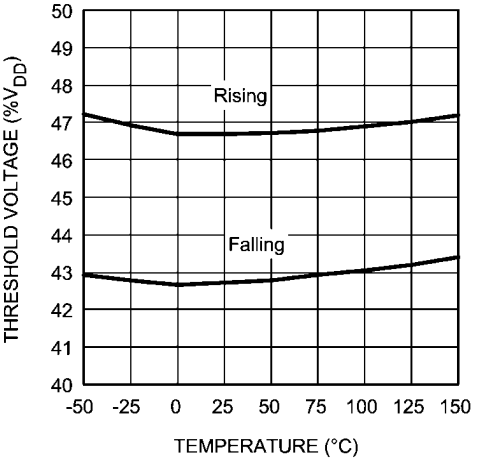
LM5100A/B/C Input Threshold vs Temperature



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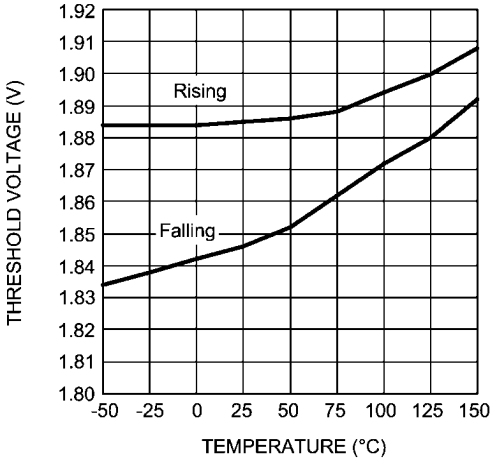
LM5101A/B/C Input Threshold vs Temperature



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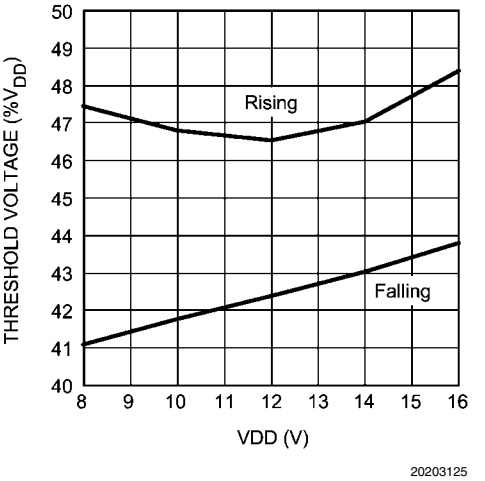
LM5100A/B/C Input Threshold vs VDD



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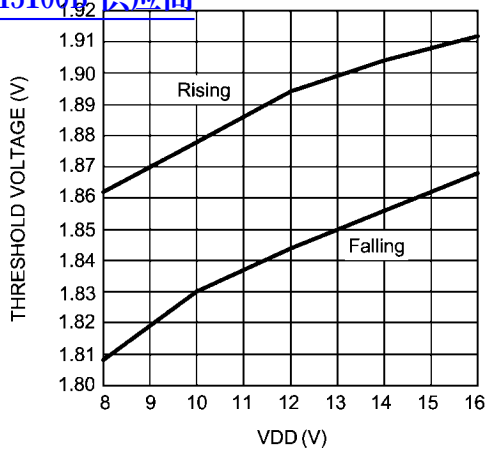
LM5101A/B/C Input Threshold vs VDD



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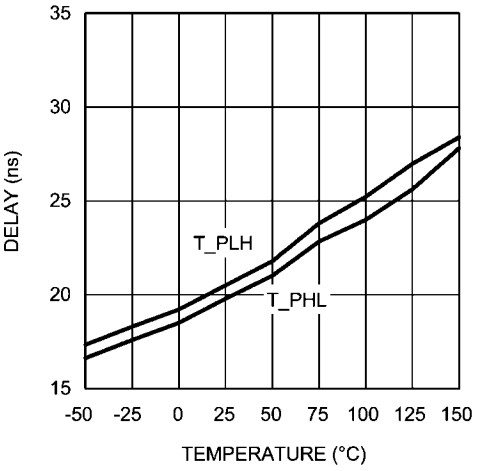
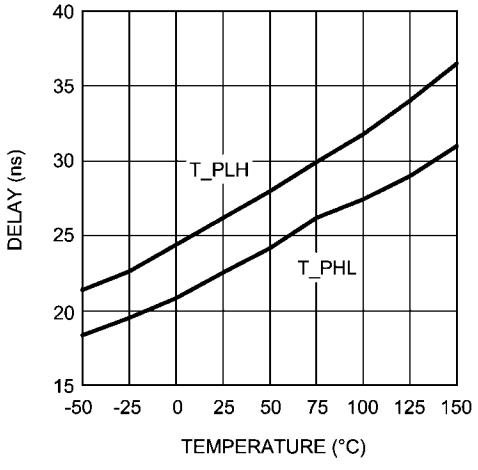
LM5100A/B/C Propagation Delay vs Temperature



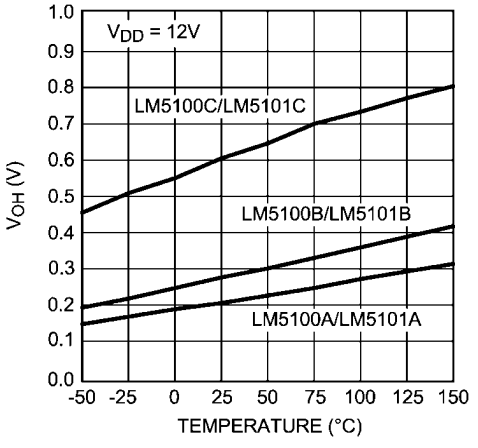
20203112

LM5101A/B/C Propagation Delay vs Temperature



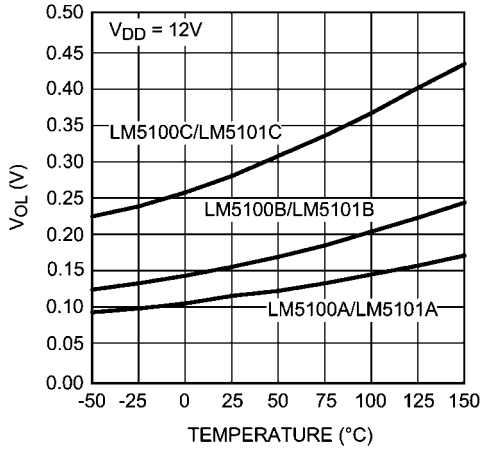
20203113

LO & HO Gate Drive - High Level Output Voltage vs Temperature



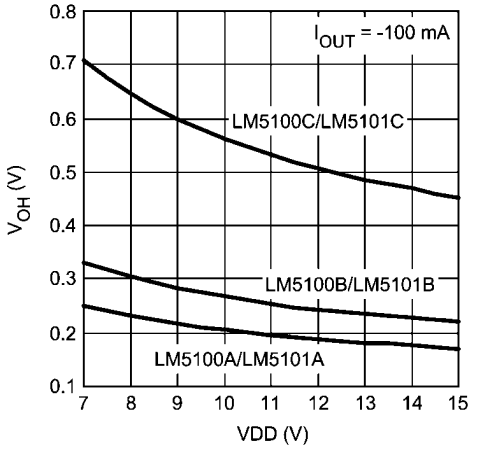
20203120

LO & HO Gate Drive - Low Level Output Voltage vs Temperature



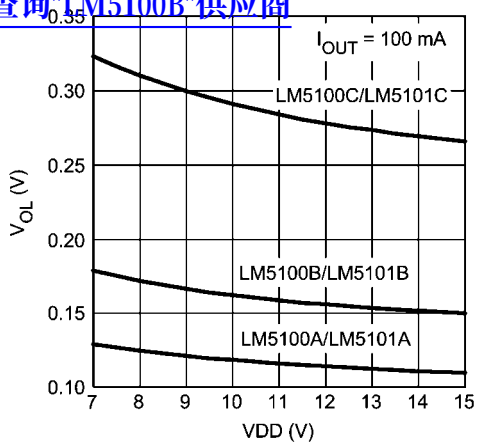
20203121

LO & HO Gate Drive - Output High Voltage vs VDD



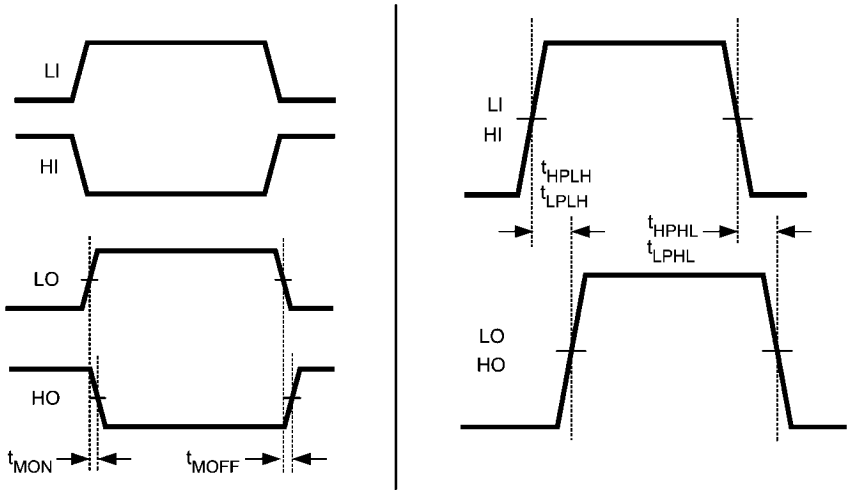
20203131

LO & HO Gate Drive - Output Low Voltage vs VDD



20203132

Timing Diagram



20203104

FIGURE 2.

Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

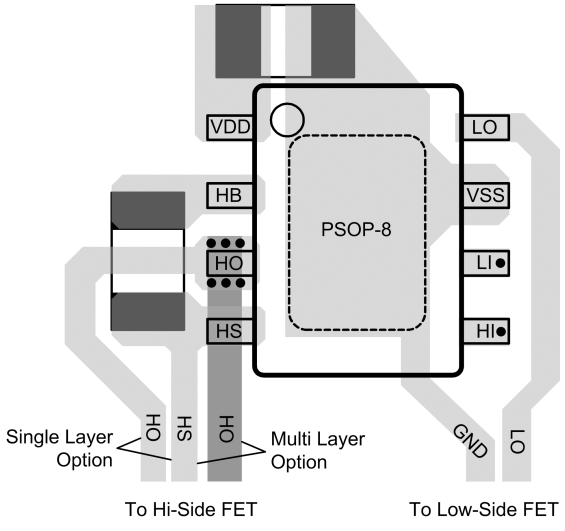
1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:

   a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.

   b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in the following figure. If possible a single layer placement is preferred.

Recommended Layout for Driver IC and Passives



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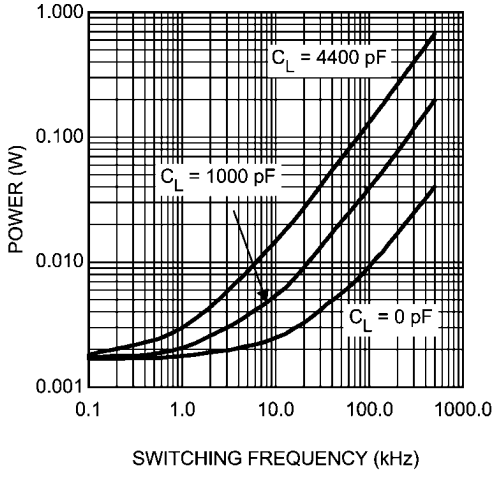
Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (VDD) and can be roughly calculated as:

$$P_{DGATES} = 2 \bullet f \bullet C_L \bullet V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

Gate Driver Power Dissipation (LO + HO)
V_{DD} = 12V, Neglecting Diode Losses

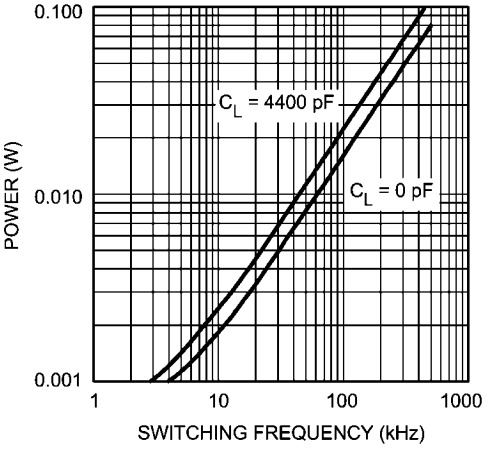


20203105

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation.

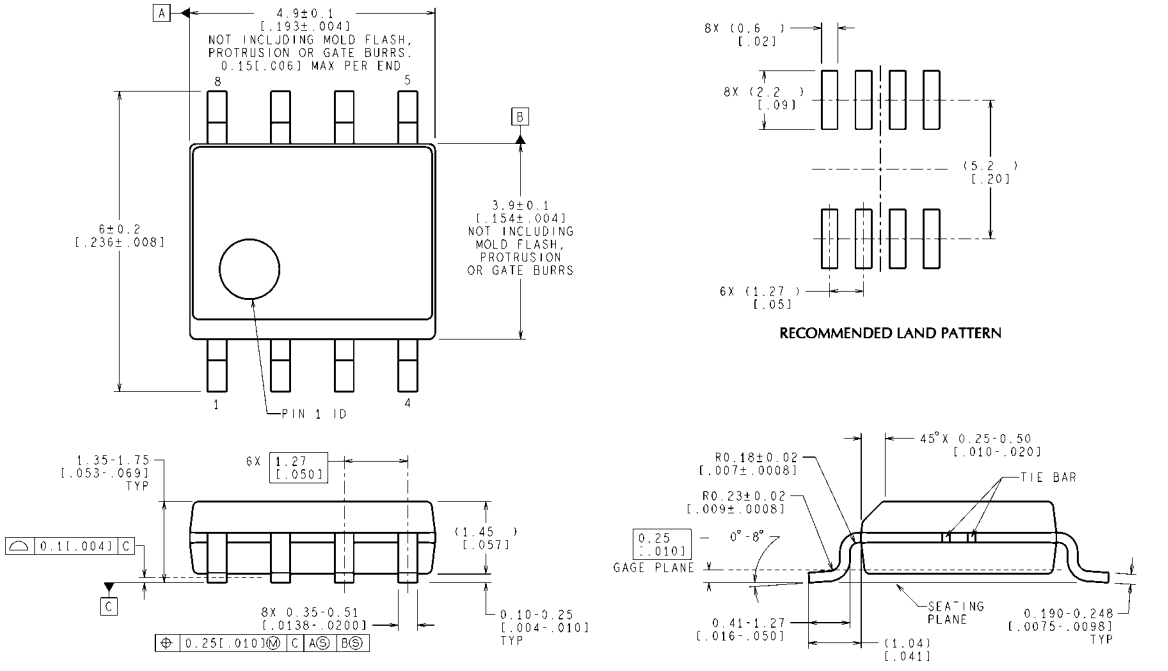
The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

Diode Power Dissipation V_{IN} = 50V



20203106

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

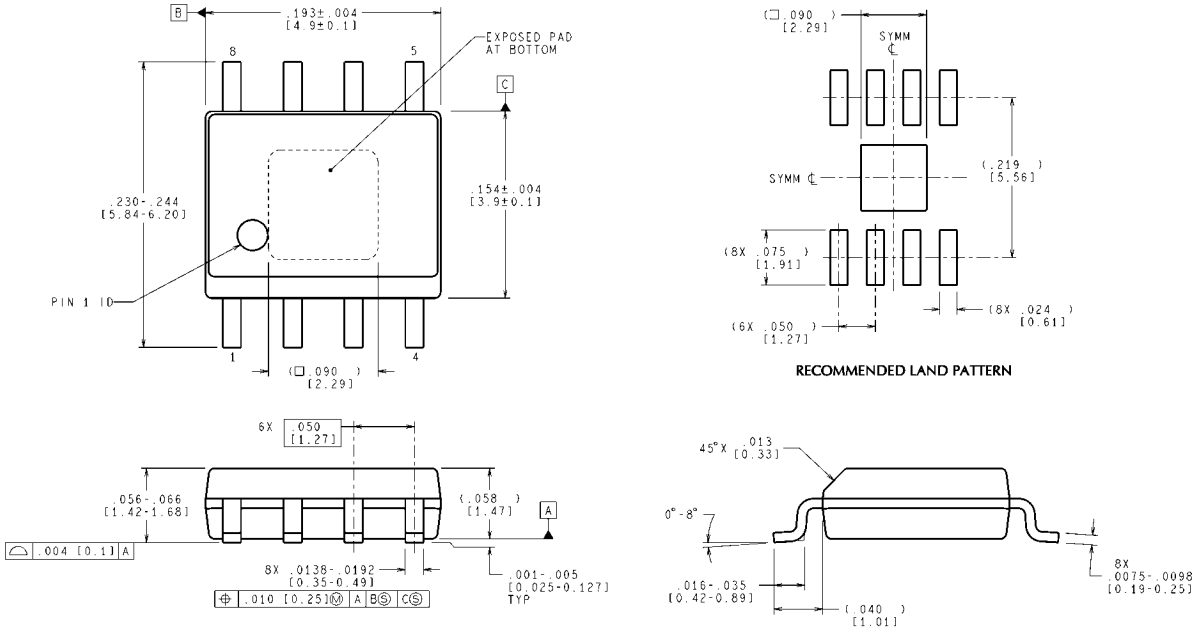
M08A (Rev M)

Controlling dimension is inch. Values in [ ] are millimeters.

Notes: Unless otherwise specified.

1. Standard lead finish to be 200 microinches/5.08 micrometers minimum lead/tin (solder) on copper.
2. Dimension does not include mold flash.
3. Reference JEDEC registration MS-012, Variation AA, dated May 1990.

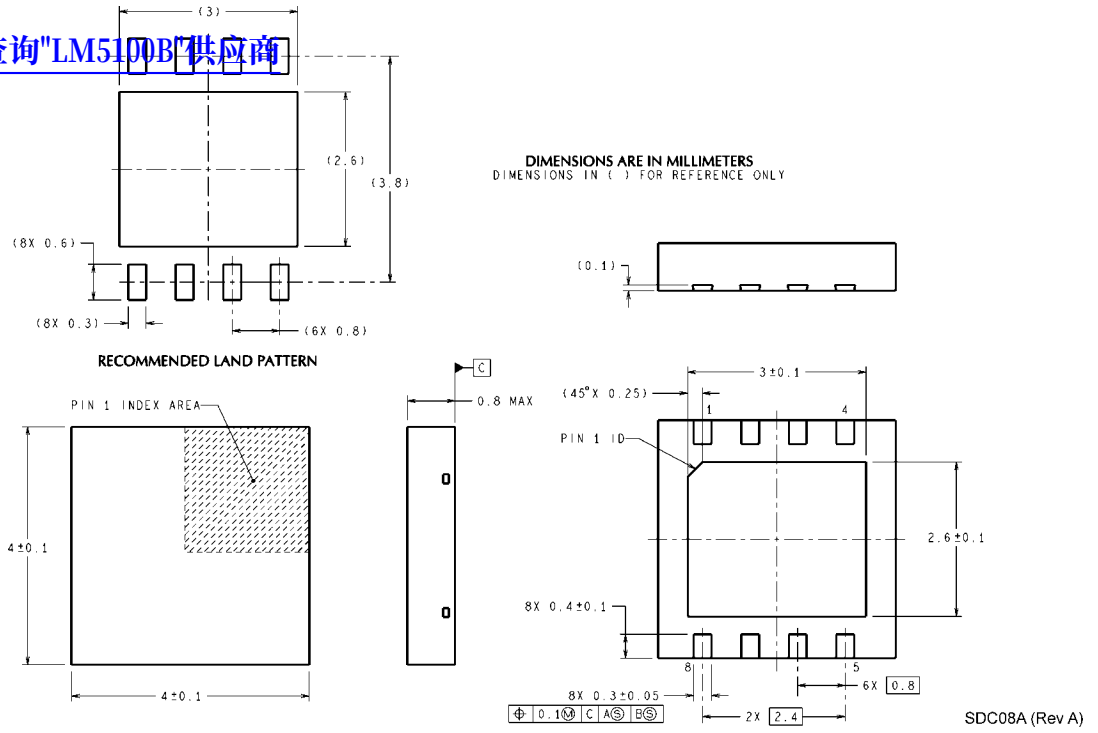
SOIC-8 Outline Drawing
NS Package Number M08A



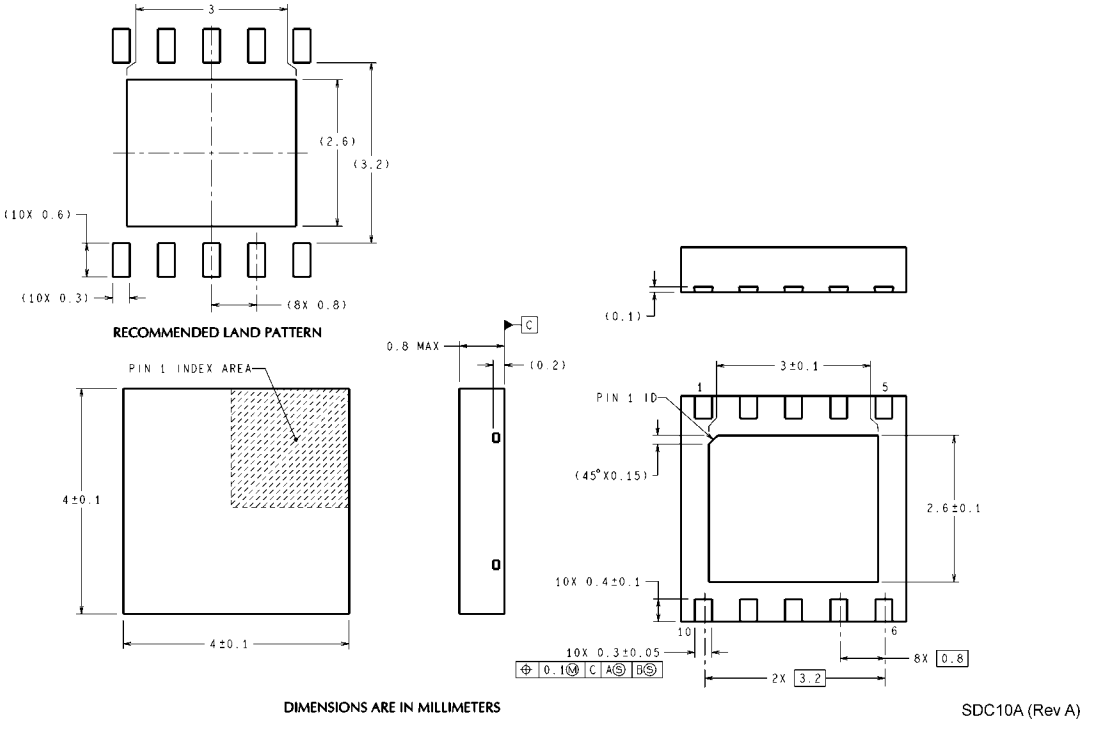
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MRA08A (Rev D)

PSOP-8 Outline Drawing
NS Package Number MRA08A



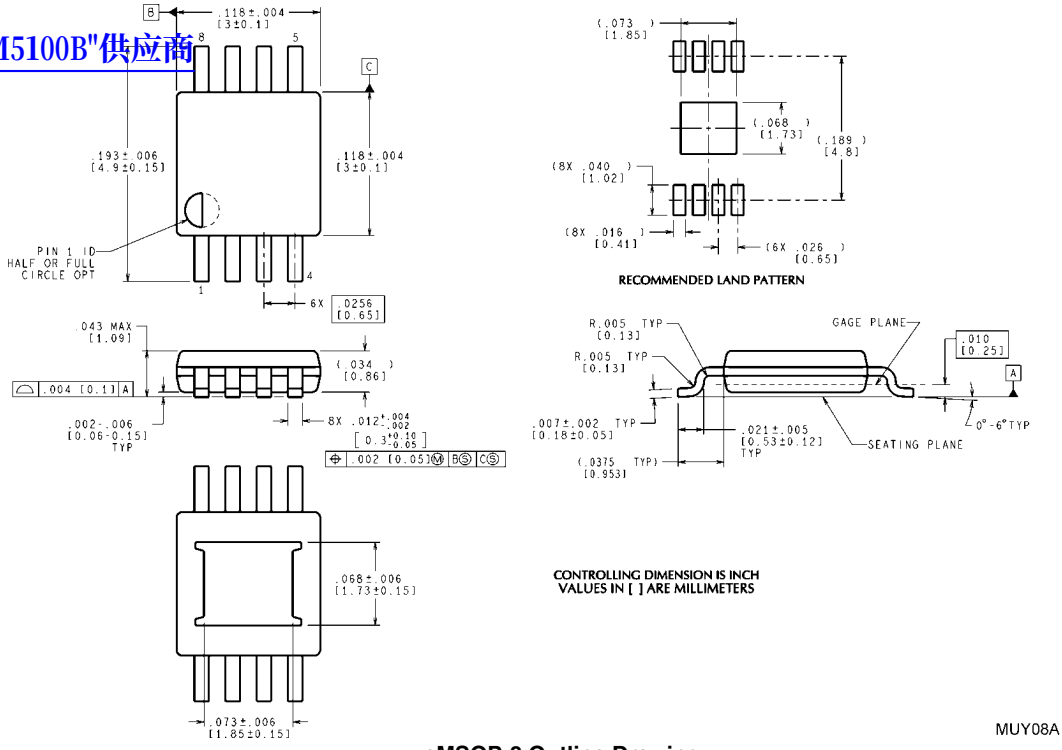
LLP-8 Outline Drawing
NS Package Number SDC08A



Notes: Unless otherwise specified.

1. For solder thickness and composition, see “Solder Information” in the packaging section of the National Semiconductor web page (www.national.com).
2. Maximum allowable metal burr on lead tips at the package edges is 76 microns.
3. No JEDEC registration as of May 2003.

LLP-10 Outline Drawing
NS Package Number SDC10A



MUY08A (Rev A)

eMSOP-8 Outline Drawing
NS Package Number MUY08A

Notes

Notes

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