



T-31-25

2050

N-Channel Junction Silicon FET

High-Frequency Low-Noise Amp Applications

©2840

Features

- Adoption of FBET process
- Large $|y_{fs}|$
- Small c_{iss}
- Very low noise figure
- Very small-sized package permitting 2SK931-applied sets to be made smaller and slimmer

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

			unit
Drain to Source Voltage	V_{DSX}	30	V
Gate to Drain Voltage	V_{GDS}	-30	V
Gate Current	I_G	10	mA
Drain Current	I_D	50	mA
Allowable Power Dissipation	P_D	200	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a = 25^\circ\text{C}$

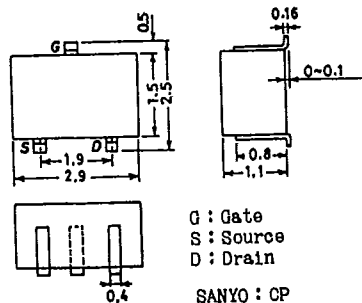
			min	typ	max	unit
Gate to Drain Breakdown Voltage	$V_{(BR)GDS}$	$I_G = -10\mu\text{A}, V_{DS} = 0\text{V}$	-30			V
Gate Cutoff Current	I_{GSS}	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}$			-1.0	nA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 5\text{V}, I_D = 100\mu\text{A}$	-0.3	-0.8	-2.0	V
Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	≈ 5.0		≈ 30.0	mA
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}, f = 1\text{kHz}$	15	30		mS
Input Capacitance	c_{iss}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		7.0		pF
Reverse Transfer Capacitance	c_{rss}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2.0		pF
Noise Figure	NF	$V_{DS} = 5\text{V}, R_g = 1\text{k}\Omega, I_D = 1\text{mA}, f = 1\text{kHz}$	1.5			dB

※ : The 2SK931 is classified by I_{DSS} as follows (unit : mA) :

5.0	21	8.5	7.3	22	12.0	10.0	23	17.0	14.5	24	24.0	18.0	25	30.0
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(Note) Marking : D
 I_{DSS} rank : 21,22,23,24,25

Case Outline 2050
(unit : mm)

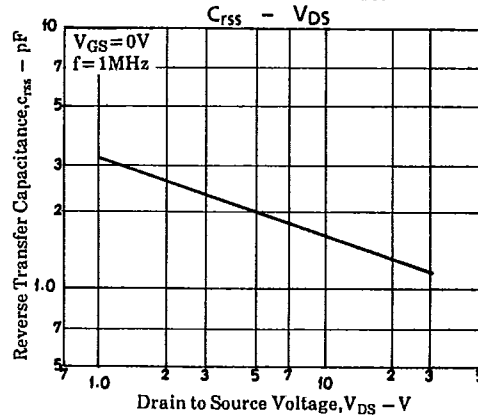
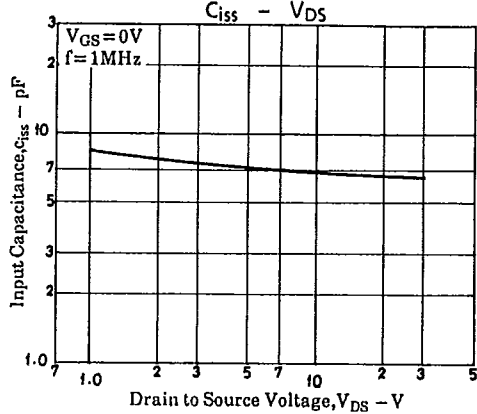
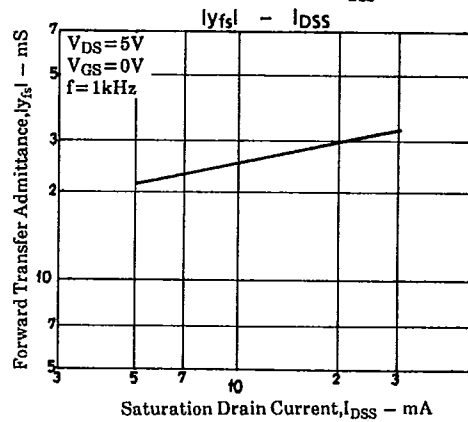
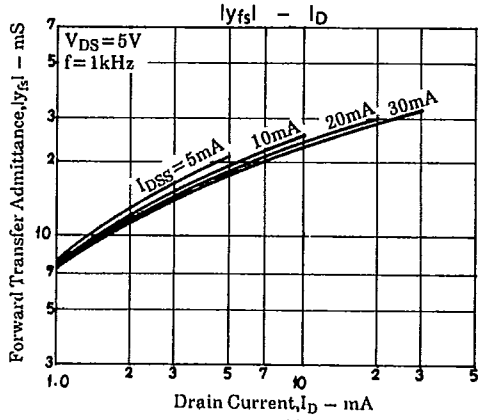
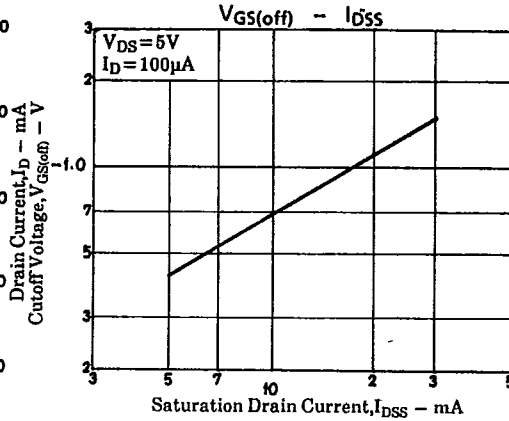
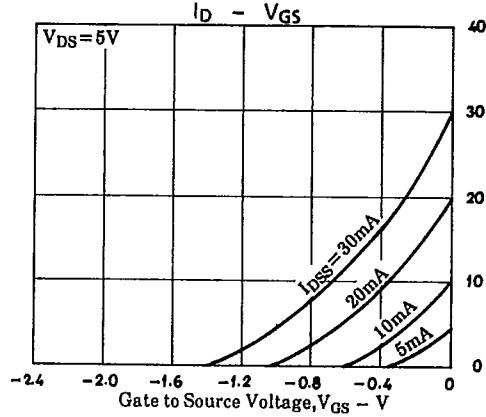
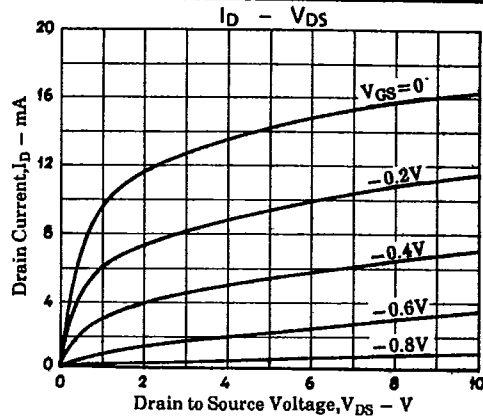
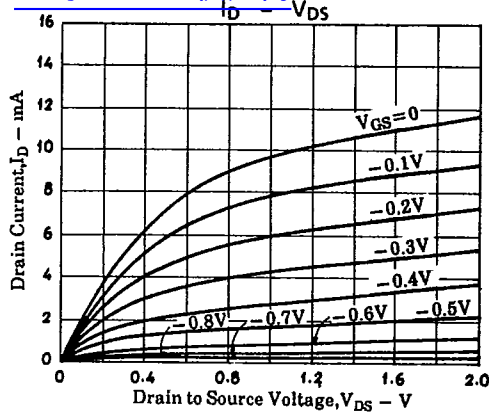


N148MO,TS No.2840-1/3

2SK931

T-31-25

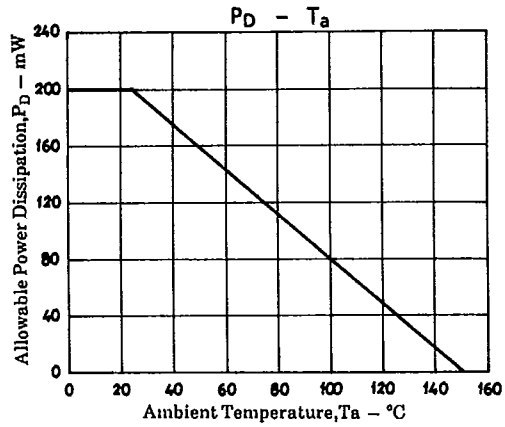
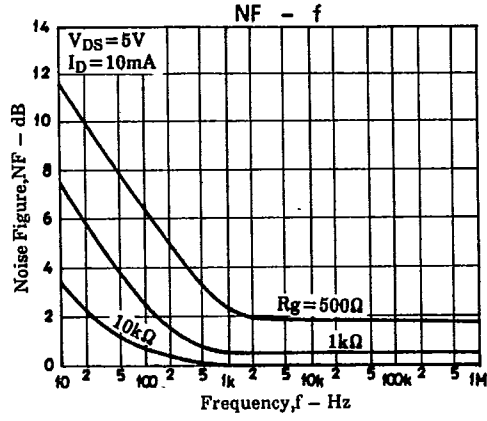
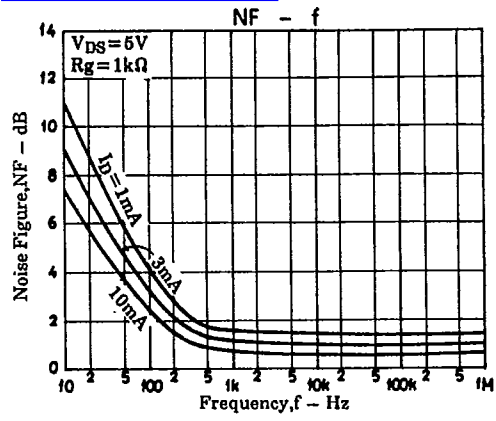
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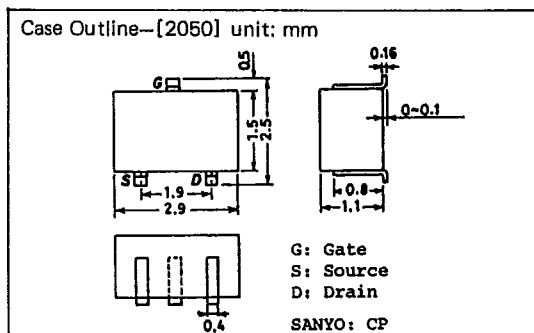
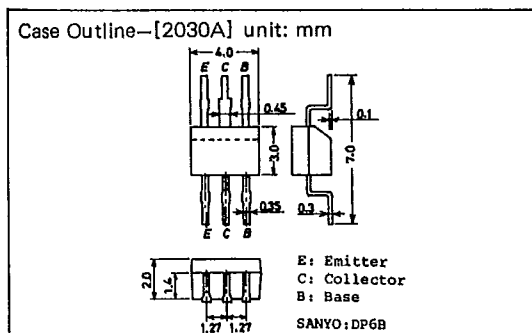
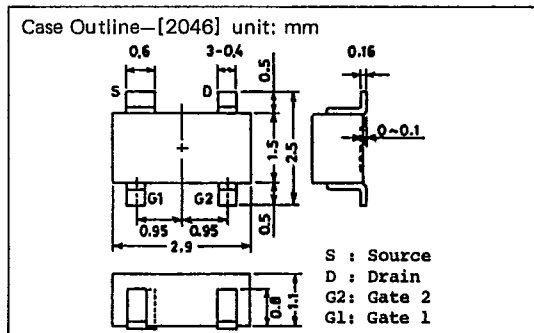
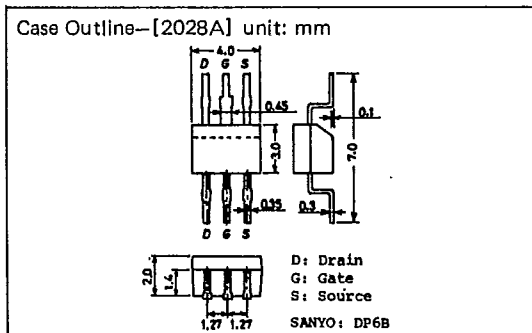
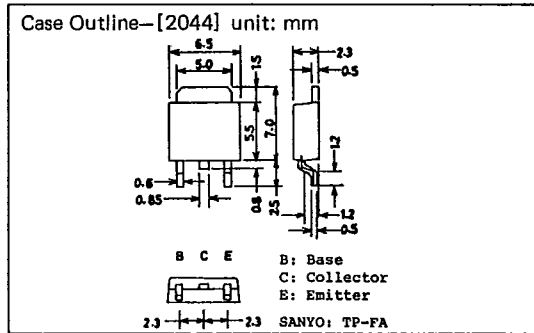
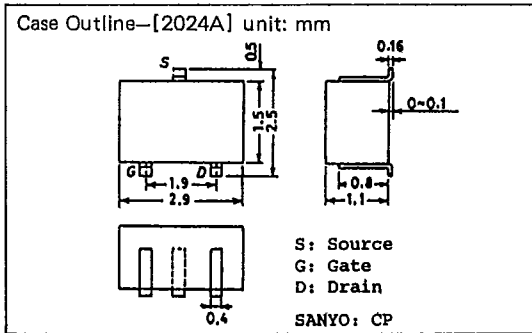
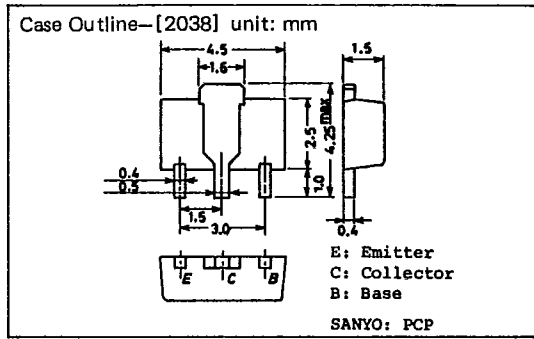
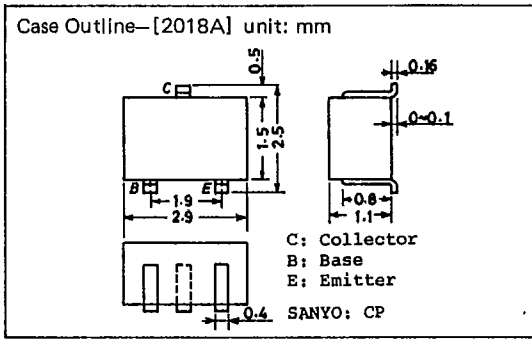


T-91-20

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CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

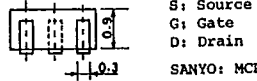
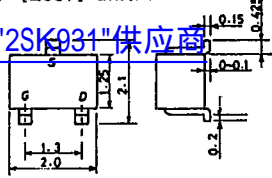
- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



T-91-20

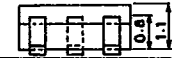
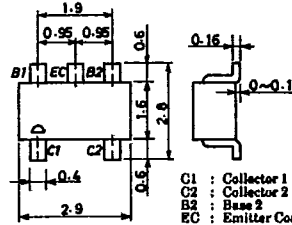
Case Outline—[2057] unit: mm

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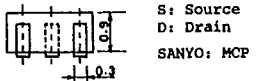
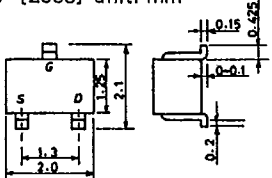
S: Source
G: Gate
D: Drain
SANYO: MCP

Case Outline—[2066] unit: mm



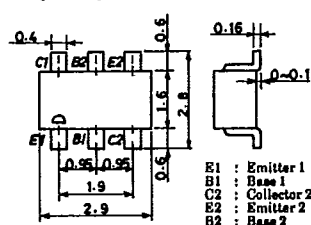
C1 : Collector 1
C2 : Collector 2
E2 : Base 2
EC : Emitter Common
B1 : Base 1
SANYO: CP6

Case Outline—[2058] unit: mm



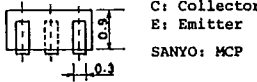
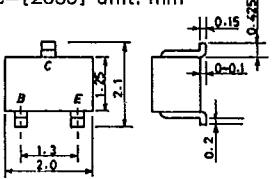
G: Gate
S: Source
D: Drain
SANYO: MCP

Case Outline—[2067] unit: mm



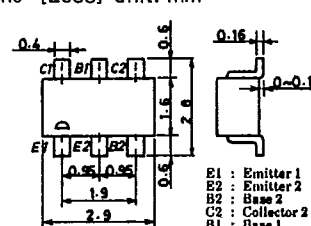
E1 : Emitter 1
B1 : Base 1
C2 : Collector 2
E2 : Emitter 2
B2 : Base 2
C1 : Collector 1
SANYO: CP6

Case Outline—[2059] unit: mm



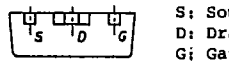
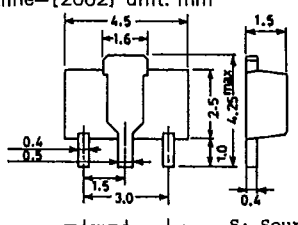
B: Base
C: Collector
E: Emitter
SANYO: MCP

Case Outline—[2068] unit: mm



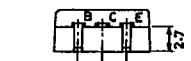
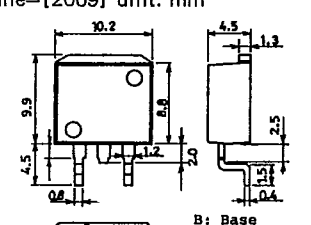
E1 : Emitter 1
E2 : Emitter 2
B2 : Base 2
C2 : Collector 2
B1 : Base 1
C1 : Collector 1
SANYO: CP6

Case Outline—[2062] unit: mm



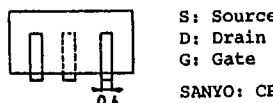
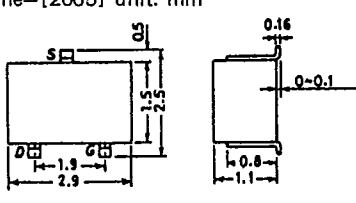
S: Source
D: Drain
G: Gate
SANYO: PCP

Case Outline—[2069] unit: mm



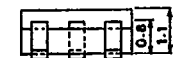
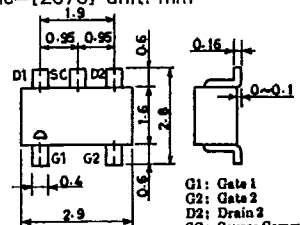
B: Base
C: Collector
E: Emitter
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source
D: Drain
G: Gate
SANYO: CP

Case Outline—[2070] unit: mm

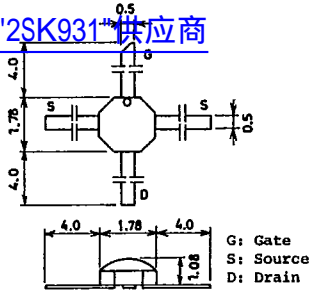


G1: Gate 1
G2: Gate 2
D2: Drain 2
SC: Source Common
D1: Drain 1
SANYO: CP6

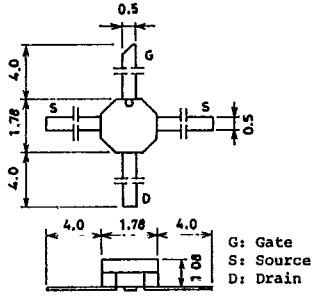
T-9120

Case Outline-[2071] unit: mm

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Case Outline-[2072] unit: mm



Case Outline-[2073] unit: mm

