1 Introduction

1.1 Features

- Stereo Audio DAC with 100dB SNR
- 4.1mW Stereo 48ksps DAC Playback
- Stereo Audio ADC with 93dB SNR
- 6.1mW Stereo 48ksps ADC Record
- PowerTune™
- Extensive Signal Processing Options
- Six Single-Ended or 3 Fully-Differential Analog Inputs
- Stereo Analog and Digital Microphone Inputs
- Stereo Headphone Outputs
- Stereo Line Outputs
- Very Low-Noise PGA
- Low Power Analog Bypass Mode
- Programmable Microphone Bias
- Programmable PLL
- Integrated LDO
- 5 mm x 5 mm 32-pin QFN Package

1.2 Applications

- Portable Navigation Devices (PND)
- Portable Media Player (PMP)
- Mobile Handsets
- Communication
- Portable Computing

1.3 Description

The TLV320AIC3204 (sometimes referred to as the AIC3204) is a flexible, low-power, low-voltage stereo audio codec with programmable inputs and outputs, PowerTune capabilities, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDOs and flexible digital interfaces.

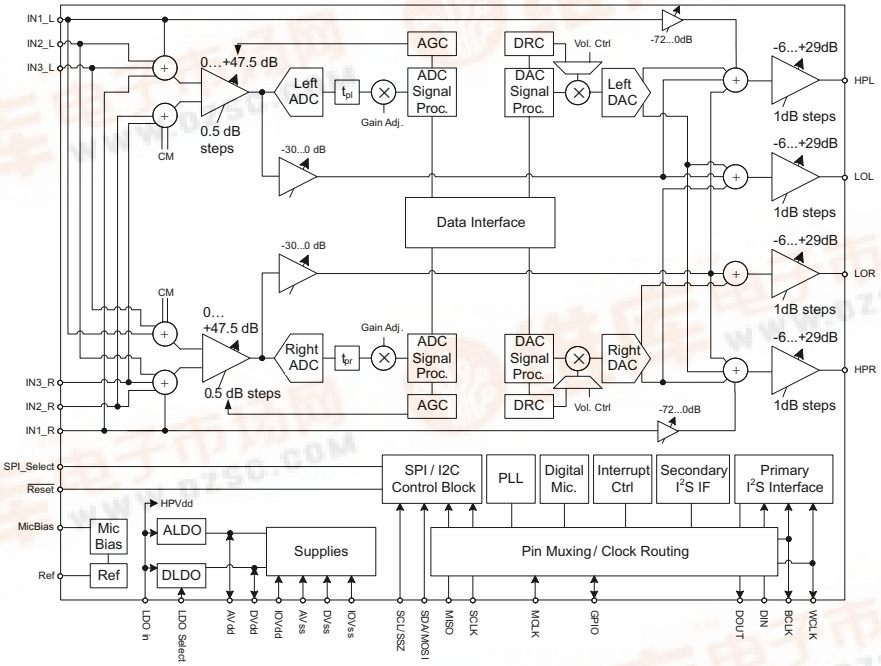


Figure 1-1. Simplified Block Diagram

1.4 Detailed Description

Extensive Register based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application. Combined with the advanced PowerTune technology, the device can cover operations from 8 kHz mono voice playback to audio stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3204 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally-controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling, e.g. optical zooming in a digital camera.

The playback path offers signal-processing blocks for filtering and effects, and supports flexible mixing of DAC and analog input signals as well as programmable volume controls. The playback path contains two high-power output drivers as well as two fully-differential outputs. The high-power outputs can be configured in multiple ways, including stereo and mono BTL.

The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern, while minimizing noise is important. With PowerTune, the TLV320AIC3204 addresses both cases.

The voltage supply range for the TLV320AIC3204 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, LDOs are integrated to generate the appropriate analog or digital supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.1V–3.6V.

The required internal clock of the TLV320AIC3204 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

The device is available in the 5-mm $\times$ 5-mm, 32-pin QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

2 Package and Signal Descriptions

2.1 Packaging/Ordering Information

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC3204	QFN	RHB	–40°C to 85°C	TLV320AIC3204IRHBT	Tape and Reel, 250
				TLV320AIC3204IRHBR	Tape and Reel, 3000

2.2 Pin Assignments

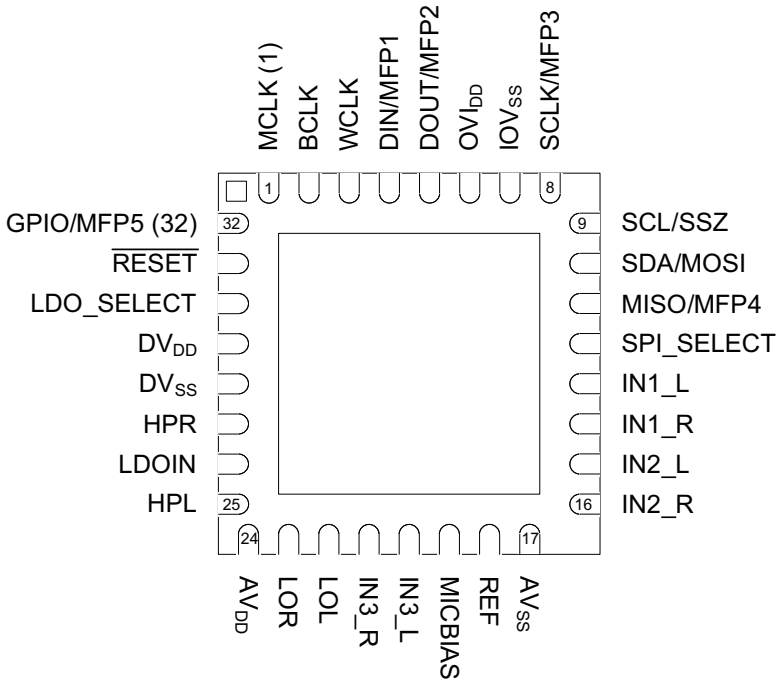


Figure 2-1. QFN (RHB) Package, Bottom View

Table 2-1. TERMINAL FUNCTIONS

TERMINAL	NAME	TYPE	DESCRIPTION
1	MCLK	I	Master Clock Input
2	BCLK	IO	Audio serial data bus (primary) bit clock
3	WCLK	IO	Audio serial data bus (primary) word clock
4	DIN MFP1	I	Primary function Audio serial data bus data input Secondary function Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) word clock input Digital Microphone Input Clock Input General Purpose Input
5	DOUT MFP2	O	Primary Audio serial data bus data output Secondary General Purpose Output Clock Output INT1 Output INT2 Output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
6	IOVDD	Power	I/O voltage supply 1.1V – 3.6V
7	IOVSS	Ground	I/O ground supply
8	SCLK MFP3	I	Primary (SPI_Select = 1) SPI serial clock Secondary: (SPI_Select = 0) Headset-detect input Digital microphone input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC/common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General Purpose Input
9	SCL/ SSZ	I	I^2C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1)
10	SDA/ MOSI	I	I^2C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1)
11	MISO MFP4	O	Primary (SPI_Select = 1) Serial data output Secondary (SPI_Select = 0) General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Digital microphone clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
12	SPI_ SELECT	I	Control mode select pin (1 = SPI, 0 = I^2C)

Table 2-1. TERMINAL FUNCTIONS (continued)

TERMINAL	NAME	TYPE	DESCRIPTION
13	IN1_L	I	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 left or Differential configuration: MIC or Line right, negative
14	IN1_R	I	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 right or Differential configuration: MIC or Line right, positive
15	IN2_L	I	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 right or Differential configuration: MIC or Line left, positive
16	IN2_R	I	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 right or Differential configuration: MIC or Line left, negative
17	AVss	Ground	Analog ground supply
18	REF	O	Reference voltage output for filtering
19	MICBIAS	O	Microphone bias voltage output
20	IN3_L	I	Multifunction Analog Input, or Single-ended configuration: MIC3 or Line 3 left, or Differential configuration: MIC or Line left, positive, or Differential configuration: MIC or Line right, negative
21	IN3_R	I	Multifunction Analog Input, or Single-ended configuration: MIC3 or Line 3 right, or Differential configuration: MIC or Line left, negative, or Differential configuration: MIC or Line right, positive
22	LOL	O	Left line output
23	LOR	O	Right line output
24	AVdd	Power	Analog voltage supply 1.5V–1.95V Input when A-LDO disabled, Filtering output when A-LDO enabled
25	HPL	O	Left high power output driver
26	LDOIN/ HPVDD	Power	LDO Input supply and Headphone Power supply 1.9V– 3.6V
27	HPR	O	Right high power output driver
28	DVss	Ground	Digital Ground and Chip-substrate
29	DVdd	Power	If LDO_SELECT Pin = 0 (D-LDO disabled) Digital voltage supply 1.26V – 1.95V If LDO_SELECT Pin = 1 (D-LDO enabled) Digital voltage supply filtering output
30	LDO_ SELECT	I	connect to DVss.
31	$\overline{\text{RESET}}$	I	Reset (active low)
32	GPIO MFP5	I	Primary General Purpose digital IO Secondary CLKOUT Output INT1 Output INT2 Output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output

3 Electrical Specifications

3.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
AVdd to AVss		–0.3 to 2.2	V
DVdd to DVss		–0.3 to 2.2	V
IOVDD to IOVSS		–0.3 to 3.9	V
LDOIN to AVss		–0.3 to 3.9	V
Digital Input voltage to ground		–0.3 to IOVDD + 0.3	V
Analog input voltage to ground		–0.3 to AVdd + 0.3	V
Operating temperature range		–40 to 85	°C
Storage temperature range		–55 to 125	°C
Junction temperature (T_J Max)		105	°C
	Power dissipation (with thermal pad soldered to board)	(T_J Max – TA)/ θ_{JA}	W
	θ_{JA} Thermal impedance	35	C/W
Lead Temperature	Infrared (15 sec)	260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
LDOIN	Power Supply Voltage Range	Referenced to AVss(1)	1.9		3.6	V
AVdd			1.5	1.8	1.95	V
IOVDD		Referenced to IOVSS(1)	1.1		3.6	V
DVdd(2)		Referenced to DVss(1)	1.26	1.8	1.95	V
	PLL Input Frequency	Clock divider uses fractional divide (D > 0), P=1, $D_{Vdd} \geq 1.65V$ (Refer to Table 5-23)	10		20	MHz
		Clock divider uses integer divide (D = 0), P=1, $D_{Vdd} \geq 1.65V$ (Refer to Table 5-23)	0.512		20	MHz
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; $D_{Vdd} \geq 1.65V$			50	MHz
		MCLK; Master Clock Frequency; $D_{Vdd} \geq 1.26V$			25	
SCL	SCL Clock Frequency				400	kHz
LOL, LOR	Stereo line output load resistance		0.6	10		kΩ
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω
	Headphone output load resistance	Differential configuration	24.4	32		Ω
C_{Lout}	Digital output load capacitance			10		pF
TOPR	Operating Temperature Range		–40		85	°C

(1) All grounds on board are tied together, so they should not differ in voltage by more than 0.2V max, for any combination of ground signals.
(2) At DVdd values lower than 1.65V, the PLL does not function. Please see Table 5-23 for details on maximum clock frequencies.

3.3 ELECTRICAL CHARACTERISTICS

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0dB)	Single-ended, CM = 0.9V		0.5		V_{RMS}
	Device Setup	1kHz sine wave input Single-ended Configuration IN1R to Right ADC and IN1L to Left ADC, R_{in} = 20K, f_s = 48kHz, AOSR = 128, MCLK = 256*f_s, PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Inputs ac-shorted to ground	80	93		dB
		IN2R, IN3R routed to Right ADC and ac-shorted to ground IN2L, IN3L routed to Left ADC and ac-shorted to ground		93		
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		92		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		–85	–70	dB
		IN2R,IN3R routed to Right ADC IN2L, IN3L routed to Left ADC –3dB full-scale, 1-kHz input signal		–85		
AUDIO ADC						
	Input signal level (0dB)	Single-ended, CM=0.75V, AVdd = 1.5V		0.375		V_{RMS}
	Device Setup	1kHz sine wave input Single-ended Configuration IN1R, IN2R, IN3R routed to Right ADC IN1L, IN2L, IN3L routed to Left ADC R_{in} = 20K, f_s = 48kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1 Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted (1) (2)	Inputs ac-shorted to ground		91		dB
DR	Dynamic range A-weighted(1) (2)	–60dB full-scale, 1-kHz input signal		90		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–80		dB
AUDIO ADC						
	Input signal level (0dB)	Differential Input, CM=0.9V		10		mV
	Device Setup	1kHz sine wave input Differential configuration IN1L and IN1R routed to Right ADC IN2L and IN2R routed to Left ADC R_{in} =10K, f_s =48kHz, AOSR=128 MCLK = 256* f_s PLL Disabled AGC = OFF, Channel Gain=40dB Processing Block = PRB_R1, Power Tune = PTM_R4				
ICN	Idle-Channel Noise, A-weighted(1) (2)	Inputs ac-shorted to ground, input referred noise		2		µV_{RMS}

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

ELECTRICAL CHARACTERISTICS *(continued)*

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC					
Gain Error	1kHz sine wave input Single-ended configuration R_{in} = 20K f_s = 48kHz, AOSR=128, MCLK = 256* f_s, PLL Disabled AGC = OFF, Channel Gain=0dB Processing Block = PRB_R1, Power Tune = PTM_R4, CM=0.9V		–0.05		dB
Input Channel Separation	1kHz sine wave input at -3dBFS Single-ended configuration IN1L routed to Left ADC IN1R routed to Right ADC, R_{in} = 20K AGC = OFF, AOSR = 128, Channel Gain=0dB, CM=0.9V		108		dB
Input Pin Crosstalk	1kHz sine wave input at –3dBFS on IN2L, IN2L internally not routed. IN1L routed to Left ADC ac-coupled to ground 1kHz sine wave input at –3dBFS on IN2R, IN2R internally not routed. IN1R routed to Right ADC ac-coupled to ground Single-ended configuration R_{in} = 20K, AOSR=128 Channel, Gain=0dB, CM=0.9V		115		dB
PSRR	217Hz, 100mVpp signal on AVdd, Single-ended configuration, Rin=20K, Channel Gain=0dB; CM=0.9V		55		dB
ADC programmable gain amplifier gain	Single-Ended, Rin = 10K, PGA gain set to 0dB		0		dB
	Single-Ended, Rin = 10K, PGA gain set to 47.5dB		47.5		dB
	Single-Ended, Rin = 20K, PGA gain set to 0dB		–6		dB
	Single-Ended, Rin = 20K, PGA gain set to 47.5dB		41.5		dB
	Single-Ended, Rin = 40K, PGA gain set to 0dB		–12		dB
	Single-Ended, Rin = 40K, PGA gain set to 47.5dB		35.5		dB
ADC programmable gain amplifier step size	1-kHz tone		0.5		dB

ELECTRICAL CHARACTERISTICS *(continued)*

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM=0.9V; Headphone Output on LDOIN Supply; IN1L routed to HPL and IN1R routed to HPR; Channel Gain=0dB				
	Gain Error			–0.8		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		3		μV_{RMS}
THD	Total Harmonic Distortion	446mVrms, 1-kHz input signal		–89		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE						
	Device Setup	Load = 10KOhm (single-ended), 56pF; Input and Output CM=0.9V; LINE Output on LDOIN Supply; IN1L routed to ADCPGA_L and IN1R routed to ADCPGA_R; Rin = 20k ADCPGA_L routed to LOL and ADCPGA_R routed to LOR; Channel Gain = 0dB				
	Gain Error			0.6		dB
	Noise, A-weighted(1)	Idle Channel, IN1L and IN1R ac-shorted to ground		7		μV_{RMS}
		Channel Gain=40dB, Input Signal (0dB) = $5mV_{rms}$ Inputs ac-shorted to ground, Input Referred		3.4		μV_{RMS}
MICROPHONE BIAS						
	Bias voltage	Bias voltage CM=0.9V, LDOin = 3.3V				
		Micbias Mode 0, Connect to AVdd or LDOin		1.25		V
		Micbias Mode 1, Connect to LDOin		1.7		V
		Micbias Mode 2, Connect to LDOin		2.5		V
		Micbias Mode 3, Connect to AVdd		AVdd		V
		Micbias Mode 3, Connect to LDOin		LDOin		V
		CM=0.75V, LDOin = 3.3V				
		Micbias Mode 0, Connect to AVdd or LDOin		1.04		V
		Micbias Mode 1, Connect to AVdd or LDOin		1.425		V
		Micbias Mode 2, Connect to LDOin		2.075		V
		Micbias Mode 3, Connect to AVdd		AVdd		V
		Micbias Mode 3, Connect to LDOin		LDOin		V
	Output Noise	CM=0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		10		μV_{RMS}
	Current Sourcing	Micbias Mode 2, Connect to LDOin		3		mA
	Inline Resistance	Micbias Mode 3, Connect to AVdd		140		Ω
		Micbias Mode 3, Connect to LDOin		87		Ω

(1) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

ELECTRICAL CHARACTERISTICS *(continued)*

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.9V DOSR = 128, MCLK=256* f_s, Channel Gain = 0dB, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio A-weighted(1) (2)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word length=20 bits		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–83	–70	dB
	DAC Gain Error	0 dB, 1kHz input full scale signal		0.3		dB
	DAC Mute Attenuation	Mute		119		dB
	DAC channel separation	–1 dB, 1kHz signal, between left and right HP out		113		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		73		dB
		100mVpp, 217Hz signal applied to AVdd		77		dB
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10 kΩ (single-ended), 56pF Line Output on AVdd Supply Input & Output CM=0.75V; AVdd=1.5V DOSR = 128 MCLK=256* fs Channel Gain = –2dB word length = 20-bits Processing Block = PRB_P1 Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1 kHz input full-scale signal		97		dB
THD+N	Total Harmonic Distortion plus Noise	–1 dB full-scale, 1-kHz input signal		–85		dB
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT						
	Device Setup	Load = 16Ω (single-ended), 50pF Headphone Output on AVdd Supply, Input & Output CM=0.9V, DOSR = 128, MCLK=256* f_s, Channel Gain=0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–83	–70	dB
	DAC Gain Error	0dB, 1kHz input full scale signal		–0.3		dB
	DAC Mute Attenuation	Mute		122		dB
	DAC channel separation	–1dB, 1kHz signal, between left and right HP out		110		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AVdd		73		dB
		100mVpp, 217Hz signal applied to AVdd		78		dB

(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

ELECTRICAL CHARACTERISTICS *(continued)*

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power Delivered	R_L=16Ω, Output Stage on AVdd = 1.8V THDN < 1%, Input CM=0.9V, Output CM=0.9V		15		mW
		R_L=16 Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM=0.9V, Output CM=1.65V		64		
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT						
	Device Setup	Load = 16Ω (single-ended), 50pF, Headphone Output on AVdd Supply, Input & Output CM=0.75V; AVdd=1.5V, DOSR = 128, MCLK=256* f_s, Channel Gain = –2dB, word length=20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	-60dB 1 kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	–1dB full-scale, 1-kHz input signal		–83		dB
AUDIO DAC – MONO DIFFERENTIAL HEADPHONE OUTPUT						
	Device Setup	Load = 32 Ω (differential), 50pF, Headphone Output on LDOIN Supply Input CM = 0.75V, Output CM=1.5V, AVdd=1.8V, LDOIN=3.0V, DOSR = 128 MCLK=256* f_s, Channel (headphone driver) Gain = 5dB for full scale output signal, word length=16-bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			1778		mV_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	All zeros fed to DAC input		98		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal		96		dB
THD	Total Harmonic Distortion	–3dB full-scale, 1-kHz input signal		–82		dB
	Power Delivered	R_L=32Ω, Output Stage on LDOIN = 3.3V, THDN < 1%, Input CM=0.9V, Output CM=1.65V		136		mW
		R_L=32Ω Output Stage on LDOIN = 3.0V, THDN < 1% Input CM=0.9V, Output CM=1.5V		114		mW
LOW DROPOUT REGULATOR (AVdd)						
	Output Voltage	LDOMode = 1, LDOin > 1.95V		1.67		V
		LDOMode = 0, LDOin > 2.0V		1.72		
		LDOMode = 2, LDOin > 2.05V		1.77		
	Output Voltage Accuracy			±2		%
	Load Regulation	Load current range 0 to 50mA		15		mV
	Line Regulation	Input Supply Range 1.9V to 3.6V		5		mV
	Decoupling Capacitor		1			µF
	Bias Current			60		µA
LOW DROPOUT REGULATOR (DVdd)						
	Output Voltage	LDOMode = 1, LDOin > 1.95V		1.67		V
		LDOMode = 0, LDOin > 2.0V		1.72		
		LDOMode = 2, LDOin > 2.05V		1.77		
	Output Voltage Accuracy			±2		%
	Load Regulation	Load current range 0 to 50mA		15		mV
	Line Regulation	Input Supply Range 1.9V to 3.6V		5		mV
	Decoupling Capacitor		1			µF
	Bias Current			60		µA

ELECTRICAL CHARACTERISTICS *(continued)*

At 25°C, AVdd, DVdd, IOVDD = +1.8V, LDO_in = 3.3V, AVdd LDO disabled, f_s (Audio) = 48kHz, Cref = 10 µF on REF PIN, PLL disabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
	CMMode = 1 (0.75V)		0.75		
Reference Noise	CM=0.9V, A-weighted, 20Hz to 20kHz bandwidth, C_{ref} = 10µF		1		μV_{RMS}
Decoupling Capacitor		1	10		µF
Bias Current			120		µA
Shutdown Current					
Device Setup	Coarse AVdd supply turned off LDO_select held at ground No external digital input is toggled.				
I(DVdd)			0.9		µA
I(AVdd)			<0.9		µA
I(LDOin)			<0.9		µA
I(IOVDD)			13		nA

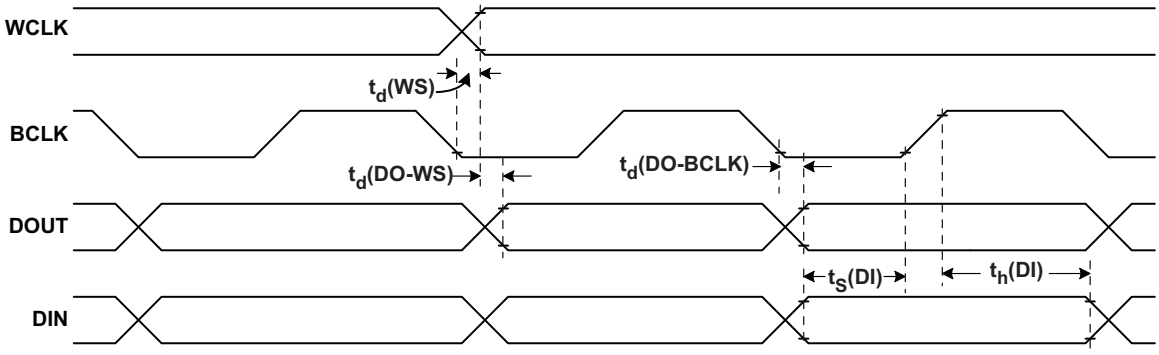
3.4 ELECTRICAL CHARACTERISTICS

At 25°C, AVdd, DVdd, IOVDD = 1.8V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY			**CMOS**		
V_{IH} Logic Level	I_{IH} = 5 µA, IOVDD > 1.6V	0.7 × IOVDD			V
	I_{IH} = 5µA, 1.2V ≤ IOVDD <1.6V	0.9 × IOVDD			V
	I_{IH} = 5µA, IOVDD < 1.2V	IOVDD			V
V_{IL}	I_{IL} = 5 µA, IOVDD > 1.6V	–0.3		0.3 × IOVDD	V
	I_{IL} = 5µA, 1.2V ≤ IOVDD <1.6V			0.1 × IOVDD	V
	I_{IL} = 5µA, IOVDD < 1.2V			0	V
V_{OH}	I_{OH} = 2 TTL loads	0.8 × IOVDD			V
V_{OL}	I_{OL} = 2 TTL loads			0.1 × IOVDD	V
Capacitive Load			10		pF

3.4.1 TIMING — AUDIO DATA SERIAL INTERFACE TIMING

All numbers are from characterization and are not tested in final production.



I2S/LJF Timing in Master Mode

Figure 3-1. I²S/LJF/RJF Timing in Master Mode

All numbers are from characterization and are not tested in final production.

3.4.2 TYPICAL TIMING CHARACTERISTICS (see Figure 3-1)

All specifications at 25°C, DVdd = 1.8V

Table 3-1. I²S/LJF/RJF Timing in Master Mode

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		30		20	ns
t_d (DO-WS)	WCLK to DOUT delay (For LJF Mode only)		20		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

Note: All timing specifications are measured at characterization but not tested at final test.

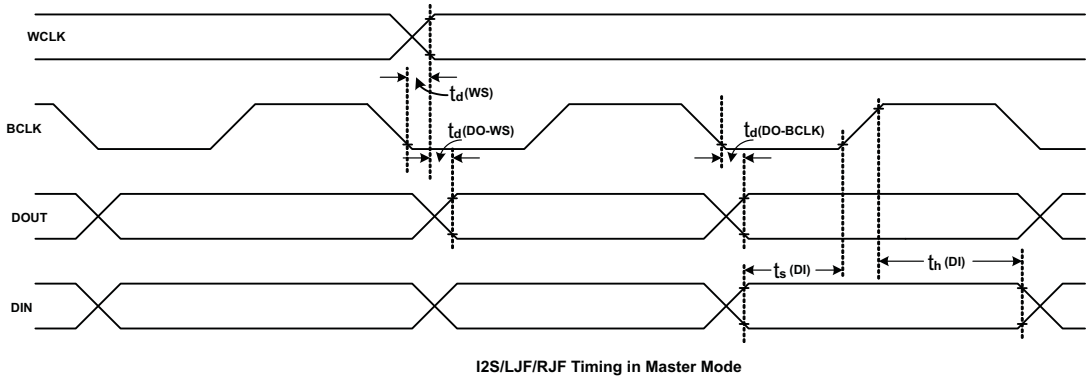


Figure 3-2. I²S/LJF/RJF Timing in Slave Mode

3.4.3 TYPICAL TIMING CHARACTERISTICS (see Figure 3-2)

All specifications at 25°C, DVdd = 1.8V

Table 3-2. I²S/LJF/RJF Timing in Slave Mode

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
$BCLK_H$ (BCLK)	BCLK high period	35		35		ns
$BCLK_L$ (BCLK)	BCLK low period	35		35		
t_s (WS)	WCLK setup	8		8		
t_h (WS)	WCLK hold	8		8		
t_d (DO-WS)	WCLK to DOUT delay (For LJF mode only)		20		20	
t_d (DO-BCLK)	BCLK to DOUT delay		22		22	
t_s(DI)	DIN setup	8		8		
t_h(DI)	DIN hold	8		8		
t_r	Rise time		4		4	
t_f	Fall time		4		4	

Note: All timing specifications are measured at characterization but not tested at final test.

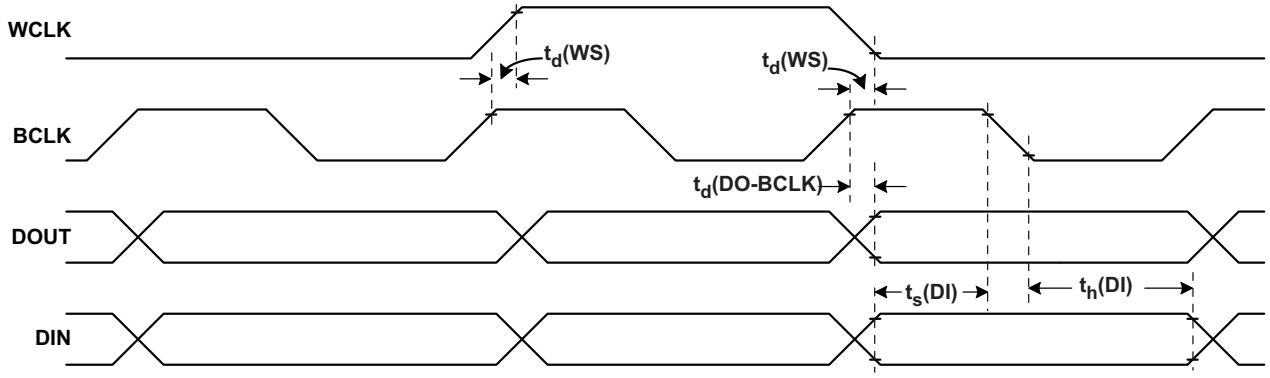


Figure 3-3. DSP Timing in Master Mode

3.4.3.1 TYPICAL TIMING CHARACTERISTICS (see Figure 3-3)

All specifications at 25°C, DVdd = 1.8V

Table 3-3. DSP Timing in Master Mode

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_d (WS)	WCLK delay		30		20	ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		24		12	ns
t_f	Fall time		24		12	ns

Note: All timing specifications are measured at characterization but not tested at final test.

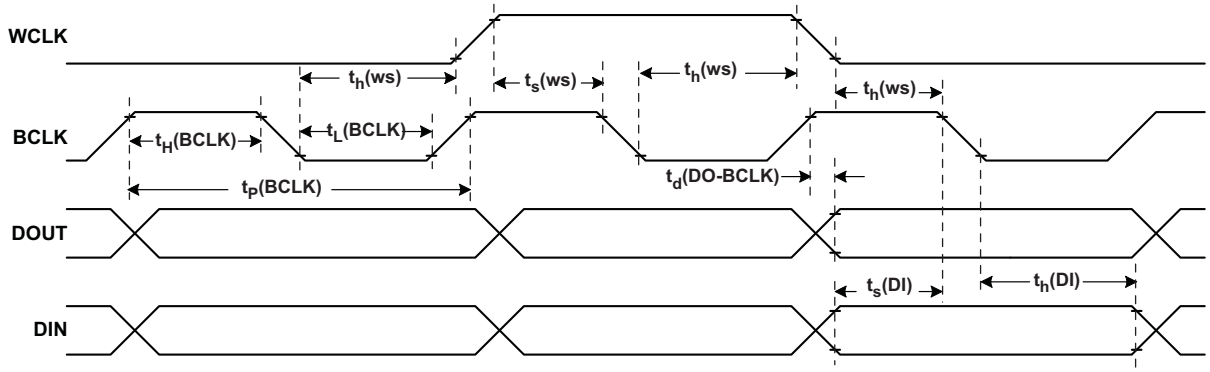


Figure 3-4. DSP Timing in Slave Mode

3.4.3.2 TYPICAL TIMING CHARACTERISTICS (see Figure 3-4)

All specifications at 25°C, DVdd = 1.8V

Table 3-4. DSP Timing in Slave Mode

PARAMETER		IOVDD=1.8V		IOVDD=3.3V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		8		ns
t_h(WS)	WCLK hold	8		8		ns
t_d (DO-BCLK)	BCLK to DOUT delay		22		22	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

Note: All timing specifications are measured at characterization but not tested at final test.

3.4.4 I^2C INTERFACE TIMING

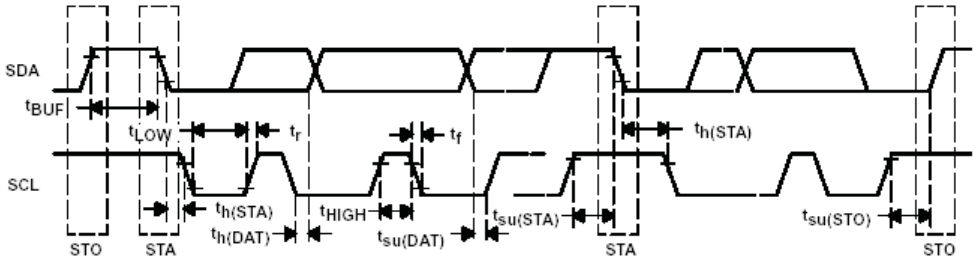


Figure 3-5.

Table 3-5. I^2C INTERFACE TIMING

PARAMETER		TEST CONDITION	Standard-Mode			Fast-Mode			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency		0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0			0.8			µs
t_{LOW}	LOW period of the SCL clock		4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock		4.0			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition		4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: For I2C bus devices		0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time		250			100			ns
t_r	SDA and SCL Rise Time				1000	20+0.1C_b		300	ns
t_f	SDA and SCL Fall Time				300	20+0.1C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition		4.7			1.3			µs
C_b	Capacitive load for each bus line				400			400	pF

3.4.5 SPI INTERFACE TIMING

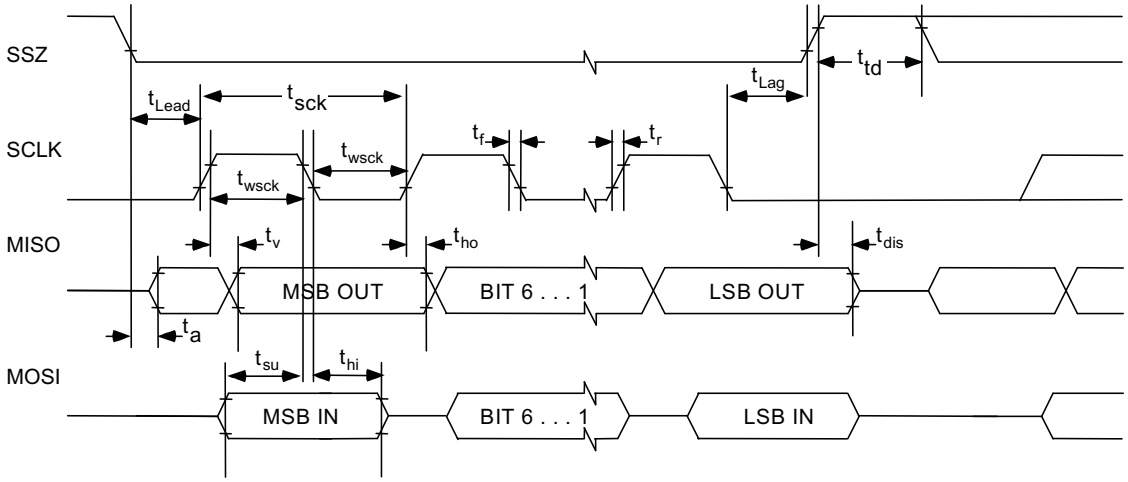


Figure 3-6. SPI Interface Timing Diagram

3.4.5.1 TIMING REQUIREMENTS (SEE Figure 3-6)

At 25°C, DVdd = 1.8V

Table 3-6. SPI Interface Timing

PARAMETER		TEST CONDITION	IOVDD=1.8V			IOVDD=3.3V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period(1)		100			50			ns
t_{sckh}	SCLK Pulse width High		50			25			ns
t_{sckl}	SCLK Pulse width Low		50			25			ns
t_{lead}	Enable Lead Time		30			20			ns
t_{trail}	Enable Trail Time		30			20			ns
$t_{d;seqxfr}$	Sequential Transfer Delay		40			20			ns
t_a	Slave DOUT access time				40			20	ns
t_{dis}	Slave DOUT disable time				40			20	ns
t_{su}	DIN data setup time		15			10			ns
$t_{h;DIN}$	DIN data hold time		15			10			ns
$t_{v;DOUT}$	DOUT data valid time				25			18	ns
t_r	SCLK Rise Time				4			4	ns
t_f	SCLK Fall Time				4			4	ns

(1) These parameters are based on characterization and are not tested in production.

4 TYPICAL CHARACTERISTICS

4.1 TYPICAL PERFORMANCE

ADC SNR
vs
CHANNEL GAIN

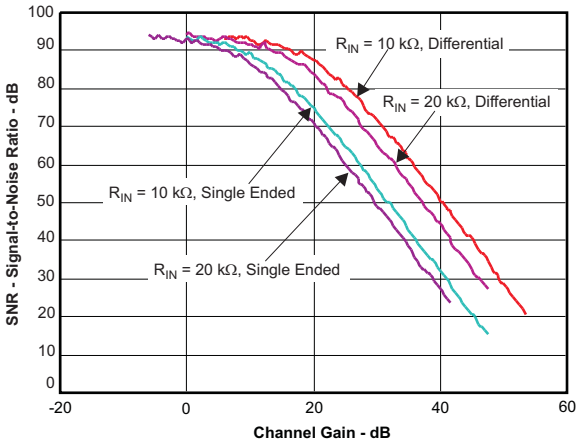


Figure 4-1.

TOTAL HARMONIC DISTORTION
vs
HEADPHONE OUTPUT POWER

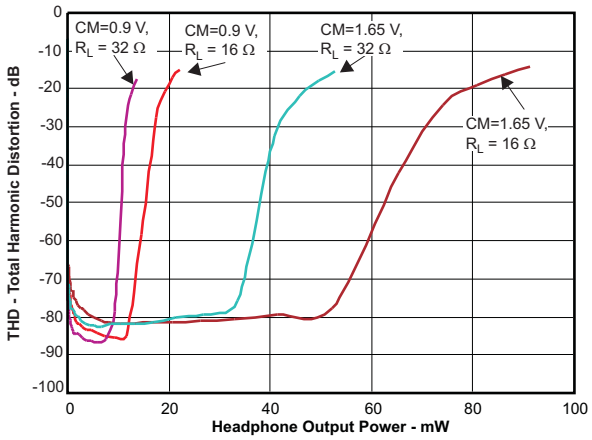


Figure 4-2.

TOTAL HARMONIC DISTORTION
vs
HEADPHONE OUTPUT POWER

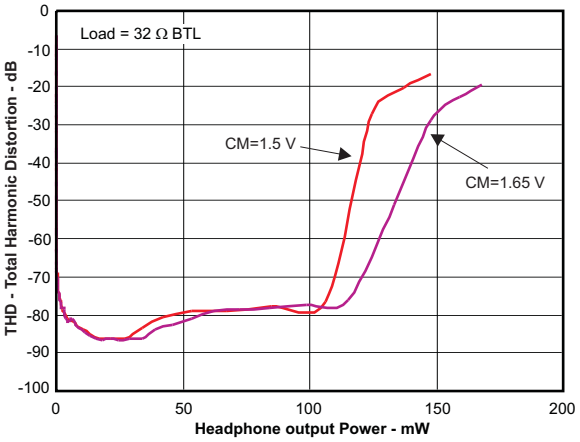


Figure 4-3.

HEADPHONE SNR AND OUTPUT POWER
vs
OUTPUT COMMON MODE SETTING

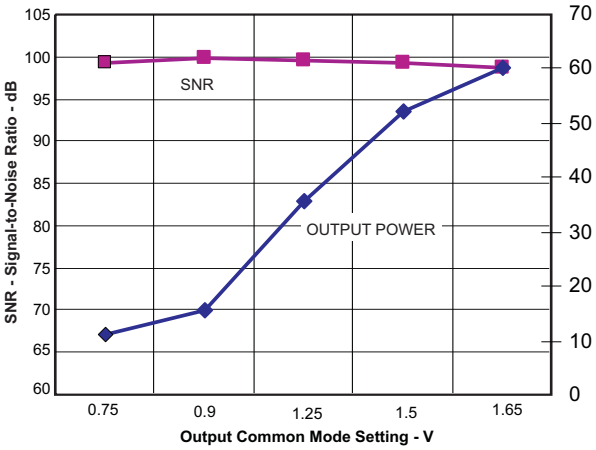


Figure 4-4.

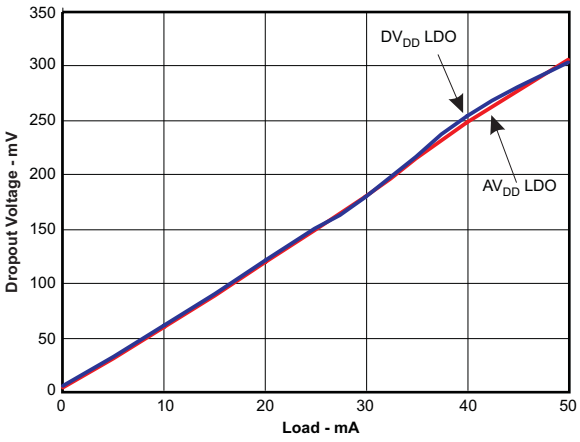


Figure 4-5.

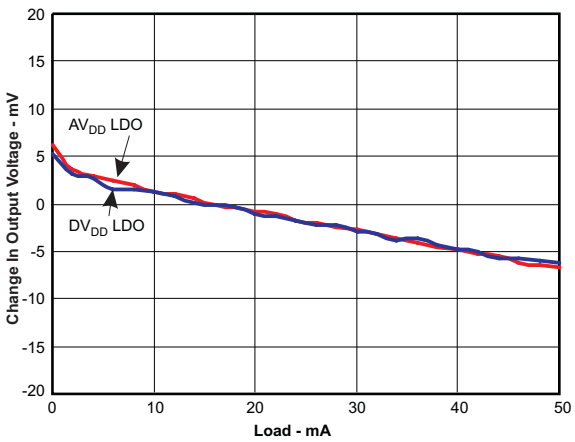


Figure 4-6.

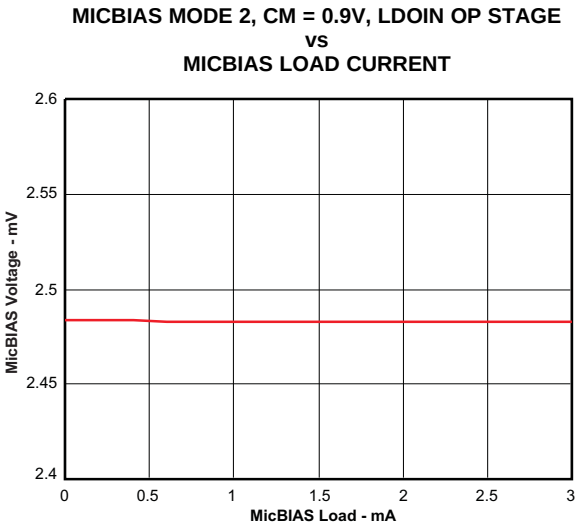


Figure 4-7.

4.2 FFT

SINGLE ENDED LINE INPUT TO ADC FFT @ -1dBr
vs
FREQUENCY

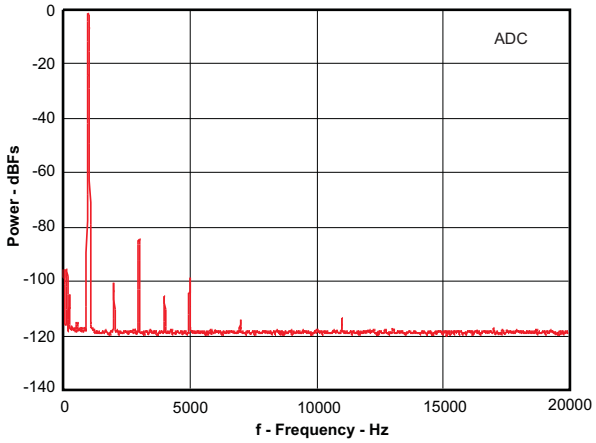


Figure 4-8.

DAC PLAYBACK TO HEADPHONE FFT @ -1dBFS
vs
FREQUENCY

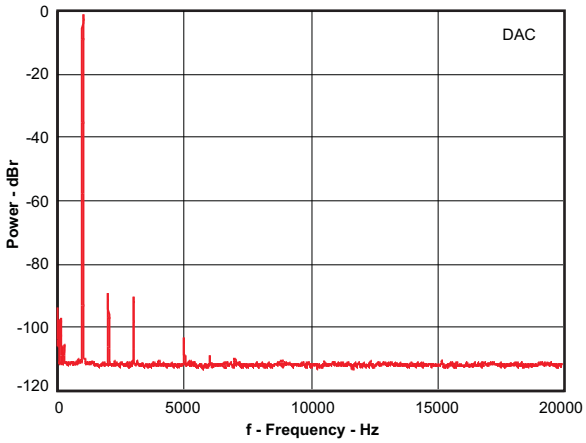


Figure 4-9.

DAC PLAYBACK TO LINE-OUT FFT @ -1dBFS
vs
FREQUENCY

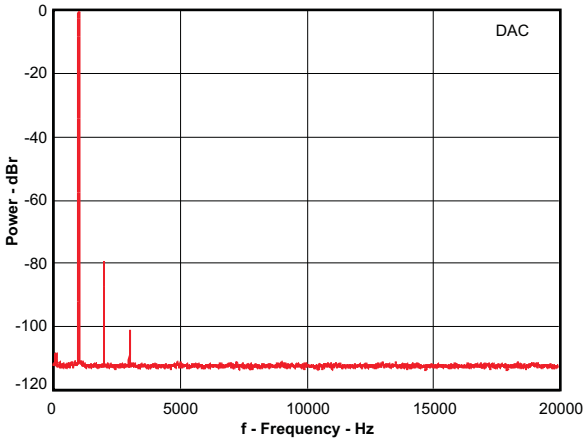


Figure 4-10.

LINE INPUT TO HEADPHONE FFT @ 446mVrms
vs
FREQUENCY

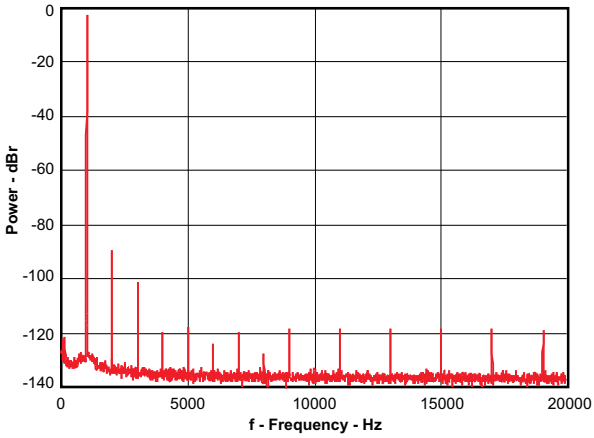


Figure 4-11.

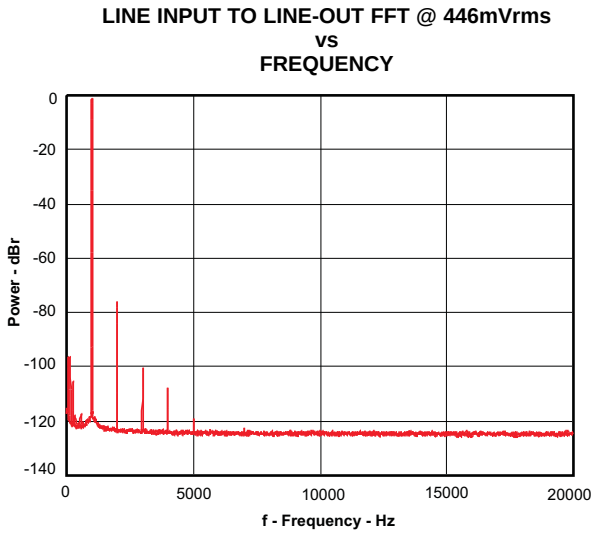

LINE INPUT TO LINE-OUT FFT @ 446mVrms
vs
FREQUENCY
Power - dBr
0
-20
-40
-60
-80
-100
-120
-140
0
5000
10000
15000
20000
f - Frequency - Hz

Figure 4-12.

5 Application Information

5.1 TYPICAL CIRCUIT CONFIGURATION

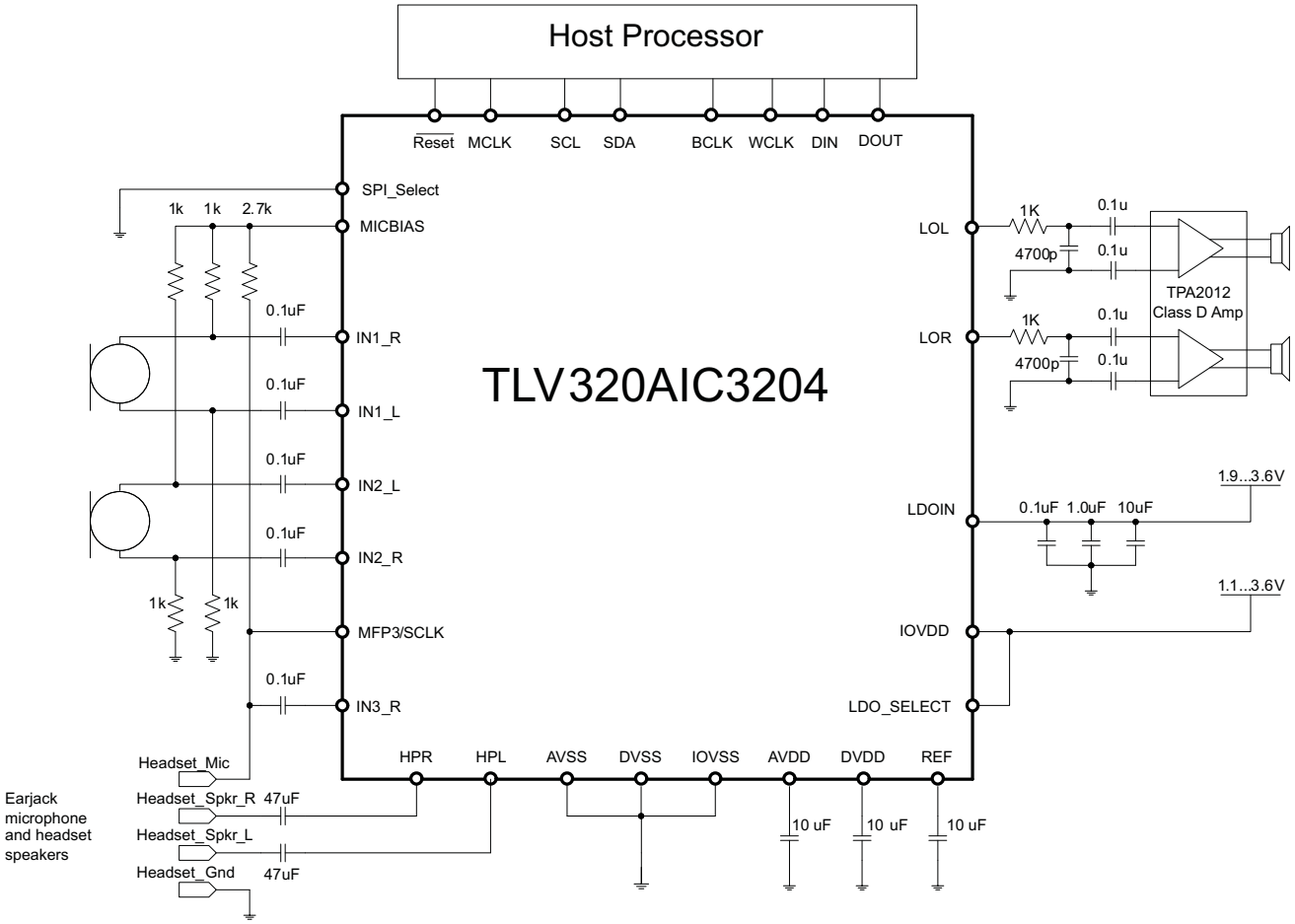


Figure 5-1. Typical Circuit Configuration

5.2 OVERVIEW

The TLV320AIC3204 offers a wide range of configuration options. Figure 1-1 shows the basic functional blocks of the device.

5.2.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset , LDO_Select and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/SSZ and SDA/MOSI are configured for either I^2C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in Section 5.2.5 below.

5.2.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input pins to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in Figure 5-2.

5.2.3 Power Supply

To power up the device, a 3.3V system rail (1.9V to 3.6V) can be used. Internal LDOs generate the appropriate digital core voltage of 1.65V and analog core voltage of 1.8V (minimum 1.5V). For maximum flexibility, the respective voltages can also be supplied externally, bypassing the built-in LDOs. To support high-output drive capabilities, the output stages of the output amplifiers can either be driven from the analog core voltage or the 1.9…3.6V rail used for the LDO inputs (LDO_in).

5.2.4 Clocking

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3204.

5.2.5 Multifunction Pins

The table below shows the possible allocation of pins for specific functions. The PLL input, for example, can be derived from any of 4 pins (MCLK, BCLK, DIN, GPIO). The next table then summarizes the register settings that must be applied to configure the pin assignment. In the second table, the letter/number combination refers to the letter defining the row and the pin number of the first table.

	Pin Function	**1 MCLK**	**2 BCLK**	**3 WCLK**	**4 DIN MFP1**	**5 DOUT MFP2**	**8 SCLK MFP3**	**11 MISO MFP4**	**32 GPIO MFP5**
A	PLL Input	S(1)	S(2)		S(3)				S(4)
B	Codec Clock Input	S(1) ,D(5)	S(2)						S(4)
C	I^2S BCLK input		S(2),D						
D	I^2S BCLK output		E(6)						
E	I^2S WCLK input			E, D					
F	I^2S WCLK output			E					
G	I^2S ADC word clock input						E		E
H	I^2S ADC WCLK out							E	E
I	I^2S DIN				S(3) ,D				
J	I^2S DOUT					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				

(1) S(1): The MCLK pin can be used to drive the PLL and Codec Clock inputs **simultaneously**
(2) S(2): The BCLK pin can be used to drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**
(3) S(3): The DIN/MFP1 pin can be used to drive the PLL and audio interface data inputs **simultaneously**
(4) S(4): The GPIO/MFP5 pin can be used to drive the PLL and Codec Clock inputs simultaneously
(5) D: Default Function
(6) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

	Pin Function	1 MCLK	2 BCLK	3 WCLK	4 DIN MFP1	5 DOUT MFP2	8 SCLK MFP3	11 MISO MFP4	32 GPIO MFP5
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
O	Digital Microphone Data Input				E		E		E
P	Digital Microphone Clock Output							E	E
Q	Secondary I^2S BCLK input						E		E
R	Secondary I^2S WCLK in						E		E
S	Secondary I^2S DIN						E		E
T	Secondary I^2S DOUT							E	
U	Secondary I^2S BLCK OUT					E		E	E
V	Secondary I^2S WCLK OUT					E		E	E
W	Headset Detect Input						E		
X	Aux Clock Output					E		E	E

5.2.6 Register Settings for Multifunction Pins

The table below summarizes the multifunction pin specific settings that must be applied. Please be aware that more settings may be necessary to obtain a full interface definition matching the application requirement (e.g. registers Pg1 Reg 32 and 33).

	Description	Required Register Setting		Description	Required Register Setting
A1	PLL Input on pin 1, MCLK	Pg 0, Reg 4, D(3:2)=00	N5	INT2 output on pin 5, DOUT/MFP2	Pg 0, Reg 53,D(3:1)=101
A2	PLL Input on pin 2, BCLK	Pg 0, Reg 4, D(3:2)=01	N11	INT2 output on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=0101
A4	PLL Input on pin 4, DIN/MFP1	Pg 0, Reg 54, D(2:1)=01 Pg 0, Reg 4, D(3:2)=11	N32	INT2 output on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0110
A32	PLL Input on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 4, D(3:2)=10	O4	Digital Microphone Data Input on pin 4, DIN/MFP1	Pg 0, Reg 54, D(2:1)=01 Pg 0, Reg 81, D(5:4)=10
B1	Codec Clock Input on pin 1, MCLK	Pg 0, Reg 4, D(1:0)=00	O8	Digital Microphone Data Input on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=01 Pg 0, Reg 81, D(5:4)=01
B2	Codec Clock Input on pin 2, BCLK	Pg 0, Reg 4, D(1:0)=01	O32	Digital Microphone Data Input on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 81, D(5:4)=00
B32	Codec Clock Input on pin 32, GPIO/MPF5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 4, D(1:0)=10	P11	Digital Microphone Clock Output on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=0111
C2	I^2S BCLK input on pin 2, BCLK	Pg 0, Reg 27, D(3)=0	P32	Digital Microphone Clock Output on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=1010
D2	I^2S BCLK output on pin 2, BCLK	Pg 0, Reg 27, D(3)=1	Q8	Secondary I^2S BCLK input on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=01 Pg 0, Reg 31,6:5)=01
E3	I^2S WCLK input on pin 3, WCLK	Pg 0, Reg 27, D(2)=0	Q32	Secondary I^2S BCLK input on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 31,6:5)=00
F3	I^2S WCLK output on pin3, WCLK	Pg 0, Reg 27, D(2)=1	R8	Secondary I^2S WCLK in on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=01 Pg 0, Reg 31, D(4:3)=01

	Description	Required Register Setting		Description	Required Register Setting
G8	I^2S ADC word clock input on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=01 Pg 0, Reg 31, D(2:1)=01	R32	Secondary I^2S WCLK in on pin 32, GPIO/MFP50	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 31, D(4:3)=0
G32	I^2S ADC word clock input on pin 32 GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 31, D(2:1)=00	S8	Secondary I^2S DIN on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=01 Pg 0, Reg 31,0=1
H11	I^2S ADC WCLK out on pin 11 MISO/MFP4	Pg 0, Reg 55, D(4:1)=0110	S32	Secondary I^2S DIN on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0001 Pg 0, Reg 31,0=0
H32	I^2S ADC WCLK out on pin 32 GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0111	T11	Secondary I^2S DOUT on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=1000
I4	I^2S DIN on pin 4, DIN/MFP1	Pg 0, Reg 54, D(2:1)=01	U5	Secondary I^2S BCLK OUT on pin 5, DOUT/MFP2	Pg 0, Reg 53, D(3:1)=110
J5	I^2S DOUT on pin 4, DOUT/MFP2	Pg 0, Reg 53, D(3:1)=001	U11	Secondary I^2S BCLK OUT on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=1001
K5	General Purpose Out I on pin 5, DOUT/MFP2	Pg 0, Reg 53, D(3:1)=010	U32	Secondary I^2S BCLK OUT on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=1000
K11	General Purpose Out II on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=0010	V5	Secondary I^2S WCLK OUT on pin 5, SCLK/MFP3	Pg 0, Reg 53, D(3:1)=111
K32	General Purpose Out III on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0011	V11	Secondary I^2S WCLK OUT on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=1010
L4	General Purpose In I on pin 4, DIN/MFP1	Pg 0, Reg 54, D(2:1)=10	V32	Secondary I^2S WCLK OUT on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=1001
L8	General Purpose In II on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=10	W8	Headset Detect Input on pin 8, SCLK/MFP3	Pg 0, Reg 56, D(2:1)=00 Pg 0,67,7=1
L32	General Purpose In III on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0010	X5	Aux Clock Output on pin 5, DOUT/MFP2	Pg 0, Reg 53, D(3:1)=011
M5	INT1 output on pin 5, DOUT/MFP2	Pg 0, Reg 53, D(3:1)=100	X11	Aux Clock Output on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=0011
M11	INT1 output on pin 11, MISO/MFP4	Pg 0, Reg 55, D(4:1)=0100	X32	Aux Clock Output on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0100
M32	INT1 output on pin 32, GPIO/MFP5	Pg 0, Reg 52, D(5:2)=0101			

5.3 ANALOG ROUTING

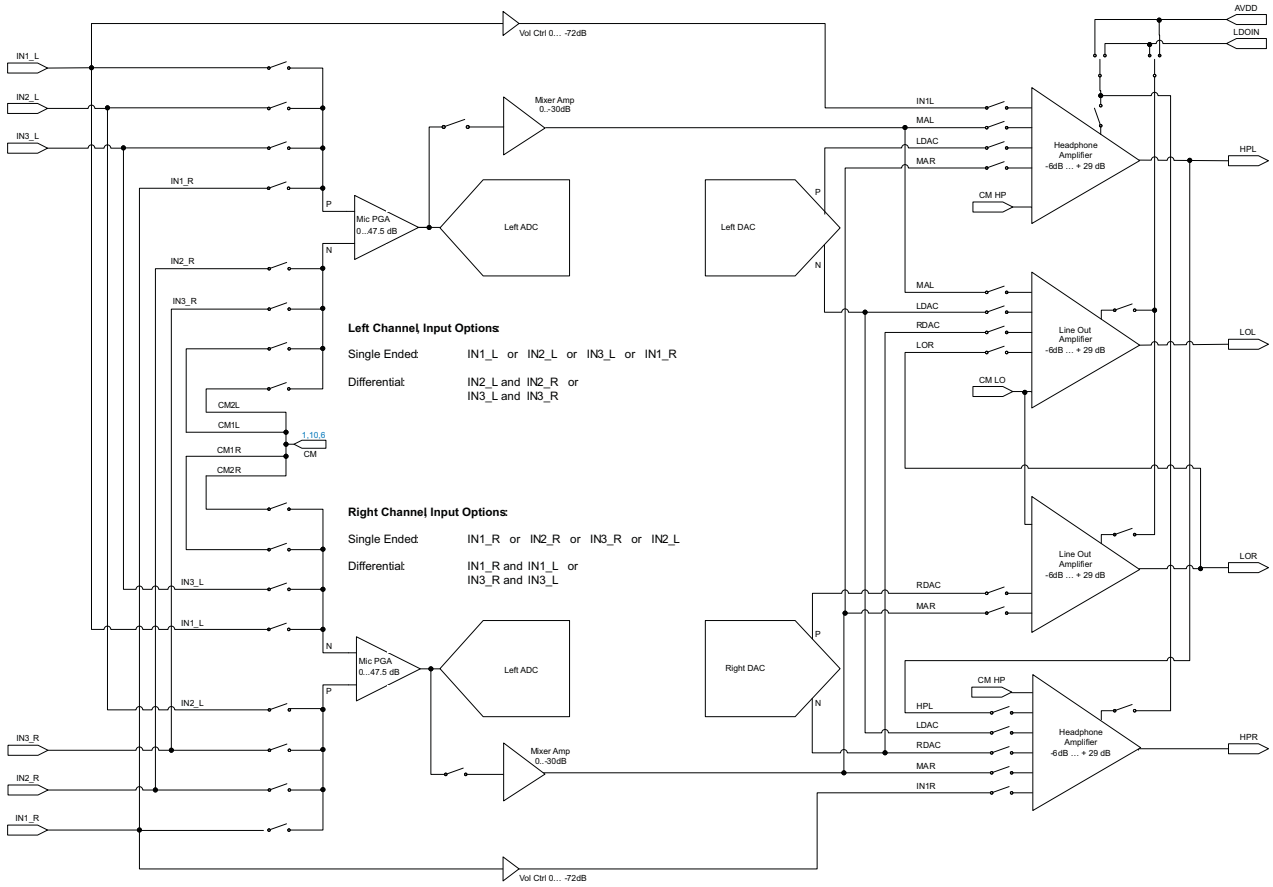


Figure 5-2. Analog Routing Diagram

5.3.1 Analog Low Power Bypass

The TLV320AIC3204 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the left headphone amplifier (HPL) and IN1R to HPR. This is configured on Page 1, Register 12, D(2) for the left channel and Page 1, Register 13, D(2) for the right channel

5.3.2 ADC Bypass Using Mixer Amplifiers

In addition to the low-power bypass mode, there is a bypass mode that uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, microphone-level signals can be amplified and routed to the line or headphone outputs, fully bypassing the ADC and DAC.

To enable this mode, the mixer amplifiers are powered on (Page1, Register 9, D(0:1).

5.4 DEVICE INITIALIZATION

5.4.1 Reset

The TLV320AIC3204 internal logic must be initialized to a known condition for proper device function. To initialize the device in its default operating condition, the hardware reset pin ($\overline{\text{RESET}}$) must be pulled low for at least 10ns. For this initialization to work, both the IOVDD and DVdd supplies must be powered up. It is recommended that while the DVdd supply is being powered up, the $\overline{\text{RESET}}$ pin be pulled low.

The device can also be reset via software reset. Writing '1' into Page 0, Register 1, D(0) resets the device. After a device reset, all registers are initialized with default values as listed in Section 6

5.4.2 Device Startup Lockout Times

After the TLV320AIC3204 is initialized through hardware reset at power-up or software reset, the internal memories is initialized to default values. This initialization takes place within 1ms after pulling the $\overline{\text{RESET}}$ signal high. During this initialization phase no Register read or Register write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

5.4.3 Analog and Reference Startup

The TLV320AIC3204 uses an external REF pin for decoupling the reference voltage used for the data converters and other analog blocks. REF pin requires a minimum 1uF decoupling capacitor from REF to AVss. In order for any analog block to be powered up, the Analog Reference block must be powered up. By default, the Analog Reference block will implicitly be powered up whenever any analog block is powered up, or it can be powered up independently. Detailed descriptions of Analog Reference including fast power-up options are provided in Section 5.19. During the time that the reference block is not completely powered up, subsequent requests for powering up analog blocks (e.g., PLL) are queued, and executed after the reference power up is complete.

5.4.4 PLL Startup

Whenever the PLL is powered up, a startup delay of approx of 10ms is involved after the power up command of the PLL and before the clocks are available to the codec. This delay is to ensure stable operation of PLL and clock-divider logic.

5.5 POWERTUNE

The TLV320AIC3204 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

5.5.1 PowerTune Modes

The TLV320AIC3204 PowerTune modes are called PTM_R1 to PTM_R4 for the recording (ADC) path and PTM_P1 to PTM_P4 for the playback (DAC) path.

5.5.1.1 ADC – Programming PTM_R1 to PTM_R4

The device powers up with PTM_R4 (highest performance) set as default. This mode always works across all combinations of common-mode voltage, chosen processing block, or chosen oversampling ratio. If the application can make use of a lower-power configuration please refer to the ADC and DAC power consumption chapters below for valid combination of PowerTune modes and other device parameters.

The ADC configuration of the PowerTune mode affects right and left channels simultaneously.

	PTM_R1	PTM_R2	PTM_R3	PTM_R4
Pg 1, Reg 61, D(7:0)	0xFF	0xB6	0x64	0x00

5.5.1.2 DAC - Programming PTM_P1 to PTM_P4

On the playback side, the performance is determined by a combination of register settings and the audio data word length applied. For the highest performance setting (PTM_P4), an audio-data word length of 20 bits is required, while for the modes PTM_P1 to PTM_P3 a word length of 16 bits is sufficient.

	PTM_P1	PTM_P2	PTM_P3	PTM_P4
Pg 1, Reg 3, D(4:2)	0x2	0x1	0x0	0x0
Pg 1, Reg 4, D(4:2)	0x2	0x1	0x0	0x0
Audio Data word length	16 bits	16 bits	16 bits	20 or more bits
Pg 0, Reg 27, D(5:4)	0x0	0x0	0x0	0x1, 0x2, 0x3

5.5.1.3 Processing Blocks

The choice of processing blocks, PRB_P1 to PRB_P25 for playback and PRB_R1 to PRB_R18 for recording, also influences the power consumption. In fact, the numerous processing blocks have been implemented to offer a choice between power-optimization and configurations with more signal-processing resources.

5.5.2 ADC Power Consumption

The tables in this section give recommendations for various PowerTune modes. Typical performance and power-consumption values are listed. PowerTune modes that are not supported are marked with an 'X'.

All measurements were taken with the PLL turned off and the ADC configured for single-ended input.

5.5.2.1 ADC, Stereo, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

AOSR = 128, Processing Block = PRB_R1 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	375	375	375	X	500	500	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	–12	0	0	X	–12	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	78.5	90.7	90.2	X	80.4	92.9	92.7	dB
Power consumption	X	11.9	14.2	18.2	X	11.9	14.2	18.2	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R2	A	+1.4
PRB_R3	A	+1.4

5.5.2.2 ADC, Stereo, 48kHz, DVdd = 1.8V, AVdd = 1.8V

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	375	X	X	X	500	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	X	0	X	X	X	0	X	dB full scale
Effective SNR w.r.t. max. allowed input level	86.0	X	88.1	X	X	X	90.4	X	dB
Power consumption	8.4	X	11.4	X	X	X	11.5	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+0.7
PRB_R9	B	+0.7
PRB_R1	A	+2.0
PRB_R2	A	+3.4
PRB_R3	A	+3.4

5.5.2.3 ADC, Stereo, 48kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B), DVdd = 1.26V

	PTM_R1 CM = 0.75V AVdd=1.5V	PTM_R3 CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	0	dB full scale
Effective SNR w.r.t. max. allowed input level	88.0	92.2	dB
Power consumption	6.0	11.4	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+ 0.3
PRB_R9	B	+ 0.3
PRB_R1	A	+ 1.0
PRB_R2	A	+ 1.6
PRB_R3	A	+ 1.6

5.5.2.4 ADC, Mono, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	375	375	375	X	500	500	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	–12	0	0	X	–12	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	78.3	90.8	90.6	X	80.3	92.8	92.7	dB
Power consumption	X	9.1	11.4	15.4	X	9.1	11.4	15.4	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R5	A	+0.7
PRB_R6	A	+0.7

5.5.2.5 ADC, Mono, 48kHz, DVdd = 1.8V, AVdd = 1.8V

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	375	X	X	X	500	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	X	0	X	X	X	0	X	dB full scale
Effective SNR w.r.t. max. allowed input level	86.0	X	88.1	X	X	X	90.3	X	dB
Power consumption	7.0	X	10.1	X	X	X	10.1	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	0
PRB_R12	B	0
PRB_R4	A	+0.7
PRB_R5	A	+1.4
PRB_R6	A	+1.4

5.5.2.6 ADC, Mono, 48 kHz, Lowest Power Consumption,

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B), DVdd = 1.26V

	PTM_R1 CM = 0.75V AVdd=1.5V	PTM_R3 CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	0	dB full scale
Effective SNR w.r.t. max. allowed input level	86.0	90.5	dB
Power consumption	5.1	9.2	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	0
PRB_R12	B	0
PRB_R4	A	+0.3
PRB_R5	A	+0.7
PRB_R6	A	+0.7

5.5.2.7 ADC, Stereo, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

AOSR = 128, Processing Block = PRB_R1 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	91.1	X	X	X	93.2	X	X	X	dB
Power consumption	6.5	X	X	X	6.5	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R2	A	+0.2
PRB_R3	A	+0.2

5.5.2.8 ADC, Stereo, 8kHz, DVdd = 1.8V, AVdd = 1.8V

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	88.2	X	X	X	90.6	X	X	X	dB
Power consumption	6.0	X	X	X	6.1	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+ 0.1
PRB_R9	B	+ 0.1
PRB_R1	A	+ 0.3

Processing Block	Filter	Est. Power Change (mW)
PRB_R2	A	+0.6
PRB_R3	A	+ 0.6

5.5.2.9 ADC, Stereo, 8kHz, Lowest Power Consumption,

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B), PowerTune Mode = PTM_R1, DVdd = 1.26

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	88.3	92.4	dB
Power consumption	4.7	5.8	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+ 0.1
PRB_R9	B	+ 0.1
PRB_R1	A	+ 0.2
PRB_R2	A	+ 0.3
PRB_R3	A	+ 0.3

5.5.2.10 ADC, Mono, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	88.5	X	X	X	93.3	X	X	X	dB
Power consumption	5.5	X	X	X	5.6	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R5	A	+0.1
PRB_R6	A	+0.1

5.5.2.11 ADC, Mono, 8kHz, DVdd = 1.8V, AVdd = 1.8V

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	88.1	X	X	X	93.0	X	X	X	dB
Power consumption	5.3	X	X	X	5.3	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	0
PRB_R12	B	0
PRB_R4	A	+0.1
PRB_R5	A	+0.2
PRB_R6	A	+0.2

5.5.2.12 ADC, Mono, 8kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B), PowerTune Mode = PTM_R1, DVdd = 1.26V

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	88.2	89.9	dB
Power consumption	4.2	5.0	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	0
PRB_R12	B	0
PRB_R4	A	+0.1
PRB_R5	A	+0.1
PRB_R6	A	+0.1

5.5.2.13 ADC, Stereo, 192kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

AOSR = 32, Processing Block = PRB_R14 (Decimation Filter C)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	X	X	375	X	X	X	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	X	X	0	X	X	X	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	X	X	86.5	X	X	X	88.7	dB
Power consumption	X	X	X	21.9	X	X	X	21.9	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R13	C	–2.7
PRB_R15	C	0

5.5.2.14 ADC, Stereo, 192kHz, Lowest Power Consumption

AOSR = 32, Processing Block = PRB_R14 (Decimation Filter C), PowerTune Mode = PTM_R4, DVdd = 1.26V

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	86.5	89.0	dB
Power consumption	16.2	18.4	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R13	C	– 1.3
PRB_R15	C	0

5.5.3 DAC Power Consumption

The tables in this section give recommendations for various DAC PowerTune modes. Typical performance and power-consumption numbers are listed. PowerTune modes which are not supported are marked with an 'X'.

All measurements were taken with the PLL turned off, no signal is present, and the DAC modulator is fully running.

5.5.3.1 DAC, Stereo, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 128, Processing Block = PRB_P8 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale(1)		75	225	375	375	100	300	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.7	94.1	98.9	99.0	90.5	96.3	100.0	100.0	dB
	Power consumption	9.4	10.1	10.9	10.9	9.5	10.1	10.9	10.9	mW
Line out	Effective SNR w.r.t. 0dB full scale	88.7	94.1	98.9	99.0	90.5	96.3	100.0	100.0	dB
	Power consumption	7.7	8.4	9.1	9.1	7.7	8.4	9.1	9.2	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	0
PRB_P2	A	+3.1
PRB_P3	A	+1.6
PRB_P7	B	–1.6
PRB_P9	B	0
PRB_P10	B	+1.6
PRB_P11	B	–0.8
PRB_P23	A	0
PRB_P24	A	+3.1
PRB_P25	A	+3.1

5.5.3.2 DAC, Stereo, 48kHz, Lowest Power Consumption

DOSR = 64, Interpolation Filter B, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V PRB_P8 PTM_P1	CM = 0.9V AVdd=1.8V PRB_P8 PTM_P1	CM = 0.75V AVdd=1.5V PRB_P7 PTM_P4	UNIT
0dB full scale(1)		75	100	375	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	89.4	89.4	99.9	dB
	Power consumption	5.5	6.9	7.1	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.5	91.2	100.1	dB
	Power consumption	4.2	4.1	5.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)(1)
PRB_P1	A	0
PRB_P2	A	+1.5
PRB_P3	A	+0.8
PRB_P7	B	–0.8
PRB_P9	B	0
PRB_P10	B	+0.8
PRB_P11	B	0
PRB_P23	A	0
PRB_P24	A	+1.5
PRB_P25	A	+1.5

(1) Estimated power change is w.r.t. PRB_P8.

5.5.3.3 DAC, Mono, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 128, Processing Block = PRB_P13 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale(1)		75	225	375	375	100	300	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.1	96.1	98.7	99.5	90.4	96.3	99.4	100	dB
	Power consumption	5.8	6.2	6.5	6.5	5.8	6.2	6.5	6.5	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.6	97.1	100.3	100.3	90.5	96.3	100	100	dB
	Power consumption	5.0	5.4	5.7	5.7	5.0	5.4	5.7	5.7	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change(mW)
PRB_P4	A	0
PRB_P5	A	+1.6
PRB_P6	A	+1.6
PRB_P12	B	–0.8
PRB_P14	B	0
PRB_P15	B	+1.6
PRB_P16	B	0

5.5.3.4 DAC, Mono, 48kHz, Lowest Power Consumption

DOSR = 64, Processing Block = PRB_P13 (Interpolation Filter B), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale(1)		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.9	90.8	dB
	Power consumption	3.4	3.8	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.5	91.1	dB
	Power consumption	3.0	3.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P4	A	0
PRB_P5	A	+0.8
PRB_P6	A	+0.8
PRB_P12	B	–0.4
PRB_P14	B	0
PRB_P15	B	+0.8
PRB_P16	B	0

5.5.3.5 DAC, Stereo, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 768, Processing Block = PRB_P7 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale		75	X	X	X	100	X	X	X	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale(1)	88.7	X	X	X	90.5	X	X	X	dB
	Power consumption	6.1	X	X	X	6.1	X	X	X	mW
Line out	Effective SNR w.r.t. 0dB full scale	88.7	X	X	X	90.5	X	X	X	dB
	Power consumption	3.6	X	X	X	4.3	X	X	X	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.3
PRB_P2	A	+0.8
PRB_P3	A	+0.5
PRB_P8	B	+0.3
PRB_P9	B	+0.3
PRB_P10	B	+0.5
PRB_P11	B	+0.3
PRB_P23	A	+0.3
PRB_P24	A	+0.8
PRB_P25	A	+0.8

5.5.3.6 DAC, Stereo, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P7 (Interpolation Filter B), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale(1)		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.4	90.2	dB
	Power consumption	3.8	5.1	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.6	91.1	dB
	Power consumption	2.4	2.9	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.1
PRB_P2	A	+0.4
PRB_P3	A	+0.3
PRB_P8	B	+0.1
PRB_P9	B	+0.1
PRB_P10	B	+0.3
PRB_P11	B	+0.1
PRB_P23	A	+0.1
PRB_P24	A	+0.4
PRB_P25	A	+0.4

5.5.3.7 DAC, Mono, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 768, Processing Block = PRB_P4 (Interpolation Filter A)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale(1)		75	X	X	X	100	X	X	X	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	89.4	X	X	X	89.8	X	X	X	dB
	Power consumption	4.4	X	X	X	4.4	X	X	X	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.6	X	X	X	91.2	X	X	X	dB
	Power consumption	3.6	X	X	X	3.6	X	X	X	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.3
PRB_P6	A	+0.3
PRB_P12	B	–0.1
PRB_P13	B	0
PRB_P14	B	0
PRB_P15	B	+0.3
PRB_P16	B	0

5.5.3.8 DAC, Mono, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P4 (Interpolation Filter A), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale(1)		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	89.1	90.7	dB
	Power consumption	2.6	3.0	mW
Line out	Effective SNR w.r.t. 0dB full scale	89.5	91.1	dB
	Power consumption	2.0	2.2	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.1
PRB_P6	A	+0.1
PRB_P12	B	–0.1
PRB_P13	B	0
PRB_P14	B	0
PRB_P15	B	+0.1
PRB_P16	B	0

5.5.3.9 DAC, Stereo, 192kHz, DVdd = 1.8V, AVdd = 1.8V

DOSR = 32, Processing Block = PRB_P17 (Interpolation Filter C)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale(1)		X	X	X	375	X	X	X	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	X	X	X	99.1	X	X	X	99.9	dB
	Power consumption	X	X	X	13.4	X	X	X	13.5	mW
Line out	Effective SNR w.r.t. 0dB full scale	X	X	X	100.5	X	X	X	100.5	dB
	Power consumption	X	X	X	11.3	X	X	X	11.3	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+9.3
PRB_P19	C	+3.1

5.5.3.10 DAC, Stereo, 192kHz, Lowest Power Consumption

DOSR = 16, Processing Block = PRB_R17 (Interpolation Filter C), PowerTune Mode = PTM_P4, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale(1)		375	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	99.4	100.3	dB
	Power consumption	7.7	8.9	mW
Line out	Effective SNR w.r.t. 0dB full scale	100.4	100.4	dB
	Power consumption	6.1	6.7	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 5.13.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+4.5
PRB_P19	C	+1.5

5.6 ADC

5.6.1 Concept

The TLV320AIC3204 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo ADC can be powered up one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully powered or entirely powered down. Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog anti-aliasing filtering are very relaxed. The TLV320AIC3204 integrates a second order analog anti-aliasing filter with 28-dB attenuation at 6MHz. This filter, combined with the digital decimation filter, provides sufficient anti-aliasing filtering without requiring additional external components.

5.6.2 Routing

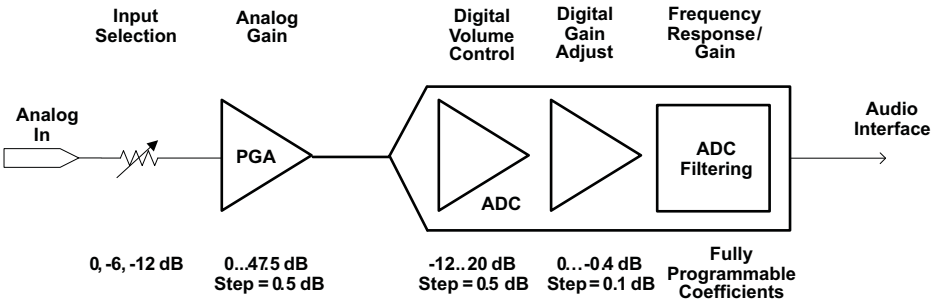
As shown in Figure 5-2, the TLV320AIC3204 includes six analog inputs which can be configured as either 3 stereo single-ended pairs or 3 fully-differential pairs. These pins connect through series resistors and switches to the virtual ground terminals of two fully-differential amplifiers (one per ADC/PGA channel). By turning on only one set of switches per amplifier at a time, the inputs can be effectively multiplexed to each ADC PGA channel. By turning on multiple sets of switches per amplifier at a time, audio sources can be mixed. The TLV320AIC3204 supports the ability to mix up to four single-ended analog inputs or up to two fully-differential analog inputs into each ADC PGA channel.

In most applications, high input impedance is desired for analog inputs. However when used in conjunction with high gain as in the case of microphone inputs, the higher input impedance results in higher noise or lower dynamic range. The TLV320AIC3204 allows the user the flexibility of choosing the input impedance from 10kΩ, 20kΩ and 40kΩ. When multiple inputs are mixed together, by choosing different input impedances, level adjustment can be achieved. For example, if one input is selected with 10kΩ input impedance and the second input is selected with 20kΩ input impedance, then the second input is attenuated by half as compared to the first input. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting.

Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the system designer is advised to take adequate precautions to avoid such a saturation from occurring. In general, the mixed signal should not exceed 0dB.

Typically, voice or audio signal inputs are capacitively coupled to the device. This allows the device to independently set the common mode of the input signals to values chosen by register control of Page 1, Register 10, D(6) to either 0.9V or 0.75V. The correct value maximizes the dynamic range across the entire analog-supply range. Failure to capacitively connect the input to the device can cause high offset due to mismatch in source common-mode and device common-mode setting. In extreme cases it could also saturate the analog channel, causing distortion.

5.7 ADC Gain Setting



When the gain of the ADC Channel is kept at 0dB and the common mode set to 0.75V, a single-ended input of $0.375V_{RMS}$ results in a full-scale digital signal at the output of ADC channel. Similarly, when the gain is kept at 0dB, and common mode is set to 0.9V, a single-ended input of $0.5V_{RMS}$ results in a full-scale digital signal at the output of the ADC channel. However various block functions control the gain through the channel. The gain applied by the PGA is described in Table 5-1. Additionally, the digital volume control adjusts the gain through the channel as described in Section 5.7.2. A finer level of gain is controlled by fine gain control as described in Section 5.7.3. The decimation filters A, B and C along with the delta-sigma modulator contribute to a DC gain of 1.0 through the channel.

5.7.1 Analog Programmable Gain Amplifier (PGA)

The TLV320AIC3204 features a built-in low-noise PGA for boosting low-level signals, such as direct microphone inputs, to full-scale to achieve high SNR. This PGA can provide a gain in the range of 0dB to 47.5dB for single-ended inputs or 6dB to 53.5dB for fully-differential inputs (gain calculated w.r.t. input impedance setting of 10kΩ, 20kΩ input impedance will result in 6dB lower and 40kΩ will result in 12dB lower gain). This gain can be user controlled by writing to Page 1, Register 59 and Page 1, Register 60. In the AGC mode this gain can also be automatically controlled by the built-in hardware AGC.

Table 5-1. Analog PGA vs Input Configuration

Page 1, Register 59, D(6:0) Page 1, Register 60, D(6:0)	EFFECTIVE GAIN APPLIED BY PGA					
	SINGLE-ENDED			DIFFERENTIAL		
	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K
000 0000	0 dB	–6 dB	-12 dB	6.0 dB	0 dB	–6.0 dB
000 0001	0.5 dB	–5.5 dB	–11.5 dB	6.5 dB	0.5 dB	-5.5 dB
000 0010	1.0 dB	–5.0 dB	–11.0 dB	7.0 dB	7.5 dB	–5.0 dB
…	…	…	…	…	…	…
101 1110	47.0 dB	41.0 dB	35.0 dB	53.0 dB	47.0 dB	41.0 dB
101 1111	47.5 dB	41.5 dB	35.5 dB	53.5 dB	47.5 dB	41.5 dB

The gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register value (see registers Page 0, Reg 81, D(1:0)). This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and at power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag Page 0, Reg 36, D(7) and D(3) is set whenever the gain applied by the PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming Page 0, Reg 81, D(1:0).

5.7.2 Digital Volume Control

The TLV320AIC3204 also has a digital volume-control block with a range from -12dB to +20dB in steps of 0.5dB. It is set by programming Page 0, Register 83 and 84 respectively for left and right channels.

Table 5-2. Digital Volume Control for ADC

Desired Gain dB	Left / Right Channel Page 1, Register 83/84, D(6:0)
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (Default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, the soft-stepping feature is used to avoid audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured via Page 1, Register 81, D(1:0), and is common to soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to -12.0dB before powering down. Due to the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320AIC3204 gives feedback to the user, through read-only flags Page 1, Reg 36, D(7) for Left Channel and Page 1, Reg 36, D(3) for the right channel.

5.7.3 Fine Digital Gain Adjustment

Additionally, the gains in each of the channels is finely adjustable in steps of 0.1dB. This is useful when trying to match the gain between channels. By programming Page 0, Register 82 the gain can be adjusted from 0dB to -0.4dB in steps of 0.1dB. This feature, in combination with the regular digital volume control allows the gains through the left and right channels be matched in the range of -0.5dB to +0.5dB with a resolution of 0.1dB.

5.7.4 AGC

The TLV320AIC3204 includes Automatic Gain Control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack

and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Since the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

- **Target Level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC3204 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the TLV320AIC3204 reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.
- **Attack Time** determines how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. Wide range of attack time programmability is supported in terms of number of samples (i.e. number of ADC sample frequency clock cycles).
- **Decay Time** determines how quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. Wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample frequency clock cycles).
- **Gain Hysteresis** is the hysteresis applied to the required gain calculated by the AGC function while changing its mode of operation from attack to decay or vice-versa. For example, while attacking the input signal, if the current applied gain by the AGC is x dB, and suddenly because of input level going down, the new calculated required gain is y dB, then this gain is applied provided y is greater than x by the value set in Gain Hysteresis. This feature avoids the condition when the AGC function can fluctuate between a very narrow band of gains leading to audible artifacts. The Gain Hysteresis can be adjusted or disabled by the user.
- **Noise threshold** determines the level below which if the input signal level falls, the AGC considers it as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise is not 'gained up' in the absence of speech. Noise threshold level in the AGC algorithm is programmable from -30dB to -90 dB of full-scale. When AGC Noise Threshold is set to –70dB, –80db, or –90dB, the microphone input Max PGA applicable setting must be greater than or equal to 11.5dB, 21.5dB, or 31.5dB respectively. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. The noise (or silence) detection feature can be entirely disabled by the user.
- **Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA can be programmed from 0 dB to 63.5 dB in steps of 0.5 dB.
- **Hysteresis**, as the name suggests, determines a window around the Noise Threshold which must be exceeded to either detect that the recorded signal is indeed noise or signal. If initially the energy of the recorded signal is greater than the Noise Threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the Noise Threshold by a value given by Hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the Noise Threshold by a value given by the Hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is very close to the Noise threshold) a non-zero hysteresis value should be chosen. The Hysteresis feature can also be disabled.
- **Debounce Time (Noise and Signal)** determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set Noise Threshold, then the AGC does not increase the input gain to achieve the Target Level. However, to handle audible artifacts which can occur when the energy of the input signal is very close to the Noise Threshold, the AGC checks if the energy of the recorded signal is less than the Noise Threshold for a time greater than the Noise Debounce Time. Similarly the AGC starts increasing the input-signal gain to reach the Target Level when the calculated energy of the input signal is greater

than the Noise Threshold. Again, to avoid audible artifacts when the input-signal energy is very close to Noise Threshold, the energy of the input signal needs to continuously exceed the Noise Threshold value for the Signal Debounce Time. If the debounce times are kept very small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the Debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to Noise Threshold. Both noise and signal debounce time can be disabled.

- The **AGC Noise Threshold Flag** is a read-only flag indicating that the input signal has levels lower than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.
- **Gain Applied by AGC** is a ready-only register setting which gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This, along with the Target Setting, can be used to determine the input signal level. In a steady state situation
  Target Level (dB) = Gain Applied by AGC (dB) + Input Signal Level (dB)
  When the AGC noise threshold flag is set, then the status of gain applied by AGC should be ignored.
- The **AGC Saturation Flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
- The **ADC Saturation Flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.
- An **AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low pass filter is in the form of a first-order IIR filter. Three 8-bit registers are used to form the 24-bit digital coefficient as shown on the register map. In this way, a total of 9 registers are programmed to form the 3 IIR coefficients. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (5\text{-}1)$$

Where:

Coefficient N0 can be programmed by writing into Page 8, Register 12, 13 and 14.
Coefficient N1 can be programmed by writing into Page 8, Register 16, 17 and 18.
Coefficient D1 can be programmed by writing into Page 8, Register 20, 21 and 22.
N0, N1 and D1 are 24-bit 2's complement numbers and their default values implement a low-pass filter with cut-off at 0.002735*ADC_FS .

See Table 5-3 for various AGC programming options. AGC can be used only if analog microphone input is routed to the ADC channel.

Table 5-3. AGC Parameter Settings

Function	Control Register Left ADC	Control Register Right ADC	Bit
AGC enable	Page 0, Register 86	Page 0,Register 94	D(7)
Target Level	Page 0, Register 86	Page 0, Register 94	D(6:4)
Gain Hysteresis	Page 0, Register 86	Page 0, Register 94	D(1:0)
Hysteresis	Page 0, Register 87	Page 0, Register 95	D(7:6)
Noise threshold	Page 0, Register 87	Page 0, Register 95	D(5:1)
Max PGA applicable	Page 0, Register 88	Page 0, Register 96	D(6:0)
Time constants (attack time)	Page 0, Register 89	Page 0, Register 97	D(7:0)
Time constants(decay time)	Page 0, Register 90	Page 0, Register 98	D(7:0)

Table 5-3. AGC Parameter Settings (continued)

Function	Control Register Left ADC	Control Register Right ADC	Bit
Debounce time (Noise)	Page 0, Register 91	Page 0, Register 99	D(4:0)
Debounce time (Signal)	Page 0, Register 92	Page 0, Register 100	D(3:0)
Gain applied by AGC	Page 0, Register 93	Page 0, Register 101	D(7:0) (Read Only)
AGC Noise Threshold Flag	Page 0, Register 45 (sticky flag), Page 0, Register 47 (non-sticky flag)	Page 0, Register 45 (sticky flag), Page 0, Register 47 (non-sticky flag)	D(6:5) (Read Only)
AGC Saturation flag	Page 0, Register 36 (sticky flag)	Page 0, Register 36 (sticky flag)	D(5), D(1) (Read Only)
ADC Saturation flag	Page 0, Register 42 (sticky flag), Page 0, Register 43 (non-sticky flag)	Page 0, Register 42 (sticky flag), Page 0, Register 43 (non-sticky flag)	D(3:2) (Read Only)

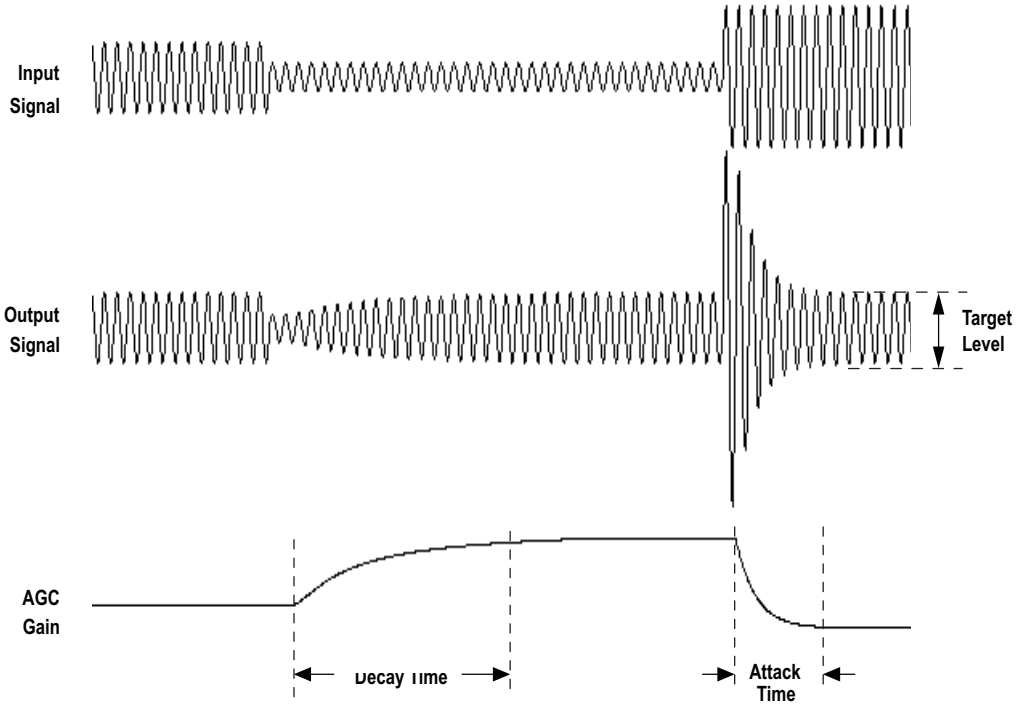


Figure 5-3. AGC Characteristics

5.8 ADC Decimation Filtering and Signal Processing

The TLV320AIC3204 ADC channel includes a built-in digital decimation filter to process the oversampled data from the sigma-delta modulator to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

5.8.1 Processing Blocks

The TLV320AIC3204 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. Table 5-4 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

Table 5-4. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Right	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

5.8.2 Processing Blocks – Details

5.8.2.1 1st order IIR, AGC, Filter A

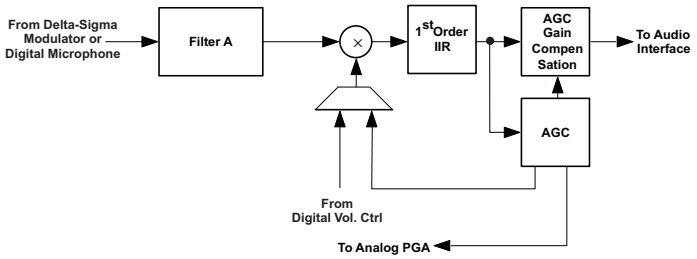


Figure 5-4. Signal Chain for PRB_R1 and PRB_R4

5.8.2.2 5 Biquads, 1st order IIR, AGC, Filter A

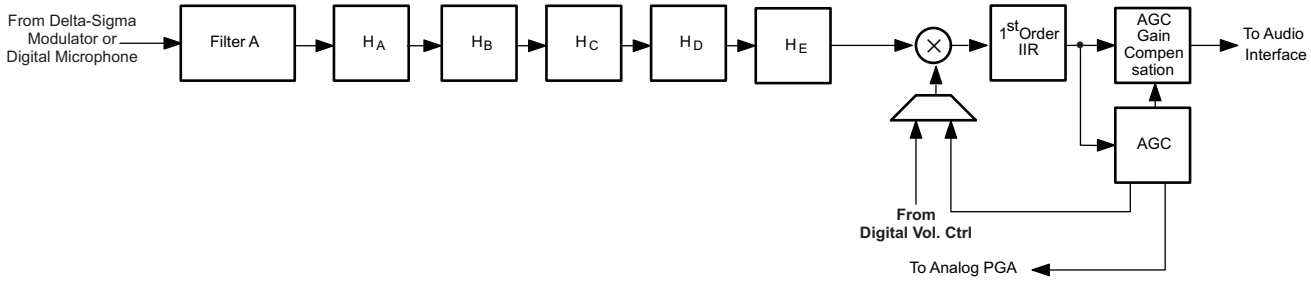


Figure 5-5. Signal Chain PRB_R2 and PRB_R5

5.8.2.3 25 Tap FIR, 1st order IIR, AGC, Filter A

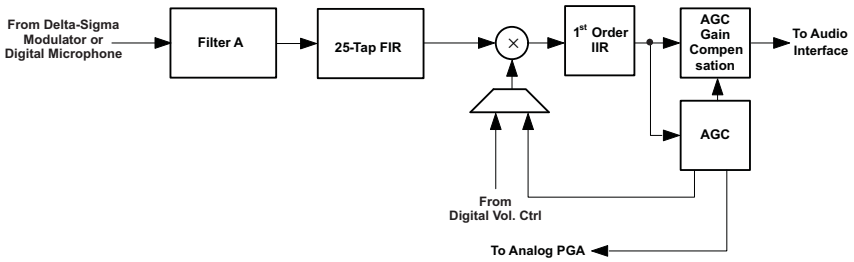


Figure 5-6. Signal Chain for PRB_R3 and PRB_R6

5.8.2.4 1st order IIR, AGC, Filter B

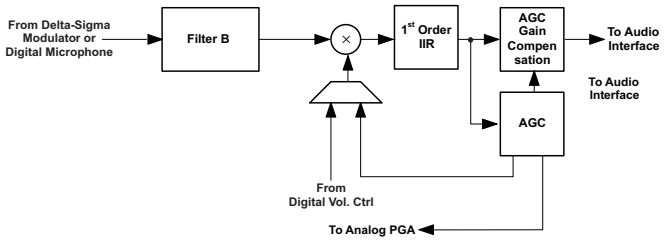


Figure 5-7. Signal Chain for PRB_R7 and PRB_R10

5.8.2.5 3 Biquads, 1st order IIR, AGC, Filter B

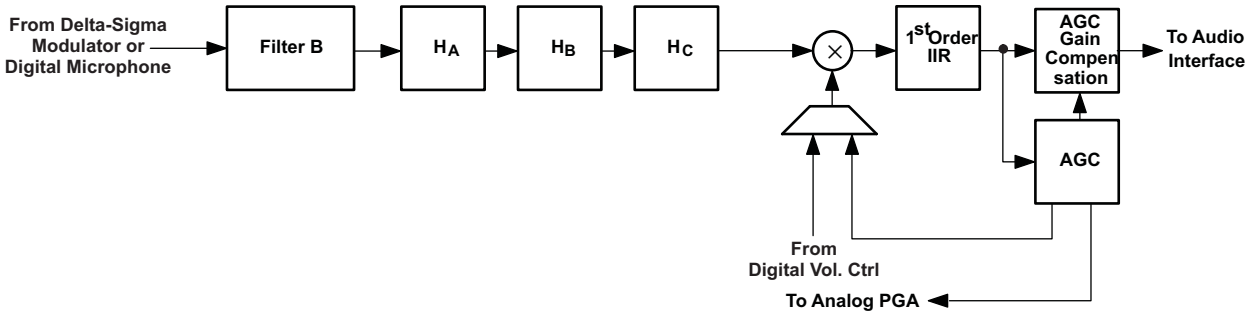


Figure 5-8. Signal Chain for PRB_R8 and PRB_R11

5.8.2.6 20 Tap FIR, 1st order IIR, AGC, Filter B

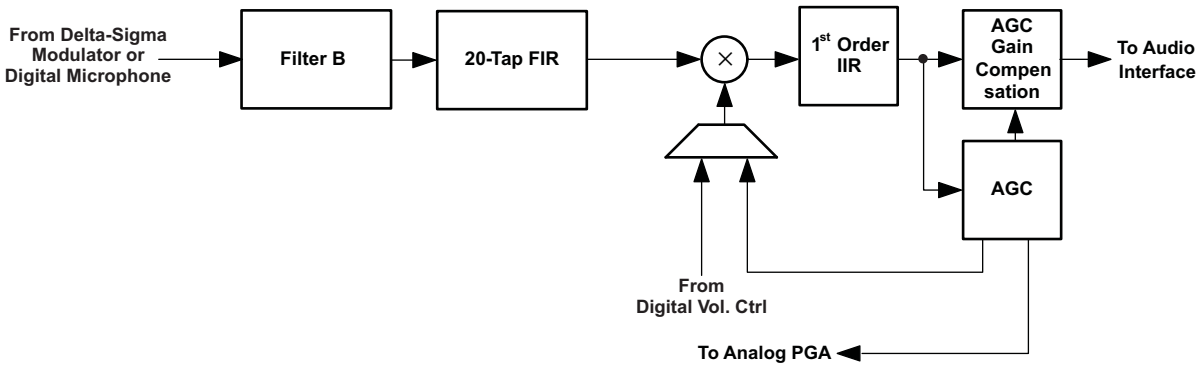


Figure 5-9. Signal Chain for PRB_R9 and PRB_R12

5.8.2.7 1st order IIR, AGC, Filter C

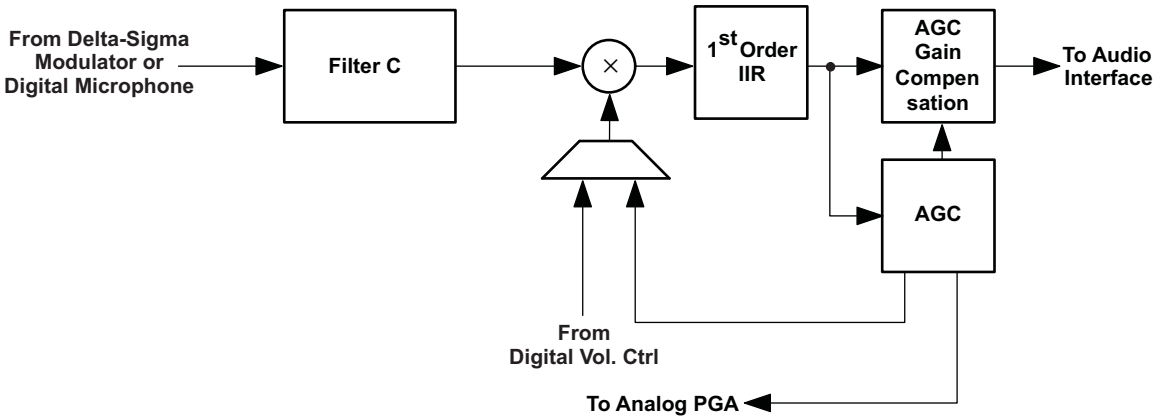


Figure 5-10. Signal Chain for PRB_R13 and PRB_R16

5.8.2.8 5 Biquads, 1st order IIR, AGC, Filter C

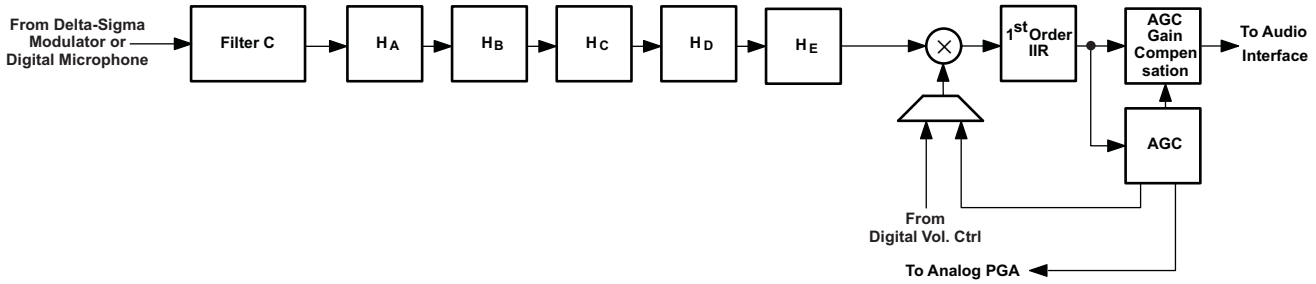


Figure 5-11. Signal Chain for PRB_R14 and PRB_R17

5.8.2.9 25 Tap FIR, 1st order IIR, AGC, Filter C

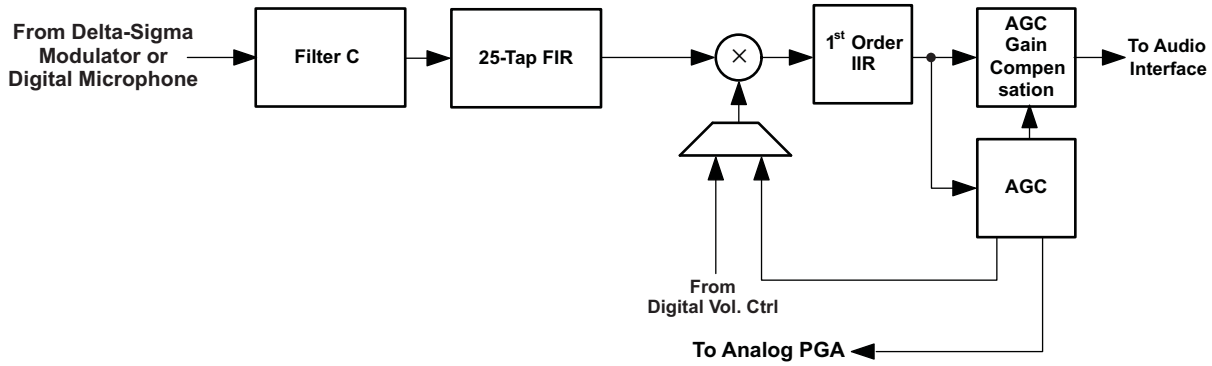


Figure 5-12. Signal for PRB_R15 and PRB_R18

5.8.3 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A 1st-order IIR filter is always available, and is useful to efficiently filter out possible DC components of the signal. Up to 5 biquad section or alternatively up to 25-tap FIR filters are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering see Section 5.9.7 below.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see .

5.8.3.1 1st Order IIR Section

The transfer function for the first order IIR Filter is give by ***[equation not in source]***

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (5\text{-}2)$$

The frequency response for the 1st order IIR Section with default coefficients is flat at a gain of 0dB.

Table 5-5. ADC 1st order IIR Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
1st Order IIR	N0	C4 (Pg 8,Reg 24,25,26)	C36 (Pg 9,Reg 32,33,34)
	N1	C5 (Pg 8,Reg 28,29,30)	C37 (Pg 9,Reg 36,37,38)
	D1	C6 (Pg 8,Reg 32,33,34)	C39 (Pg 9,Reg 40,41,42)

5.8.3.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2*N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2*D_1 z^{-1} - D_2 z^{-2}} \quad (5\text{-}3)$$

The frequency response for each of the biquad section with default coefficients is flat at a gain of 0dB.

Table 5-6. ADC Biquad Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
BIQUAD A	N0	C7 (Pg 8, Reg 36,37,38)	C39 (Pg 9, Reg 44,45,46)
	N1	C8 (Pg 8, Reg 40,41,42)	C40 (Pg 9, Reg 48,49,50)
	N2	C9 (Pg 8, Reg 44,45,46)	C41 (Pg 9, Reg 52,53,54)
	D1	C10 (Pg 8, Reg 48,49,50)	C42 (Pg 9, Reg 56,57,58)
	D2	C11 (Pg 8, Reg 52,53,54)	C43 (Pg 9, Reg 60,61,62)
BIQUAD B	N0	C12 (Pg 8, Reg 56,57,58)	C44 (Pg 9, Reg 64,65,66)
	N1	C13 (Pg 8, Reg 60,61,62)	C45 (Pg 9, Reg 68,69,70)
	N2	C14 (Pg 8, Reg 64,65,66)	C46 (Pg 9, Reg 72,73,74)
	D1	C15 (Pg 8, Reg 68,69,70)	C47 (Pg 9, Reg 76,77,78)
	D2	C16 (Pg 8, Reg 72,73,74)	C48 (Pg 9, Reg 80,81,82)
BIQUAD C	N0	C17 (Pg 8, Reg 76,77,78)	C49 (Pg 9, Reg 84,85,86)
	N1	C18 (Pg 8, Reg 80,81,82)	C50 (Pg 9, Reg 88,89,90)
	N2	C19 (Pg 8, Reg 84,85,86)	C51 (Pg 9, Reg 92,93,94)
	D1	C20 (Pg 8, Reg 88,89,90)	C52 (Pg 9, Reg 96,97,98)
	D2	C21 (Pg 8, Reg 92,93,94)	C53 (Pg 9, Reg 100,101,102)
BIQUAD D	N0	C22 (Pg 8, Reg 96,97,98)	C54 (Pg 9, Reg 104,105,106)
	N1	C23 (Pg 8, Reg 100,101,102)	C55 (Pg 9, Reg 108,109,110)
	N2	C24 (Pg 8, Reg 104,105,106)	C56 (Pg 9, Reg 112,113,114)
	D1	C25 (Pg 8, Reg 108,109,110)	C57 (Pg 9, Reg 116,117,118)
	D2	C26 (Pg 8, Reg 112,113,114)	C58 (Pg 9, Reg 120,121,122)
BIQUAD E	N0	C27 (Pg 8, Reg 116,117,118)	C59 (Pg 9, Reg 124,125,126)
	N1	C28 (Pg 8, Reg 120,121,122)	C60 (Pg 10, Reg 8,9,10)
	N2	C29 (Pg 8, Reg 124,125,126)	C61 (Pg 10, Reg 12,13,14)
	D1	C30 (Pg 9, Reg 8,9,10)	C62 (Pg 10, Reg 16,17,18)
	D2	C31 (Pg 9, Reg 12,13,14)	C63 (Pg 10, Reg 20,21,22)

5.8.3.3 FIR Section

Six of the available ADC processing blocks offer FIR filters for signal processing. PRB_R9 and PRB_R12 feature a 20-tap FIR filter while the processing blocks PRB_R3, PRB_R6, PRB_R15 and PRB_R18 feature a 25-tap FIR filter

$$H(z) = \sum_{n=0}^{M} Fir_n z^{-n}$$

$$M = 24, \text{for PRB\_R3, PRB\_R6, PRB\_R15 and PRB\_R18}$$

$$M = 19, \text{for PRB\_R9 and PRB\_R12} \quad (5\text{-}4)$$

The coefficients of the FIR filters are 24-bit 2's complement format and correspond to the ADC coefficient space as listed below. There is no default transfer function for the FIR filter. When the FIR filter gets used all applicable coefficients must be programmed.

Table 5-7. ADC FIR Filter Coefficients

Filter	FIlter Coefficient Left ADC Channel	Filter Coefficient Right ADC Channel
Fir0	C7 (Pg 8, Reg 36,37,38)	C39 (Pg 9, Reg 44,45,46)
Fir1	C8 (Pg 8, Reg 40,41,42)	C40 (Pg 9, Reg 48,49,50)
Fir2	C9 (Pg 8, Reg 44,45,46)	C41 (Pg 9, Reg 52,53,54)
Fir3	C10 (Pg 8, Reg 48,49,50)	C42 (Pg 9, Reg 56,57,58)
Fir4	C11 (Pg 8, Reg 52,53,54)	C43 (Pg 9, Reg 60,61,62)
Fir5	C12 (Pg 8, Reg 56,57,58)	C44 (Pg 9, Reg 64,65,66)
Fir6	C13 (Pg 8, Reg 60,61,62)	C45 (Pg 9, Reg 68,69,70)
Fir7	C14 (Pg 8, Reg 64,65,66)	C46 (Pg 9, Reg 72,73,74)
Fir8	C15 (Pg 8, Reg 68,69,70)	C47 (Pg 9, Reg 76,77,78)
Fir9	C16 (Pg 8, Reg 72,73,74)	C48 (Pg 9, Reg 80,81,82)
Fir10	C17 (Pg 8, Reg 76,77,78)	C49 (Pg 9, Reg 84,85,86)
Fir11	C18 (Pg 8, Reg 80,81,82)	C50 (Pg 9, Reg 88,89,90)
Fir12	C19 (Pg 8, Reg 84,85,86)	C51 (Pg 9, Reg 92,93,94)
Fir13	C20 (Pg 8, Reg 88,89,90)	C52 (Pg 9, Reg 96,97,98)
Fir14	C21 (Pg 8, Reg 92,93,94)	C53 (Pg 9, Reg 100,101,102)
Fir15	C22 (Pg 8, Reg 96,97,98)	C54 (Pg 9, Reg 104,105,106)
Fir16	C23 (Pg 8, Reg 100,101,102)	C55 (Pg 9, Reg 108,109,110)
Fir17	C24 (Pg 8, Reg 104,105,106)	C56 (Pg 9, Reg 112,113,114)
Fir18	C25 (Pg 8, Reg 108,109,110)	C57 (Pg 9, Reg 116,117,118)
Fir19	C26 (Pg 8, Reg 112,113,114)	C58 (Pg 9, Reg 120,121,122)
Fir20	C27 (Pg 8, Reg 116,117,118)	C59 (Pg 9, Reg 124,125,126)
Fir21	C28 (Pg 8, Reg 120,121,122)	C60 (Pg 10, Reg 8,9,10)
Fir22	C29 (Pg 8, Reg 124,125,126)	C61 (Pg 10, Reg 12,13,14)
Fir23	C30 (Pg 9, Reg 8,9,10)	C62 (Pg 10, Reg 16,17,18)
Fir24	C31 (Pg 9, Reg 12,13,14)	C63 (Pg 10, Reg 20,21,22)

5.8.4 Decimation Filter

The TLV320AIC3204 offers 3 different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR*Fs to the final output sampling rate of Fs. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B and C.

5.8.4.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance the oversampling ratio must be set to 128. Please also refer to the PowerTune chapter for details on performance and power in dependency of AOSR.

Filter A can also be used for 96kHz at an AOSR of 64.

Table 5-8. ADC Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…64Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…32Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.1	dB

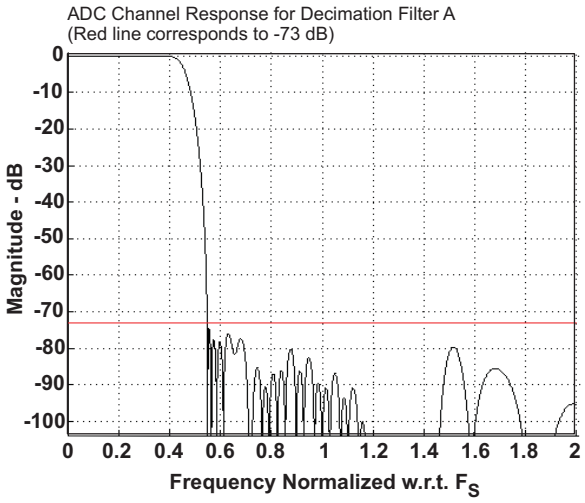


Figure 5-13. ADC Decimation Filter A, Frequency Response

5.8.4.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96kHz at a oversampling ratio of 64.

Table 5-9. ADC Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39Fs	±0.077	dB
Filter Gain Stop Band	0.60Fs…32Fs	–46	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39Fs	0.076	dB
Pass Band Ripple, 44.1 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.11	dB

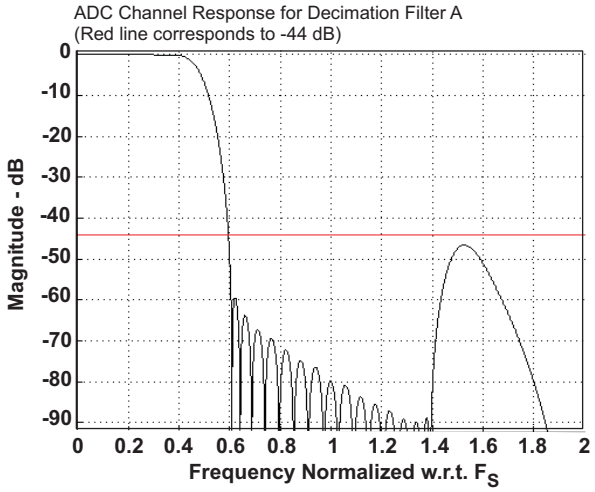


Figure 5-14. ADC Decimation Filter B, Frequency Response

5.8.4.3 Decimation Filter C

Filter type C along with AOSR of 32 is specially designed for 192ksps operation for the ADC. The pass band which extends up to 0.11*Fs (corresponds to 21kHz), is suited for audio applications.

Table 5-10. ADC Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11Fs	0…0.11Fs	±0.033	dB
Filter Gain from 0.28Fs to 16Fs	0.28Fs…16Fs	–60	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 44.1 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 192 ksps	0…20kHz	0.086	dB

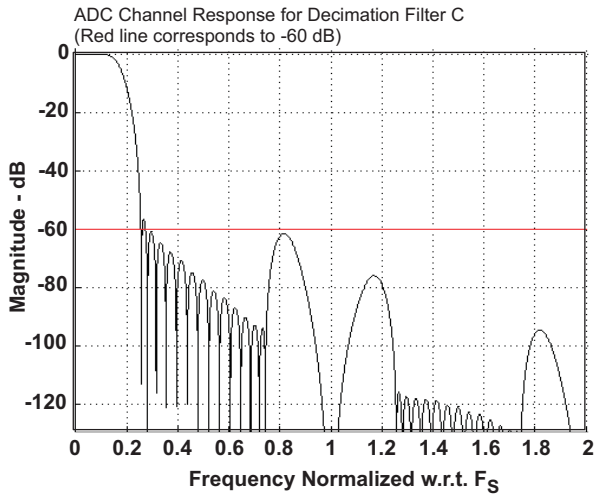


Figure 5-15. ADC Decimation Filter C, Frequency Response

5.8.5 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface once every cycle of Fs,ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

5.9 ADC Special Functions

5.9.1 Microphone Bias

The TLV320AIC3204 has a built-in low noise Microphone Bias support for electret-condenser microphones. The Bias amplifier can support up to 3mA of load current to support multiple microphones. The Bias amplifier has been designed to provide a combination of high PSRR, low noise and programmable bias voltages to allow the user to fine tune the biasing to specific microphone combinations. To support a wide range of bias voltages, the bias amplifier can work of either a low analog supply or high LDOIN supply.

Table 5-11. MICBIAS Voltage Control

Page 1, Reg 51, D(5:4)	Page 1, Reg 10, D(6)	Page 1, Reg 51, D(3)	MICBIAS Voltage (without load)
00	0	X	1.0V
00	1	X	1.25V
01	0	X	1.4V
01	1	X	1.7V
10	0	1	2.1V
10	1	1	2.5V
11	X	0	AVdd
11	X	1	LDOIN

5.9.2 Digital Microphone Function

In addition to supporting analog microphones, the TLV320AIC3204 also interfaces to digital microphones.

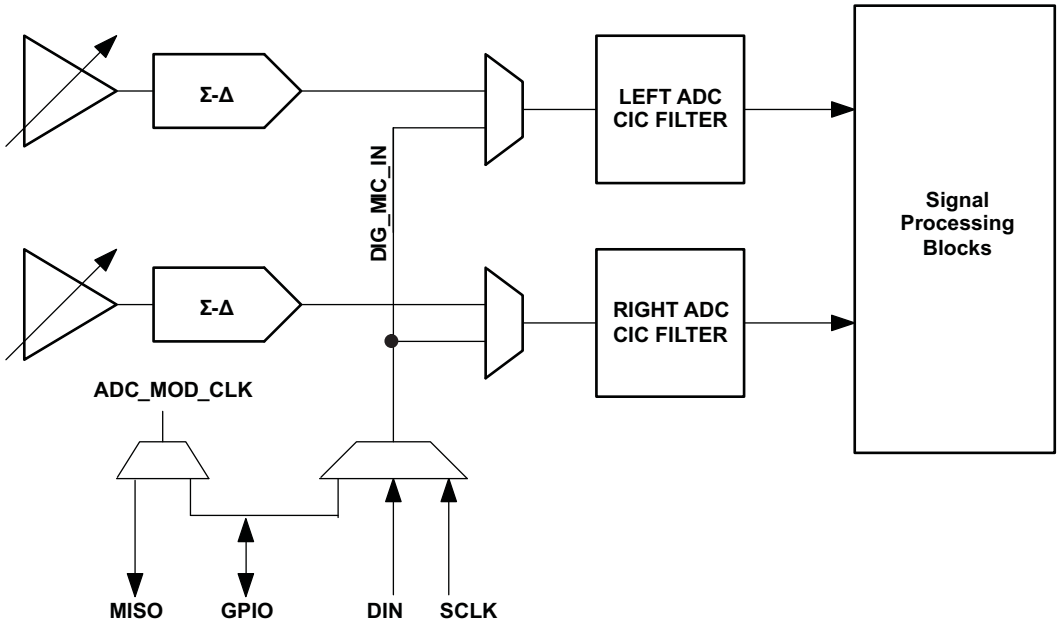


Figure 5-16. Digital Microphone in TLV320AIC3204

The TLV320AIC3204 outputs internal clock ADC_MOD_CLK on GPIO pin (Page 0, Register 51, D(5:2)) or MISO pin (Page 0, Register 55, D(4:1)). This clock can be connected to the external digital microphone device. The single-bit output of the external digital microphone device can be connected to GPIO, DIN or SCLK pins. Internally the TLV320AIC3204 latches the steady value of data on the rising edge of ADC_MOD_CLK for the Left ADC channel, and the steady value of data on falling edge for the Right ADC channel.

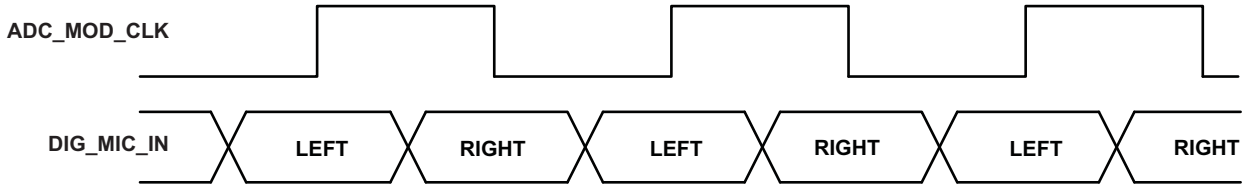


Figure 5-17. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

5.9.3 Channel-to-Channel Phase Adjustment

The TLV320AIC3204 has a built-in feature to fine-adjust the phase between the stereo ADC record signals. The phase compensation is particularly helpful to adjust delays when using dual microphones for noise cancellation etc.

This delay can be controlled in fine amounts in the following fashion.

Delay(7:0) = Page 0/Register 85/D(7:0)

Where

$$RIGHT\_ADC\_PHASE\_COMP(t) = RIGHT\_ADC\_OUT(t - t_{pr}) \quad (5\text{-}5)$$

where

$$t_{pr} = \frac{(Delay(4:0) + Delay(6:5) * AOSR * k_f)}{AOSR * ADC\_FS}$$

Where k_f is a function of the decimation filter:

Decimation Filter Type	k_f
A	0.25
B	0.5
C	1

and

$$LEFT\_ADC\_PHASE\_COMP(t) = LEFT\_ADC\_OUT(t - t_{pl}) \quad (5\text{-}6)$$

Where

$$t_{pl} = \frac{Delay(7)}{AOSR * ADC\_FS} \quad (5\text{-}7)$$

5.9.4 DC Measurement

The TLV320AIC3204 supports a highly flexible DC measurement feature using the high resolution oversampling and noise-shaping ADC. This mode can be used when the particular ADC channel is not used for the voice/audio record function. This mode can be enabled by programming Page 0, Register 102, D(7:6). The converted data is 24-bits, using 2.22 numbering format. The value of the converted data for the left-channel ADC can be read back from Page 0, Register 104-106 and for the right-channel ADC from Page 0, Register 107-109. Before reading back the converted data, Page 0, Register 103, D(7:6) must be programmed to latch the converted data into the read-back register. After the converted data is read back, Page 0, Register 103, D(7:6) must be reset to 00 immediately. In DC measurement mode, two measurement methods are supported.

Mode A

In DC-measurement mode A, a variable-length averaging filter is used. The length of the averaging filter D, can be programmed from 1 to 20 by programming Page 0, Register 100, D(4:0). To choose mode A, Page 0, Register 102, D(5) must be programmed to 0.

Mode B

To choose mode B Page 0, Register 102, D(5) must be programmed to 1. In DC-measurement mode B, a first-order IIR filter is used. The coefficients of this filter are determined by D, Page 0, Register 102, D(4:0). The nature of the filter is given in the table below

Table 5-12. DC Measurement Bandwidth Settings

D:Page 0, Reg 102 , D(4:0)	–3 dB BW (kHz)	–0.5 dB BW (kHz)
1	688.44	236.5
2	275.97	96.334
3	127.4	44.579
4	61.505	21.532
5	30.248	10.59
6	15.004	5.253
7	7.472	2.616
8	3.729	1.305
9	1.862	652
10	931	326
11	465	163
12	232.6	81.5
13	116.3	40.7
14	58.1	20.3
15	29.1	10.2
16	14.54	5.09
17	7.25	2.54
18	3.63	1.27
19	1.8	0.635
20	0.908	0.3165

By programming Page 0, Reg 103, D(5) to ‘1’, the averaging filter is periodically reset after 2^R number of ADC_MOD_CLK, where R is programmed in Page 0, Reg 103, D(4:0). When Page 0, Reg 103, D(5) is set to 1 then the value of D should be less than the value of R. When Page 0, Reg 103, D(5) is programmed as 0 the averaging filter is never reset.

5.9.5 Fast Charging AC Capacitors

The value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage. To enable quick charging, the TLV320AIC3204 has modes to speed up the charging of the coupling capacitor. These are controlled by controlling Page 1, Register 71, D(5:0).

5.9.6 Anti Thump

For normal voice or audio recording, the analog input pins of the TLV320AIC3204, must be AC-coupled to isolate the DC-common mode voltage of the driving circuit from the common-mode voltage of the TLV320AIC3204.

When the analog inputs are not selected for any routing, the input pins are 3-stated and the voltage on the pins is undefined. When the unselected inputs are selected for any routing, the input pins must charge from the undefined voltage to the input common-mode voltage. This charging signal can cause audible

artifacts. In order to avoid such artifacts the TLV320AIC3204 also incorporates anti-thump circuitry to allow connection of unused inputs to the common-mode level. This feature is disabled by default, and can be enabled by writing the appropriate value into Page 1, Register 58, D(7:2). The use of this feature in combination with the PTM_R1 setting in Page 0, Register 61 when the ADC channel is powered down causes the additional current consumption of 700µA from AVdd and 125µA from DVdd in the sleep mode.

5.9.7 Adaptive Filtering

After the ADC is running, the filter coefficients are locked and cannot be accessed for read or write. However the TLV320AIC3204 offers an adaptive filter mode as well. Setting Register Page 8,Reg 1, D(2)=1 turns on double buffering of the coefficients. In this mode filter coefficients can be updated through the host and activated without stopping and restarting the ADC, enabling advanced adaptive filtering applications.

To support double buffering, all coefficients are stored in two buffers (Buffer A and B). When the ADC is running and adaptive filtering mode is turned on, setting the control bit Page 8, Reg 1,D(0)=1 switches the coefficient buffers at the next start of a sampling period. The bit reverts to 0 after the switch occurs. At the same time, the flag Page 8, Reg 1, D(1) toggles.

The flag in Page 8, Reg 1, D(1) indicates which of the two buffers is actually in use.

Page 8, Reg 1, D(1)=0: Buffer A is in use by the ADC engine, D(1)=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the ADC, regardless to which buffer the coefficients have been written

ADC running	Flag, Page 8, Reg 1, D(1)	Coefficient Buffer in use	Writing to	Will update
No	0	None	C4, Buffer A	C4, Buffer A
No	0	None	C4, Buffer B	C4, Buffer B
Yes	0	Buffer A	C4, Buffer A	C4, Buffer B
Yes	0	Buffer A	C4, Buffer B	C4, Buffer B
Yes	1	Buffer B	C4, Buffer A	C4, Buffer A
Yes	1	Buffer B	C4, Buffer B	C4, Buffer A

5.10 ADC Setup

The following discussion is intended to guide a system designer through the steps necessary to configure the TLV320AIC3204 ADC.

Step 1

The system clock source (master clock) and the targeted ADC sampling frequency must be identified.

Depending on the targeted performance, the decimation filter type (A, B or C) and OSR value can be determined.

- Filter A with AOSR of 128 should be used for 48kHz high performance operation.
- Filter B with AOSR of 64 should be used for 96kHz operations.

  In conjunction with a common mode setting of 0.75V and PTM_R1 this can also be used for 48kHz PowerTune operation.
- Filter C with AOSR of 32 should be used for 192kHz operations

Based on the identified filter type and the required signal processing capabilities the appropriate processing block can be determined from the list of available processing blocks (PRB_R1 to PRB_R18) (See Table 5-4).

Based on the available master clock, the chosen OSR and the targeted sampling rate, the clock divider values NADC and MADC can be determined. If necessary the internal PLL will add a large degree of flexibility.

In summary, Codec_Clkin which is either derived directly from the system clock source or from the internal PLL, divided by MADC, NADC and AOSR, must be equal to the ADC sampling rate ADC_FS. The Clodec_Clkin clock signal is shared with the DAC clock generation block.

CODEC_CLKIN = NADC*MADC*AOSR*ADC_FS

To a large degree NADC and MADC can be chosen independently in the range of 1 to 128. In general NADC should be as large as possible as long as the following condition can still be met:

MADC*AOSR/32 ≥ RC

RC is a function of the chosen processing block and is listed in the Table 5-4 Overview Processing Blocks

The common mode setting of the device is determined by the available analog power supply and the desired PowerTune mode, this common mode setting is shared across ADC, DAC (input common mode) and analog bypass path.

At this point the following device specific parameters are known:

PRB_Rx, AOSR, NADC, MADC, common mode setting

Additionally if the PLL is used the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed between powering the device up and reading data from the device:

Define starting point:	Set register page to 0 Initiate SW Reset
Program Clock Settings	Program PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program the processing block to be used

At this point, at the latest, analog power supply must be applied to the device (via internal LDO or external)

Program Analog Blocks	Set register Page to 1 Disable coarse AVdd generation Enable Master Analog Power Control Program Common Mode voltage Program PowerTune (PTM) mode Program MicPGA startup delay Program Reference fast charging Routing of inputs/common mode to ADC input Unmute analog PGAs and set analog gain
Power Up ADC	Set register Page to 0 Power up ADC Channels Unmute digital volume control

A detailed example can be found in Section 5.22.

5.11 DAC

The TLV320AIC3204 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3204 allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring the Page 0, Reg 13, and Reg 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3204 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

5.11.1 Processing Blocks

The TLV320AIC3204 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. The Table 5-13 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 5-13. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Number of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P1	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	No	5	Yes	Yes	No	12
PRB_P25	A	Stereo	No	5	Yes	Yes	Yes	12

5.11.2 Processing Blocks – Details

5.11.2.1 3 Biquads, Filter A

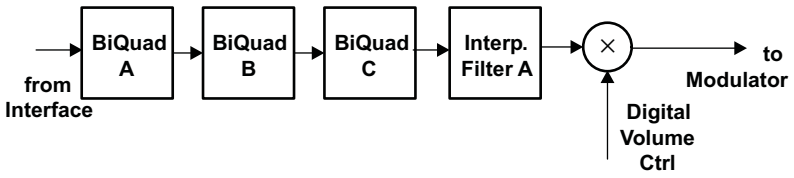


Figure 5-18. Signal Chain for PRB_P1 and PRB_P4

5.11.2.2 6 Biquads, 1st order IIR, DRC, Filter A or B

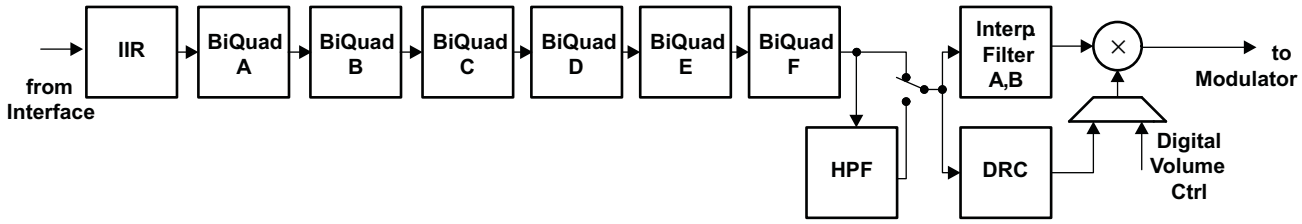


Figure 5-19. Signal Chain for PRB_P2, PRB_P5, PRB_P10 and PRB_P15

5.11.2.3 6 Biquads, 1st order IIR, Filter A or B

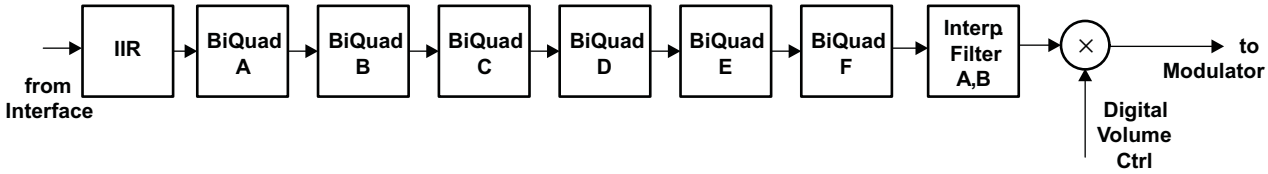


Figure 5-20. Signal Chain for PRB_P3, PRB_P6, PRB_P11 and PRB_P16

5.11.2.4 IIR, , Filter B or C

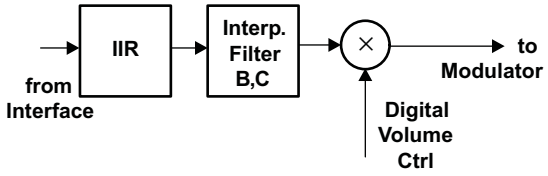


Figure 5-21. Signal Chain for PRB_P7, PRB_P12, PRB_P17 and PRB_P20

5.11.2.5 4 Biquads, DRC, Filter B

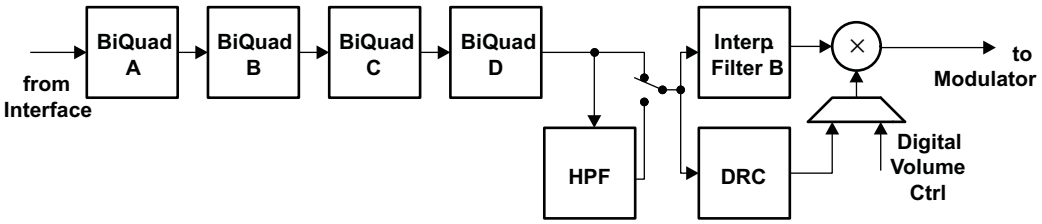


Figure 5-22. Signal Chain for PRB_P8 and PRB_P13

5.11.2.6 4 Biquads, Filter B

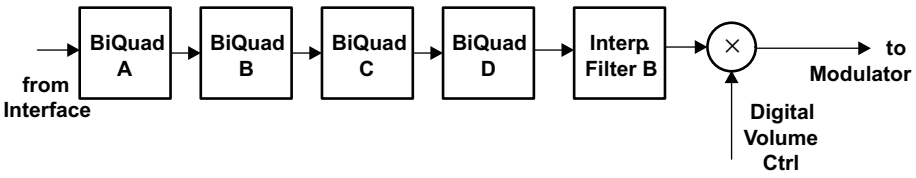


Figure 5-23. Signal Chain for PRB_P9 and PRB_P14

5.11.2.7 4 Biquads, 1st order IIR, DRC, Filter B

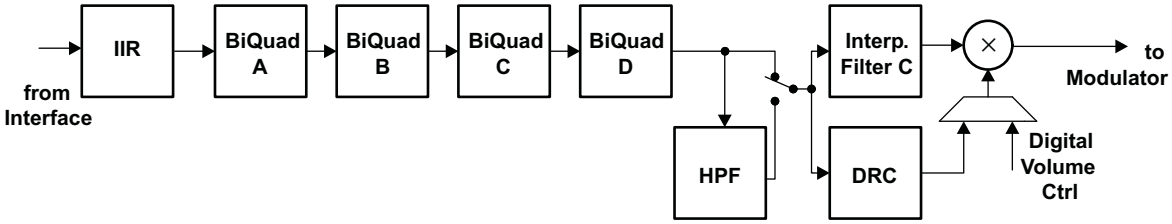


Figure 5-24. Signal Chain for PRB_P18 and PRB_P21

5.11.2.8 4 Biquads, 1st order IIR, Filter C

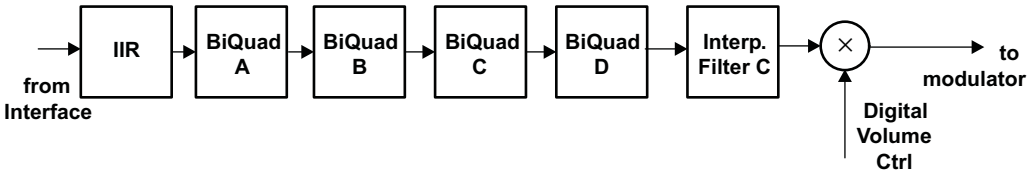


Figure 5-25. Signal Chain for PRB_P19 and PRB_P22

5.11.2.9 2 Biquads, 3D, Filter A

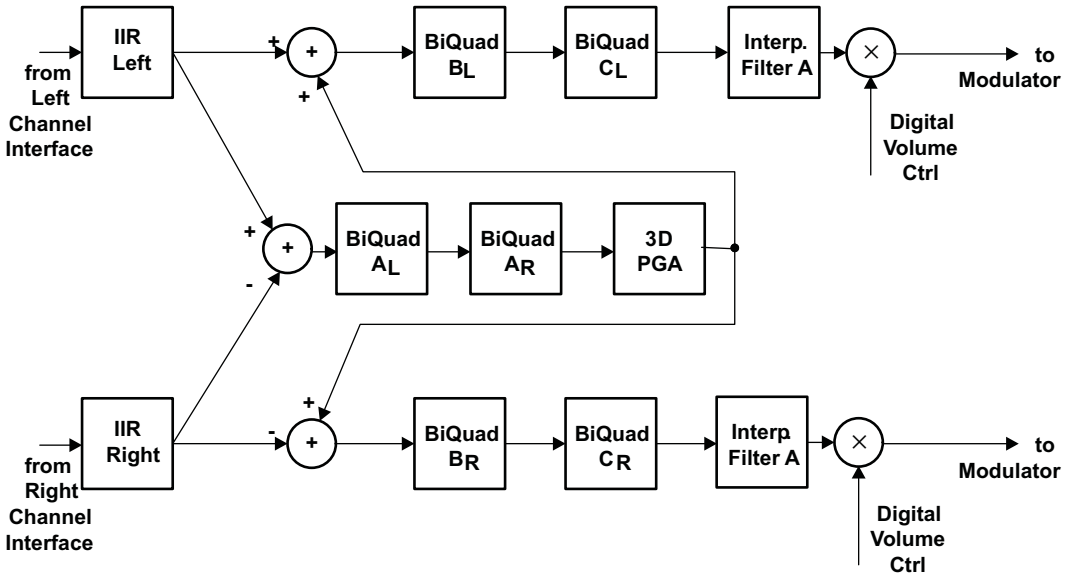


Figure 5-26. Signal Chain for PRB_P23

5.11.2.10 5 Biquads, DRC, 3D, Filter A

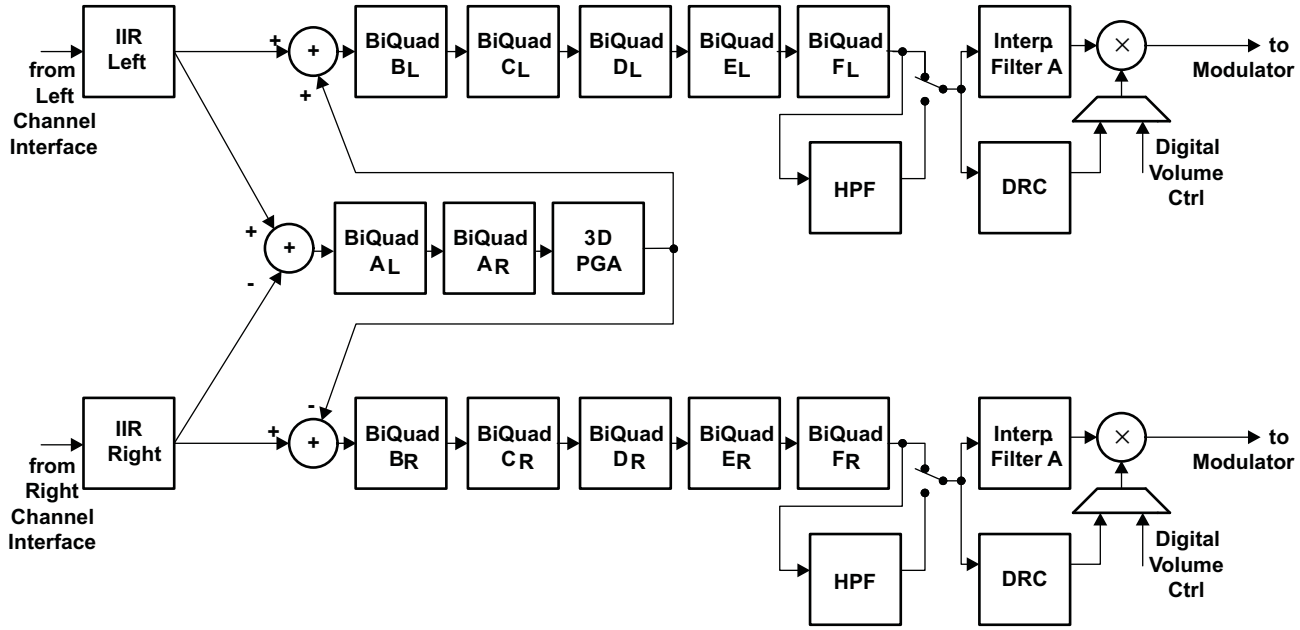


Figure 5-27. Signal Chain for PRB_P24

5.11.2.11 5 Biquads, DRC, 3D, Beep Generator, Filter A

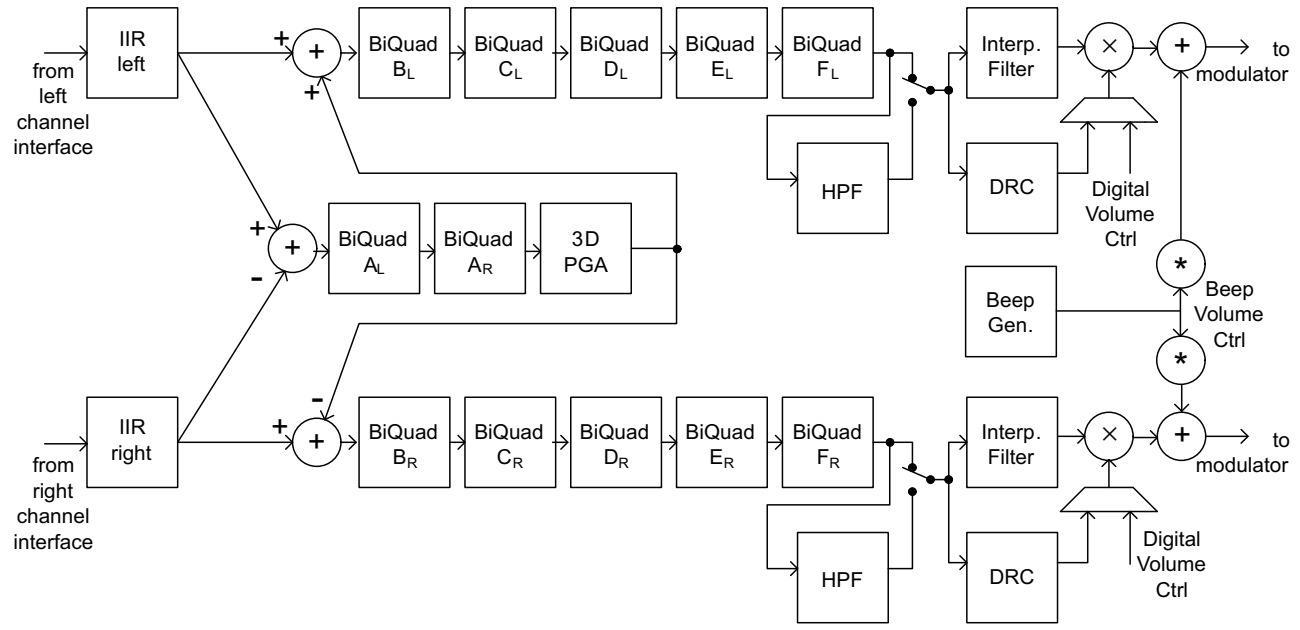


Figure 5-28. Signal Chain for PRB_P25

5.11.3 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. Up to 6 biquad sections are available for specific processing blocks.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering please see Section 5.14.3.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see Section 6.6.

5.11.3.1 1st-Order IIR Section

The IIR is of first-order and its transfer function is given by

Figure 5-29.

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (5\text{-}8)$$

The frequency response for the 1st order IIR Section with default coefficients is flat

Table 5-14. DAC IIR Filter Coefficients

Filter	Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
1st Order IIR	N0	C65 (Pg 46, Reg 28,29,30)	C68 (Pg 46, Reg 40,41,42)
	N1	C66 (Pg 46. Reg 32,33,34)	C69 (Pg 46, Reg 44,45,46)
	D1	C67 (Pg 46, Reg 36,37,38)	V70 (Pg 46, Reg 48,49,50)

5.11.3.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2*N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2*D_1 z^{-1} - D_2 z^{-2}} \quad (5\text{-}9)$$

Table 5-15. DAC Biquad Filter Coefficients

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD A	N0	C1 (Pg 44, Reg 12,13,14)	C33 (Pg 45, Reg 20,21,22)
	N1	C2 (Pg 44, Reg 16,17,18)	C34 (Pg 45, Reg 24,25,26)
	N2	C3 (Pg 44, Reg 20,21,22)	C35 (Pg 45, Reg 28,29,30)
	D1	C4 (Pg 44, Reg 24,25,26)	C36 (Pg 45, Reg 32,33,34)
	D2	C5 (Pg 44, Reg 28,29,30)	C37 (Pg 45, Reg 36,37,38)
BIQUAD B	N0	C6 (Pg 44, Reg 32,33,34)	C38 (Pg 45, Reg 40,41,42)
	N1	C7 (Pg 44, Reg 36,37,38)	C39 (Pg 45, Reg 44,45,46)
	N2	C8 (Pg 44, Reg 40,41,42)	C40 (Pg 45, Reg 48,49,50)
	D1	C9 (Pg 44, Reg 44,45,46)	C41 (Pg 45, Reg 52,53,54)
	D2	C10 (Pg 44, Reg 48,49,50)	C42 (Pg 45, Reg 56,57,58)
BIQUAD C	N0	C11 (Pg 44, Reg 52,53,54)	C43 (Pg 45, Reg 60,61,62)
	N1	C12 (Pg 44, Reg 56,57,58)	C44 (Pg 45, Reg 64,65,66)
	N2	C13 (Pg 44, Reg 60,61,62)	C45 (Pg 45, Reg 68,69,70)
	D1	C14 (Pg 44, Reg 64,65,66)	C46 (Pg 45, Reg 72,73,74)
	D2	C15 (Pg 44, Reg 68,69,70)	C47 (Pg 45, Reg 76,77,78)
BIQUAD D	N0	C16 (Pg 44, Reg 72,73,74)	C48 (Pg 45, Reg 80,81,82)

Table 5-15. DAC Biquad Filter Coefficients (continued)

Filter	Coefficient	Left DAC Channel	Right DAC Channel
	N1	C17 (Pg 44, Reg 76,77,78)	C49 (Pg 45, Reg 84,85,86)
	N2	C18 (Pg 44, Reg 80,81,82)	C50 (Pg 45, Reg 88,89,90)
	D1	C19 (Pg 44, Reg 84,85,86)	C51 (Pg 45, Reg 92,93,94)
	D2	C20 (Pg 44, Reg 88,89,90)	C52 (Pg 45, Reg 96,97,98)
BIQUAD E	N0	C21 (Pg 44, Reg 92,93,94)	C53 (Pg 45, Reg 100,101,102)
	N1	C22 (Pg 44, Reg 96,97,98)	C54 (Pg 45, Reg 104,105,106)
	N2	C23 (Pg 44, Reg 100,101,102)	C55 (Pg 45, Reg 108,109,110)
	D1	C24 (Pg 44, Reg 104,105,106)	C56 (Pg 45, Reg 112,113,114)
	D2	C25 (Pg 44, Reg 108,109,110)	C57 (Pg 45, Reg 116,117,118)
BIQUAD F	N0	C26 (Pg 44, Reg 112,113,114)	C58 (Pg 45, Reg 120,121,122)
	N1	C27 (Pg 44, Reg 116,117,118)	C59 (Pg 45, Reg 124,125,126)
	N2	C28 (Pg 44, Reg 120,121,122)	C60 (Pg 46, Reg 8,9,10)
	D1	C29 (Pg 44, Reg 124,125,126)	C61 (Pg 46, Reg 12,13,14)
	D2	C30 (Pg 45, Reg 8,9,10)	C62 (Pg 46, Reg 16,17,18)

5.11.4 INTERPOLATION FILTER

5.11.4.1 Interpolation Filter A

Table 5-16. DAC Interpolation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45Fs	±0.015	dB
Filter Gain Stop Band	0.55Fs… 7.455Fs	–65	dB
Filter Group Delay		21/Fs	s

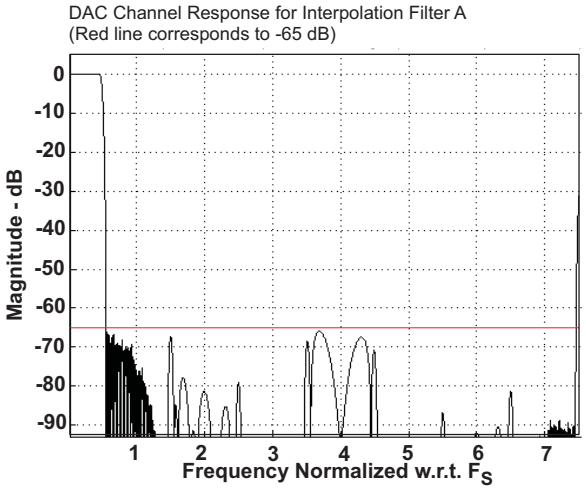


Figure 5-30. DAC Interpolation Filter A, Frequency Response

5.11.4.2 Interpolation Filter B

Filter B is specifically designed for an Fs of above 96ksps. Thus, the flat pass-band region easily covers the required audio band of 0-20kHz.

Table 5-17. DAC Interpolation Filter B, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45Fs	±0.015	dB
Filter Gain Stop Band	0.55Fs… 3.45Fs	–58	dB
Filter Group Delay		18/Fs	s

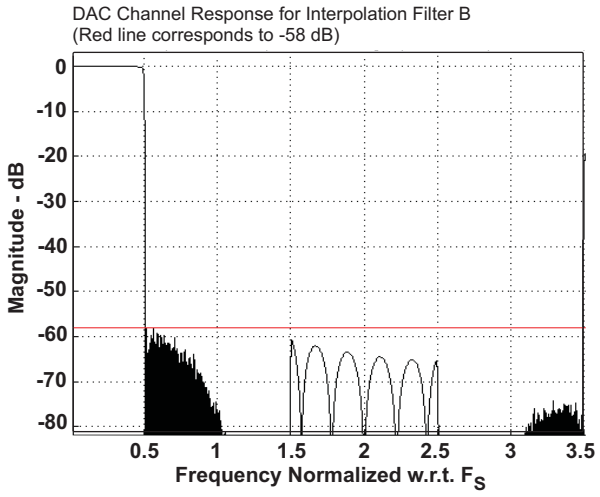


Figure 5-31. Channel Interpolation Filter B, Frequency Response

5.11.4.3 Interpolation Filter C

Filter C is specifically designed for the 192ksps mode. The pass band extends up to 0.40*Fs (corresponds to 80kHz), more than sufficient for audio applications.

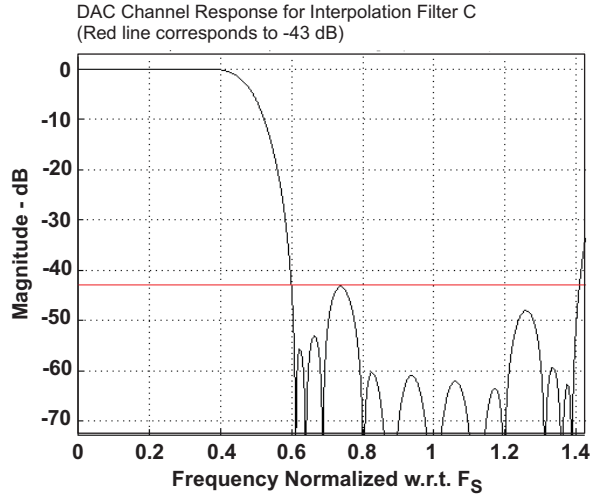


Figure 5-32. DAC Interpolation Filter C, Frequency Response

The basic filter characteristics for the Interpolation Filters A, B and C are as follows. These values are at 48ksps with the droop of the analog reconstruction filters taken into account.

Table 5-18. DAC Interpolation Filter C, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.35Fs	±0.03	dB
Filter Gain Stop Band	0.60Fs… 1.4Fs	–43	dB
Filter Group Delay		13/Fs	s

5.12 DAC Output Drivers

5.12.1 Headphone Amplifier

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating at 1.8V analog supplies. While running off AVdd supply the output common mode of headphone driver is set by the common mode setting of analog inputs in Page 1, Reg 10, D(6), to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly off the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common mode can be adjusted to either 1.25V, 1.5V or 1.65V by configuring Page 1, Reg 10, D(5:4). When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal, left and right ADC PGA signal and line-bypass from analog input IN1L and IN1R by configuring Page 1, Reg and Page 1, Reg 13 respectively. The ADC PGA signals can be attenuated up to 30dB before routing to headphone drivers by configuring Page 1, Reg 24 and Page 1, Reg 25. The line-input signals can be attenuated up to 72dB before routing by configuring Page 1, Reg 22 and 23. The level of the DAC signal can be controlled using the digital volume control of the DAC in Page 0, Reg 65 and 66. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB(1) in steps of 1dB. These can be configured by programming Page 1, Reg 16 and 17. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Refer to Section 5.13.1 for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

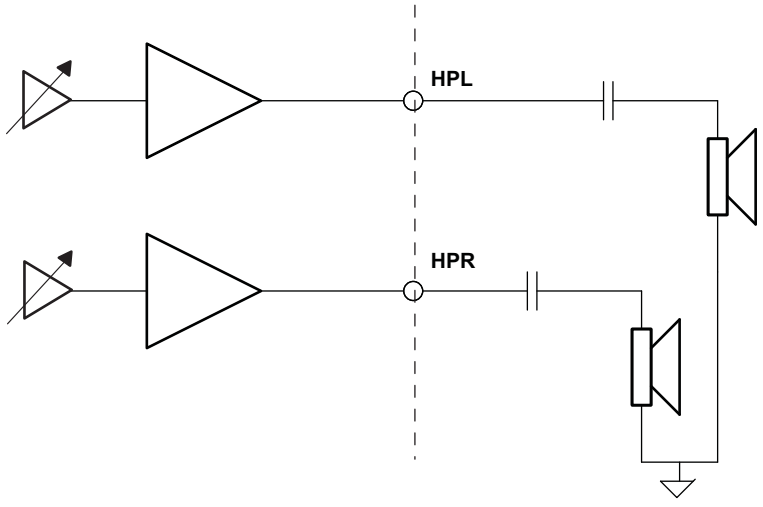


Figure 5-33. Stereo Headphone Configuration

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

Differential Loading

The headphone amplifiers can be configured differentially as shown in Figure 5-34. However this scheme is supported only when using the headphone-output stage powered from the AVdd supply.

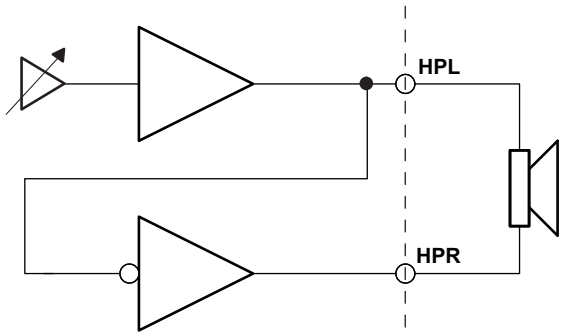


Figure 5-34. Differential Receiver Speaker Configuration

The TLV320AIC3204 supports an additional low-power mode for routing a mono DAC for a differential headphone configuration as shown in Figure 5-35.

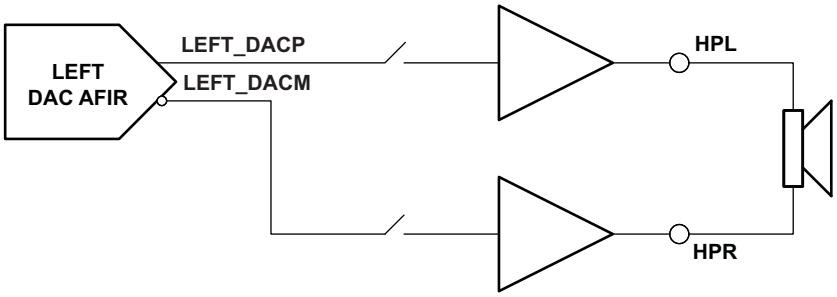


Figure 5-35. Low Power Mono DAC to Differential Headphone

The TLV320AIC3204 headphone drivers support pop-free operation. Because the HPL and HPR are high-power drivers, pop can result due to sudden transient changes in the output drivers if care is not taken. The most critical care is required while using the drivers as stereo single-ended capacitively-coupled drivers as shown in Figure 5-33. The output drivers achieve pop-free power-up by using slow power-up modes. Conceptually, the circuit during power-up can be visualized as

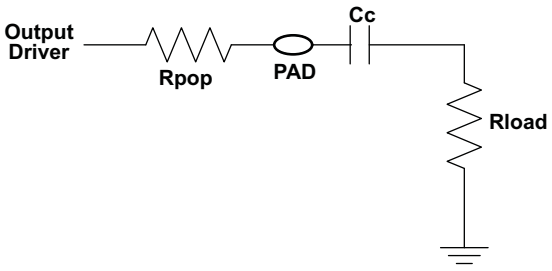


Figure 5-36. Conceptual Circuit for Pop-Free Power-up

The value of Rpop can be chosen by setting register Page 1, Register 20, D(1:0).

Table 5-19. R_{pop} Values

Page 1, Register 20, D(1:0)	Rpop Value
00	2 kΩ
01	6 kΩ
10	25 kΩ

To minimize audible artifacts, two parameters can be adjusted to match application requirements. The voltage V_{load} across R_{load} at the beginning of slow charging should not be more than a few mV. At that time the voltage across R_{load} can be determined as:

$$V_{load} = \frac{R_{load}}{R_{load} + R_{pop}} \times V_{cm} \quad (5\text{-}10)$$

For a typical R_{load} of 32 Ω, R_{pop} of 6 kΩ or 25 kΩ will deliver good results (see Table 5-19 for register settings).

According to the conceptual circuit in Figure 5-36, the voltage on PAD will exponentially settle to the output common-mode voltage based on the value of R_{pop} and C_c. Thus, the output drivers must be in slow power-up mode for time T, such that at the end of the slow power-on period, the voltage on V_{pad} is very close to the common-mode voltage. The TLV320AIC3204 allows the time T to be adjusted to allow for a wide range of R_{load} and C_c by programming Page 1, Register 20, D(5:2). For the time adjustments, the value of C_c is assumed to be 47µF. N=5 is expected to yield good results.

Page 1, Register 20D(5:2)	Slow Charging Time=N*Time Constants(for Rpop and 47µF)
0000	N=0
0001	N=0.5
0010	N=0.625
0011	N=0.75
0100	N=0.875
0101	N=1.0
0110	N=2.0
0111	N=3.0
1000	N=4.0
1001	N=5.0
1010	N=6.0
1011	N=7.0
1100	N=8.0
1101	N=16 (Not valid for Rpop=25K)
1110	N=24 (Not valid for Rpop=25K)
1111	N=32 (Not valid for Rpop=25K)

Again for e.g., for R_{load}=32Ω, C_c=47µF and common mode of 0.9V the number of time constants required for pop-free operation is 5 or 6. Higher or lower value of C_c will require higher or lower value for N.

During the slow-charging period, no signal is routed to the output driver. Therefore, choosing a larger than necessary value of N results in a delay from power-up to signal at output. At the same time, choosing N to be smaller than the optimal value results in poor pop performance at power-up.

The signals being routed to headphone drivers (e.g. DAC, MAL , MAR and IN1) often have DC offsets due to less-than-ideal processing. As a result, when these signals are routed to output drivers, the offset voltage causes a pop. To improve the pop-performance in such situations, a feature is provided to soft-step the DC-offset. At the beginning of the signal routing, a high-value attenuation can be applied which can be progressively reduced in steps until the desired gain in the channel is reached. The time interval between each of these gain changes can be controlled by programming Page 1, Register 20, D(7:6). This gain soft-stepping is applied only during the initial routing of the signal to the output driver and not during subsequent gain changes.

Page 1, Register 20, D(7:6)	Soft-stepping Step Time During initial signal routing
00	0 ms (soft-stepping disabled)
01	50ms
10	100ms
11	200ms

It is recommended to use the following sequence for achieving optimal pop performance at power-up

1. Choose the value of R_{pop}, N (time constants) and soft-stepping step time for slow power-up.
2. Choose the configuration for output drivers, including common modes and output stage power connections
3. Select the signals to be routed to headphones.
4. Power-up the blocks driving signals into HPL and HPR, but keep it muted
5. Unmute HPL and HPR and set the desired gain setting.
6. Power-on the HPL and HPR drivers.
7. Unmute the block driving signals to HPL and HPR after the Driver PGA flags are set to indicate completion of soft-stepping after power-up. These flags can be read from Page 1, Register 63, D(7:6).

It is important to configure the Headphone Output driver depop control registers before powering up the headphone; these register contents should not be changed when the headphone drivers are powered up.

Before powering down the HPL and HPR drivers, it is recommended that user read back the flags in Page 1, Register 63. For example. before powering down the HPL driver, ensure that bit D(7) = 1 and bit D(3) = 1 if IN1_L is routed to HPL and bit D(1) = 1 if the Left Mixer is routed to HPL. The output driver should be powered down only after a steady-state power-up condition has been achieved. This steady state power-up condition also must be satisfied for changing the HPL/R driver mute control in Page 1, Register 16 and 17, D(7), i.e. muting and unmuting should be done after the gain and volume controls associated with routing to HPL/R finished soft-stepping.

In the differential configuration of HPL and HPR, when no coupling capacitor is used, the slow charging method for pop-free performance need not be used. In the differential load configuration for HPL and HPR, it is recommended to not use the output driver MUTE feature, because a pop may result.

During the power-down state, the headphone outputs are weakly pulled to ground using an approximately 50kΩ resistor to ground, to maintain the output voltage on HPL and HPR pins.

5.12.2 Headphone Amplifier Class-D Mode

By default the headphone amplifiers in the TLV320AIC3204 work in Class-AB mode. By writing to Page 1, Register 3, D(7:6) for the left headphone amplifier, and Page 1, Register 4, D(7:6) with value 11, the headphone amplifiers enter a Class-D mode of operation.

In this mode a high frequency digital pulse-train representation of the DAC signal is fed to the load connected to HPL and HPR outputs.

Because the output signal is a pulse train switching between Power Supply and Ground, the efficiency of the amplifier is greatly improved. In this mode however, for good noise performance, care should be taken to keep the analog power supply clean.

For using the Class-D mode of operation, the following clock-divider condition should be met:

MDAC = I × 4, where I = 1, 2, ..., 32

When a direct digital pulse train is driven out as a signal, high frequencies as a function of pulse train frequency are also present which lead to power waste. To increase the efficiency and reduce power dissipation in the load due to these high frequencies, an LC filter should be used in series with the output and the load. The cutoff frequency of the LC filter should be adjusted to allow audio signals below 20kHz to pass through, but highly attenuate the high-frequency signal content.

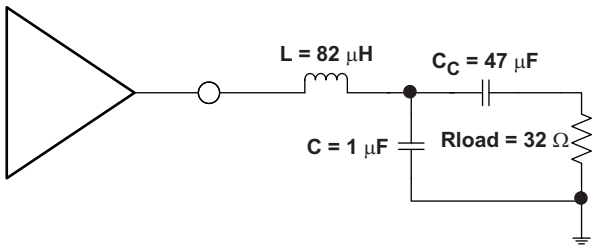


Figure 5-37. Configuration for Using Headphone Amplifier in Class-D Mode

For using the headphones in the Class-D mode of operation, the headphones should first be powered up in default Class-AB mode to charge the AC-coupling capacitor to the set common mode voltage. Once the headphone amplifiers have been so powered up, the DAC should be routed to headphones and unmuted before they can be switched to the Class-D mode. After Class D mode has been turned on, the linear, Class AB mode amplifier must be turned off. For powering down the headphone amplifiers, the DAC should first be muted.

5.12.3 Line Out Amplifier

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common modes of line level drivers can be configured to equal either the analog input common-mode setting, or 1.65V by programming Page 1, Register 3, D(3). With output common-mode setting of 1.65V and LDOIN supply at 3.3V the line-level drivers can drive up to 1Vrms output signal. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal. The signal mixing can be configured by programming Page 1, Register 14 and 15. Additionally, the two line-level drivers can be configured to act as a mono differential line level driver by routing output of LOR to LOL (Page 1, Register 14, D(0) = ‘1’).

The output of DAC can be simultaneously played back to the stereo headphone drivers as well as stereo line- level drivers. In such a case, the DAC signal at the headphone outputs and line outputs are out-of-phase with respect to each other.

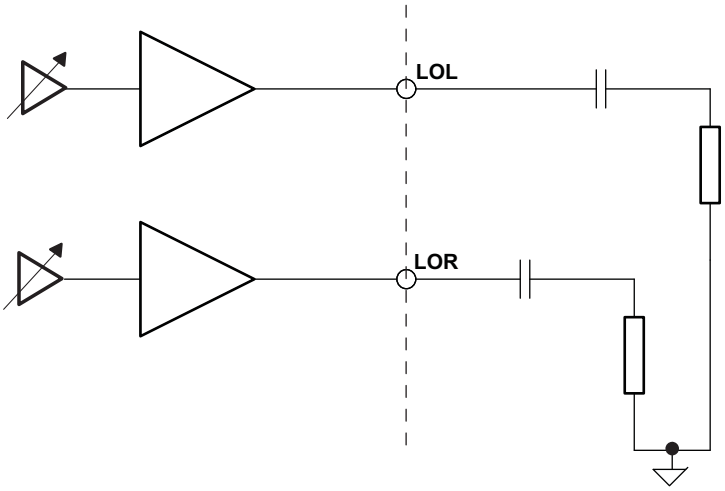


Figure 5-38. Stereo Single-Ended Line-out

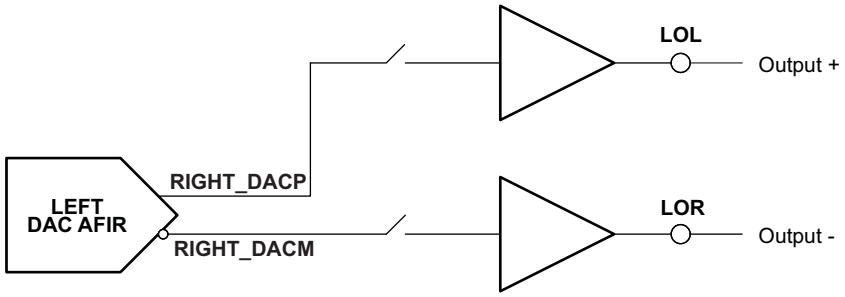


Figure 5-39. Low Power Mono DAC to Differential Line-out

5.13 DAC GAIN SETTING

5.13.1 PowerTune Modes

As part of the PowerTune strategy, the analog properties of the DAC are adjusted. As a consequence, the full-scale signal swing achieved at the headphone and line outputs must be adjusted.

Please see Table 5-20 for the proper gain compensation values across the different combinations.

Table 5-20. DAC Gain vs. PowerTune Modes

DAC PowerTune Mode Control	PowerTune Mode	Headphone/Line-out Gain	
Page 1,Register 3/4, D(4:2)		CM = 0.75V, Gain for 375mV$_{RMS}$ output swing at 0dB full scale input	CM = 0.9V, Gain for 500mV$_{RMS}$ output swing at 0dB full scale input
000	PTM_P3, PTM_P4	–2	0
001	PTM_P2	2	4
010	PTM_P1	12	14

5.13.2 Digital Volume Control

The TLV320AIC3204 signal processing blocks incorporate a digital volume control block that can control the volume of the playback signal from +24dB to –63.5dB in steps of 0.5dB. These can be controlled by writing to Page 0, Register 65 and 66. The volume control of left and right channels by default can be controlled independently, however by programming Page 0, Reg 64, D(1:0), they can be made interdependent. The volume changes are soft-stepped in steps of 0.5dB to avoid audible artifacts during

gain change. The rate of soft-stepping can be controlled by programming Page 0, Reg 63, D(1:0) to either one step per frame (DAC_FS) or one step per 2 frames. The soft-stepping feature can also be entirely disabled. During soft-stepping the value of the actual applied gain would differ from the programmed gain in register. The TLV320AIC3204 gives a feedback to the user in form of register readable flag to indicate that soft-stepping is currently in progress. The flags for left and right channels can be read back by reading Page 0, Reg 38, D(4) and D(0) respectively. A value of 0 in these flags indicates a soft-stepping operation in progress, and a value of 1 indicates that soft-stepping has completed. A soft-stepping operation comes into effect during a) power-up, when the volume control soft-steps from –63.5dB to programmed gain value b) volume change by user when DAC is powered up and c) power-down, when the volume control block soft-steps to –63.5dB before powering down the channel.

5.13.3 Dynamic Range Compression

Typical music signals are characterized by crest factors, the ratio of peak signal power to average signal power, of 12dB or more. In order to avoid audible distortions due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping of peak signals. As a result, during nominal periods, the applied gain is low, causing the perception that the signal is not loud enough. To overcome this problem, the DRC in the TLV320AIC3204 continuously monitors the output of the DAC Digital Volume control to detect its power level w.r.t. 0dB FS. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. This results in sounds more pleasing to the ear as well as sounding louder during nominal periods.

The DRC functionality in the TLV320AIC3204 is implemented by a combination of Processing Blocks in the DAC channel as described in Section 5.11.2.

The DRC can be disabled by writing into Page 0, Reg 68, D(6:5).

The DRC typically works on the filtered version of the input signal. The input signals have no audio information at DC and extremely low frequencies; however they can significantly influence the energy estimation function in DRC. Also most of the information about signal energy is concentrated in the low frequency region of the input signal.

In order to estimate the energy of the input signal, the signal is first fed to the DRC high-pass filter and then to the DRC low-pass filter. These filters are implemented as first-order IIR filters given by

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (5\text{-}11)$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (5\text{-}12)$$

The coefficients for these filters are 24-bits wide in two’s-complement and are user programmable through register write as given in Table 5-21

Table 5-21. DRC HPF and LPF Coefficients

Coefficient	Location
HPF N0	C71 Page 46, Register 52 to 55
HPF N1	C72 Page 46, Register 56 to 59
HPF D1	C73 Page 46, Register 60 to 63
LPF N0	C74 Page 46, Register 64 to 67
LPF N1	C75 Page 46, Register 68 to 71
LPF D1	C76 Page 46, Register 72 to 75

The default values of these coefficients implement a high-pass filter with a cut-off at 0.00166*DAC_FS, and a low-pass filter with a cutoff at 0.00033 * DAC_FS.

The output of the DRC high-pass filter is fed to the Processing Block selected for the DAC Channel. The absolute value of the DRC-LPF filter is used for energy estimation within the DRC.

The gain in the DAC Digital Volume Control is controlled by Page 0, Register 65 and 66. When the DRC is enabled, the applied gain is a function of the Digital Volume Control register setting and the output of the DRC.

The DRC parameters are described in sections that follow.

5.13.3.1 DRC Threshold

The DRC Threshold represents the level of the DAC playback signal at which the gain compression becomes active. The output of the digital volume control in the DAC is compared with the set threshold. The threshold value is programmable by writing to register Page 0, Register 68, D(4:2). The Threshold value can be adjusted between –3dBFS to -24dBFS in steps of 3dB. Keeping the DRC Threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC Threshold value too low can limit the perceived loudness of the output signal.

The recommended DRC-Threshold value is –24 dB.

When the output signal exceeds the set DRC Threshold, the interrupt flag bits at Page 0, Register 44, D(3:2) are updated. These flag bits are 'sticky' in nature, and are reset only after they are read back by the user. The non-sticky versions of the interrupt flags are also available at Page 0, Register 46, D(3:2).

5.13.3.2 DRC Hysteresis

DRC Hysteresis is programmable by writing to Page 0, Register 68, D(1:0). It can be programmed to values between 0dB and 3dB in steps of 1dB. It is a programmable window around the programmed DRC Threshold that must be exceeded for a disabled DRC to become enabled, or an enabled DRC to become disabled. For example, if the DRC Threshold is set to -12dBFS and DRC Hysteresis is set to 3dB, then if the gain compressions in the DRC is inactive, the output of the DAC Digital Volume Control must exceed –9dBFS before gain compression due to the DRC is activated. Similarly, when the gain compression in the DRC is active, the output of the DAC Digital Volume Control needs to fall below -15dBFS for gain compression in the DRC to be deactivated. The DRC Hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of DAC Digital Volume Control rapidly fluctuates in a narrow region around the programmed DRC Threshold. By programming the DRC Hysteresis as 0dB, the hysteresis action is disabled.

Recommended Value of DRC Hysteresis is 3 dB.

5.13.3.3 DRC Hold

The DRC Hold is intended to slow the start of decay for a specified period of time in response to a decrease in energy level. To minimize audible artifacts, it is recommended to set the DRC Hold time to 0 through programming Page 0, Register 69, D(6:3) = 0000.

5.13.3.4 DRC Attack Rate

When the output of the DAC Digital Volume Control exceeds the programmed DRC Threshold, the gain applied in the DAC Digital Volume Control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called Attack. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the Attack Rate programmable via Page 0, Register 70, D(7:4). Attack Rates can be programmed from 4dB gain change per 1/DAC_FS to 1.2207e-5dB gain change per 1/DAC_FS.

Attack Rates should be programmed such that before the output of the DAC Digital Volume control can clip, the input signal should be sufficiently attenuated. High Attack Rates can cause audible artifacts, and too-slow Attack Rates may not be able to prevent the input signal from clipping.

The recommended DRC Attack Rate value is 1.9531e-4 dB per 1/DAC_FS.

5.13.3.5 DRC Decay Rate

When the DRC detects a reduction in output signal swing beyond the programmed DRC Threshold, the DRC enters a Decay state, where the applied gain in Digital Volume Control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the Decay Rate programmed through Page 0, Register 70, D(3:0). The Decay Rates can be programmed from 1.5625e-3dB per 1/DAC_FS to 4.7683e-7dB per 1/DAC_FS. If the Decay Rates are programmed too high, then sudden gain changes can cause audible artifacts. However, if it is programmed too slow, then the output may be perceived as too low for a long time after the peak signal has passed.

The recommended Value of DRC Attack Rate is 2.4414e-5 dB per 1/DAC_FS.

5.13.3.6 Example Setup for DRC

- PGA Gain = 12 dB
- Threshold = -24 dB
- Hysteresis = 3 dB
- Hold time = 0 ms
- Attack Rate = 1.9531e-4 dB per 1/DAC_FS
- Decay Rate = 2.4414e-5 dB per 1/DAC_FS

Script

```
#Go to Page 0
w 30 00 00
#DAC => 12 db gain left
w 30 41 18
#DAC => 12 db gain right
w 30 42 18
#DAC => DRC Enabled for both channels, Threshold = -24 db, Hysteresis = 3 dB
w 30 44 7F
#DRC Hold = 0 ms, Rate of Changes of Gain = 0.5 dB/Fs'
w 30 45 00
#Attack Rate = 1.9531e-4 dB/Frame , DRC Decay Rate =2.4414e-5 dB/Frame
w 30 46 B6
#Go to Page 46
w 30 00 2E
#DRC HPF
w 30 34 7F AB 00 00 80 55 00 00 7F 56 00 00
#DRC LPF
W 30 40 00 11 00 00 00 11 00 00 7F DE 00 00
```

5.14 DAC Special Functions

5.14.1 Beep Generation

A special function has also been included in the processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. This is intended for generating key-click sounds for user feedback. A default value for the sine-wave frequency, sine burst length, and signal magnitude is kept in the Tone Generator Registers Page 0/Registers 71 through 79. The sine wave generator is very flexible, and is completely register programmable via 9 registers of 8 bits each to provide many different sounds.

Two registers are used for programming the 16-bit, two's-complement, sine-wave coefficient (Page 0, Registers 76 and 77). Two other registers program the 16-bit, two's-complement, cosine-wave coefficient (Page 0, Registers 78 and 79). This coefficient resolution allows virtually any frequency of sine wave in the audio band to be generated up to DAC_FS/2.

Three registers are used to control the length of the sine burst waveform which are located on Page 0, Registers 73, 74, and 75. The resolution (bit) in the registers of the sine burst length is one sample time, so this allows great control on the overall time of the sine burst waveform. This 24-bit length timer supports 16,777,215 sample times. (For example if DAC_FS is set at 48kHz, and the registers combined value equals 96000d (01770h), then the sine burst would last exactly two seconds.)

Two registers are used to independently control the Left sine-wave volume and the Right sine-wave volume. The 6-bit digital volume control allows level control of 0dB to –63dB in one dB steps. The left-channel volume is controlled by writing to Page 0, Register 71, D(5:0). The right-channel volume is controlled by Page 0, Register 72, D(5:0). A master volume control for the left and right channel of the beep generator can be set up using Page 0, Register 72, D(7:6). The default volume control setting is 0dB, the tone generator maximum-output level.

For playing back the sine wave, the DAC must be configured with regards to clock setup and routing. The sine wave gets started by setting the Beep Generator Enable Bit (Page 1, Reg 71, D(7)=1)). After the sine wave has played for its predefined time period this bit will automatically set back to 0. While the sine wave is playing, the parameters of the beep generator cannot be changed. To stop the sine wave while it is playing set the Beep Generator Enable Bit to 0.

5.14.2 DIGITAL AUTO MUTE

The TLV320AIC3204 also incorporates a special feature, in which the DAC channel is auto-muted when a continuous stream of DC-input is detected. By default, this feature is disabled. It can be enabled by writing a non-000 value into Page 0, Register 64, D(6:4). The non-zero value controls the duration of continuous stream of DC-input before which the auto-mute feature takes effect. This feature is especially helpful for eliminating high-frequency-noise power being delivered into the load even during silent periods of speech or music.

5.14.3 Adaptive Filtering

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However the TLV320AIC3204 offers an adaptive filter mode as well. Setting Register Page 44,Reg 1, D(2)=1 will turn on double buffering of the coefficients. In this mode, filter coefficients can be updated through the host, and activated without stopping and restarting the DAC. This enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (Buffers A and B). When the DAC is running and adaptive filtering mode is turned on, setting the control bit Page 44, Reg 1, D(0)=1 switches the coefficient buffers at the next start of a sampling period. This bit is set back to 0 after the switch occurs. At the same time, the flag Page 44, Reg 1, D(1) toggles.

The flag in Page 44, Reg 1, D(1) indicates which of the two buffers is actually in use.

Page 44, Reg 1, D(1)=0: Buffer A is in use by the DAC engine, D(1)=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless to which buffer the coefficients have been written.

DAC running	Page 44, Reg 1, D(1)	Coefficient Buffer in use	Writing to	Will update
No	0	None	C1, Buffer A	C1, Buffer A
No	0	None	C1, Buffer B	C1, Buffer B
Yes	0	Buffer A	C1, Buffer A	C1, Buffer B
Yes	0	Buffer A	C1, Buffer B	C1, Buffer B
Yes	1	Buffer B	C1, Buffer A	C1, Buffer A
Yes	1	Buffer B	C1, Buffer B	C1, Buffer A

The user programmable coefficients C1 to C70 are defined on Pages 44, 45 and 46 for Buffer A and Pages 62, 63 and 64 for Buffer B.

5.15 DAC Setup

The following paragraphs are intended to guide a user through the steps necessary to configure the TLV320AIC3204 DAC.

Step 1

The system clock source (master clock) and the targeted DAC sampling frequency must be identified.

Depending on the targeted performance the decimation filter type (A, B or C) and DOSR value can be determined.

Filter A should be used for 48kHz high-performance operation, DOSR must be a multiple of 8.

Filter B should be used for up to 96kHz operations, DOSR must be a multiple of 4.

Filter C should be used for up to 192kHz operations, DOSR must be a multiple of 2.

In all cases the DOSR is limited in its range by the following condition:

2.8MHz < DOSR * DAC_FS < 6.2MHz

Based on the identified filter type and the required signal processing capabilities, the appropriate processing block can be determined from the list of available processing blocks (PRB_P1 to PRB_P25).

Based on the available master clock, the chosen DOSR and the targeted sampling rate, the clock divider values NDAC and MDC can be determined. If necessary, the internal PLL can add a large degree of flexibility.

In summary, Codec_Clkin (derived directly from the system clock source or from the internal PLL) divided by MDAC, NDAC and DOSR must be equal to the DAC sampling rate DAC_FS. The Clodec_Clkin clock signal is shared with the ADC clock generation block.

CODEC_CLKIN = NADC*MADC*DOSR*DAC_FS

To a large degree, NDAC and MDAC can be chosen independently in the range of 1 to 128. In general, NDAC should be as large as possible as long as the following condition can still be met:

MADC*DOSR/32 ≥ RC

RC is a function of the chosen processing block and is listed in Table 5-13.

The common-mode voltage setting of the device is determined by the available analog power supply and the desired PowerTune mode. This common-mode (input common-mode) value is common across the ADC, DAC and analog bypass path. The output common-mode setting is determined by the available analog power supplies (AVdd and LDOin) and the desired output-signal swing.

At this point the following device specific parameters are known:

PRB_Rx, DOSR, NADC, MADC, input and output common-mode values

If the PLL is used, the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed in the time between powering the device up and reading data from the device:

Define starting point: Set register page to 0
Initiate SW Reset

Program Clock Settings	Program PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program I^2S word length if required (e.g. 20bit) Program the processing block to be used

At this point, at the latest, analog power supply must be applied to the device (via internal LDO or external)

Program Analog Blocks	Set register Page to 1 Disable coarse AVdd generation Enable Master Analog Power Control Program Common Mode voltage Program PowerTune (PTM) mode Program Reference fast charging Program Headphone specific depop settings (in case of headphone driver used) Program routing of DAC output to the output amplifier (headphone or line out) Unmute and set gain of output driver Power up output driver

Apply waiting time determined by the de-pop settings and the soft-stepping settings of the driver gain or poll Page 1, Reg 63

Power Up DAC	Set register Page to 0 Power up DAC Channels Unmute digital volume control

A detailed example can be found in Section 5.22.

5.16 CLOCK GENERATION AND PLL

The TLV320AIC3204 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks as shown in Figure 5-40. The clocks for ADC and DA require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPI pins. The source reference clock for the codec can be chosen by programming the CODEC_CLKIN value on Page 0, Register 4, D(1:0). The CODEC_CLKIN can then be routed through highly-flexible clock dividers shown in Figure 5-40 to generate the various clocks required for the ADC and DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK or GPIO, the TLV320AIC3204 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC3204 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the processing block.

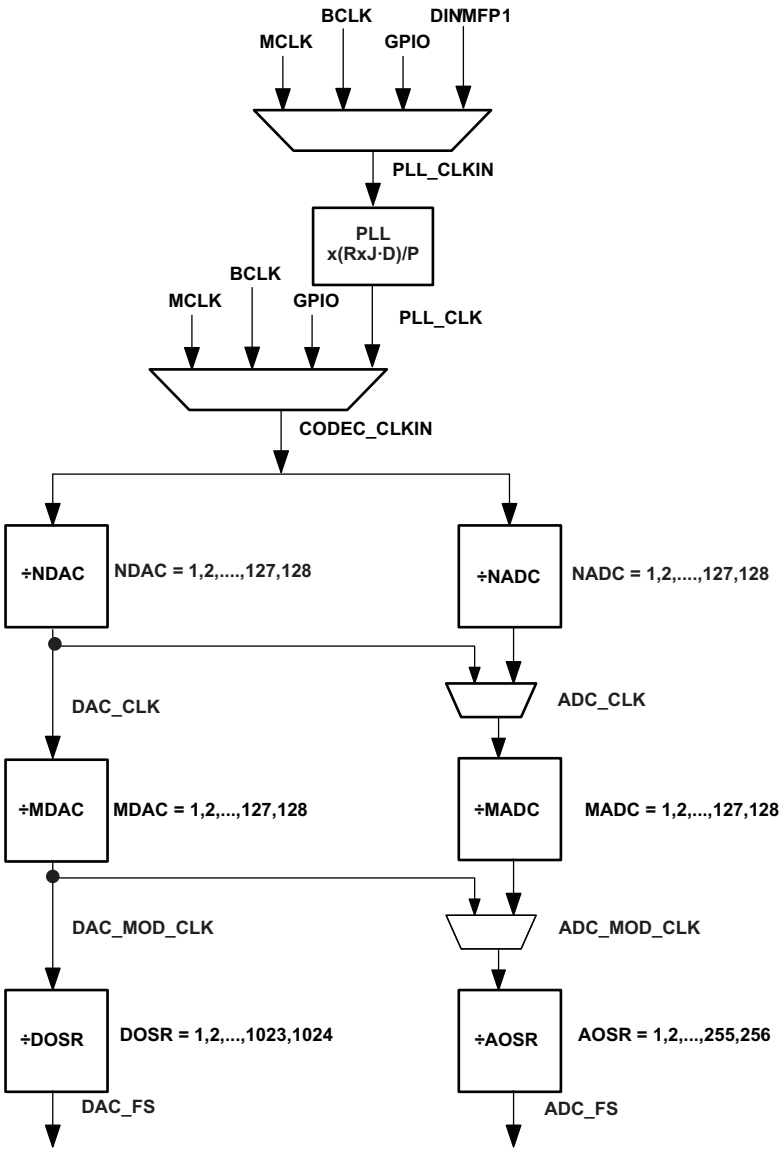


Figure 5-40. Clock Distribution Tree

$$ADC\_FS = \frac{CODEC\_CLKIN}{NADC \times MADC \times AOSR} \quad (5\text{-}13)$$

$$ADC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NADC \times MADC} \quad (5\text{-}14)$$

$$DAC\_FS = \frac{CODEC\_CLKIN}{NDAC \times MDAC \times DOSR} \quad (5\text{-}15)$$

$$DAC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NDAC \times MDAC} \quad (5\text{-}16)$$

Table 5-22. CODEC CLKIN Clock Dividers

Divider	Bits
NDAC	Page 0, Register 11, D(6:0)
MDAC	Page 0, Register 12, D(6:0)
DOSR	Page 0, Register 13, D(1:0) + Page 0, Register 14, D(7:0)

Table 5-22. CODEC CLKIN Clock Dividers (continued)

Divider	Bits
NADC	Page 0, Register 18, D(6:0)
MADC	Page 0, Register 19, D(6:0)
AOSR	Page 0, Register 20, D(7:0)

The DAC Modulator is clocked by DAC_MOD_CLK. For proper power-up operating of the DAC Channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (Page 0,Register 11, D(7) =1 and Page 0, Register 12, D(7)=1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read back the power-status flag Page 0, Register 37, D(7) and Page 0, Register 37, D(3). When both the flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider.

The ADC modulator is clocked by ADC_MOD_CLK. For proper power-up of the ADC Channel, these clocks are enabled by the NADC and MADC clock dividers (Page 0,Register 18, D(7) =1 and Page 0, Register 19, D(7)=1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NADC and MADC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read back the power-status flag Page 0, Register 36, D(6) and Page 0, Register 36, D(2). When both the flags indicate power-down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK is derived from the NDAC divider output, the NDAC must be kept powered up till the power-down status flags for ADC do not indicate power-down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_FS is needed (i.e. when WCLK is generated by TLV320AIC3204 or AGC is enabled) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, all the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.

The TLV320AIC3204 also has options for routing some of the internal clocks to the output pins of the device to be used as general purpose clocks in the system. The feature is shown in Figure 5-41.

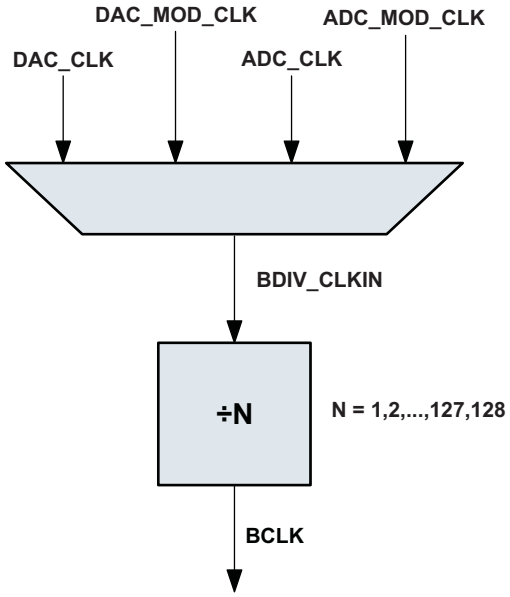


Figure 5-41. BCLK Output Options

In the mode when TLV320AIC3204 is configured to drive the BCLK pin (Page 0, Register 27, D3='1') it can be driven as divided value of BDIV_CLKIN. The division value can be programmed in Page 0, Register 30, D(6:0) from 1 to 128. The BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the BDIV_CLKIN mux in Page 0, Register 29, D(1:0). Additionally a general purpose clock can be driven out on either GPIO, DOUT or MISO pin. This clock can be a divided down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to Page 0, Register 26, D(6:0). The CDIV_CLKIN can itself be programmed as one of the clocks among the list shown in Figure 5-42. This can be controlled by programming the mux in Page 0, Register 25, D(2:0).

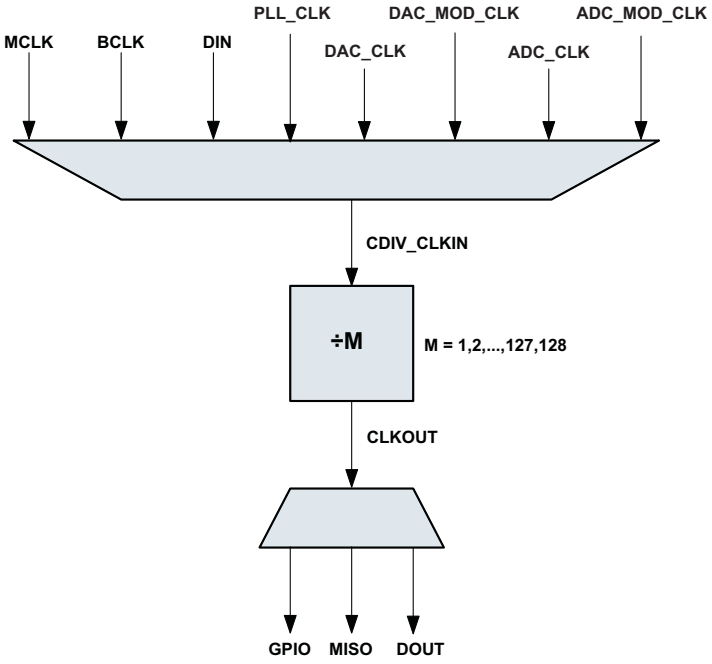


Figure 5-42. General Purpose Clock Output Options

Table 5-23. Maximum TLV320AIC3204 Clock Frequencies

	DVdd ≥ 1.26V	**DVdd ≥ 1.65V**
CODEC_CLKIN	50MHz	137MHz when NDAC is even, NADC is even 112MHz when NDAC is even, NADC is odd 110MHz when NDAC is odd, NADC is even 110MHz when NDAC is odd, NADC is odd
ADC_CLK	25MHz	55.296MHz
ADC_MOD_CLK	6.758MHz	6.758MHz
ADC_FS	0.192MHz	0.192MHz
DAC_CLK	25MHz	55.296MHz
DAC_MOD_CLK	6.758MHz 4.2MHz when Class-D Mode Headphone is used	6.758MHz
DAC_FS	0.192MHz	0.192MHz
BDIV_CLKIN	25MHz	55.296MHz
CDIV_CLKIN	50MHz	112MHz when M is odd 137MHz when M is even

5.16.1 PLL

The TLV320AIC3204 has an on chip PLL with fractional multiplication to generate the clock frequency needed by the audio ADC, DAC, and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system.

The PLL input supports clocks varying from 512kHz to 20MHz and is register programmable to enable generation of required sampling rates with fine precision. The PLL can be turned on by writing to Page 0, Register 5, D(7). When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation:

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{P} \quad (5\text{-}17)$$

R = 1, 2, 3,4

J = 4,5,6,… 63, and D = 0, 1, 2… 9999

P = 1, 2, 3… 8

R, J, D, and P are register programmable.

The PLL can be programmed via Page 0, Registers 5 thru 8. The PLL can be turned on via Page 0, Register 5, D(7). The variable P can be programmed via Page 0, Register 5, D(6:4). The default register value for P is 2. The variable R can be programmed via Page 0, Register 5, D(3:0). The default register value for R is 1. The variable J can be programmed via Page 0, Register 6, D(5:0). The variable D is 12-bits and is programmed into two registers. The MSB portion can be programmed via Page 0, Register 7, D(5:0), and the LSB portion is programmed via Page 0, Register 8, D(5:0). The default register value for D is 0.

When the PLL is enabled the following conditions must be satisfied

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512kHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (5\text{-}18)$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10MHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (5\text{-}19)$$

In TLV320AIC3204 the PLL_CLK supports a wide range of output clock, based on register settings and power-supply conditions.

Table 5-24. PLL_CLK Frequency Range

AVdd	PLL Mode Page 0, Reg 4, D6	Min PLL_CLK frequency (MHz)	Max PLL_CLK frequency (MHz)
≥1.5V	0	80	103
	1	95	110
≥1.65V	0	80	118
	1	92	123
≥1.80V	0	80	132
	1	92	137

The PLL can be powered up independent of the ADC and DAC blocks, and can also be used as a general purpose PLL by routing its output to the GPIO output. After powering up the PLL, PLL_CLK is available typically after 10ms. The PLL output frequency is controlled by J.D and R dividers

PLL Divider	Bits
J	Page 0, Register 6, D(5:0)
D	Page 0, Register 7, D(5:0) && Page 0, Register 8, D(7:0)
R	Page 0, Register 5, D(3:0)

The D-divider value is 14-bits wide and is controlled by 2 registers. For proper update of the D-divider value, Page 0, Register 7 must be programmed first followed immediately by Page 0, Register 8. Unless the write to Page 0, Register 8 is completed, the new value of D will not take effect.

The clocks for codec and various signal processing blocks, CODEC_CLKIN can be generated from MCLK input, BCLK input, GPIO input or PLL_CLK (Page 0/Register 4/D(1:0)).

If the CODEC_CLKIN is derived from the PLL, then the PLL must be powered up first and powered down last.

Table 5-25 lists several example cases of typical MCLK rates and how to program the PLL to achieve a sample rate Fs of either 44.1kHz or 48kHz.

Table 5-25. PLL Example Configurations

Fs = 44.1kHz										
MCLK (MHz)	**PLLP**	**PLLR**	**PLLJ**	**PLLD**	**MADC**	**NADC**	**AOSR**	**MDAC**	**NDAC**	**DOSR**
2.8224	1	3	10	0	3	5	128	3	5	128
5.6448	1	3	5	0	3	5	128	3	5	128
12	1	1	7	560	3	5	128	3	5	128
13	1	2	4	2336	13	3	64	4	6	104
16	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	4	4100	3	5	128	3	5	128
48	4	1	7	560	3	5	128	3	5	128
Fs = 48kHz										
2.048	1	3	14	0	2	7	128	7	2	128
3.072	1	4	7	0	2	7	128	7	2	128
4.096	1	3	7	0	2	7	128	7	2	128
6.144	1	2	7	0	2	7	128	7	2	128
8.192	1	4	3	0	2	8	128	4	4	128
12	1	1	7	1680	2	7	128	7	2	128
16	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	4	4800	2	7	128	7	2	128
48	4	1	7	1680	2	7	128	7	2	128

5.17 INTERFACE

5.17.1 AUDIO DIGITAL I/O INTERFACE

Audio data is transferred between the host processor and the TLV320AIC3204 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3204 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30 (see Figure 5-40). The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3204s may share the same audio bus.

The TLV320AIC3204 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The TLV320AIC3204 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The TLV320AIC3204 further includes programmability (Page 0, Register 27, D0) to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a 3-state output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC3204, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

5.17.1.1 Right Justified Mode

The Audio Interface of the TLV320AIC3204 can be put into Right Justified Mode by programming Page 0, Register 27, D(7:6) = 10. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

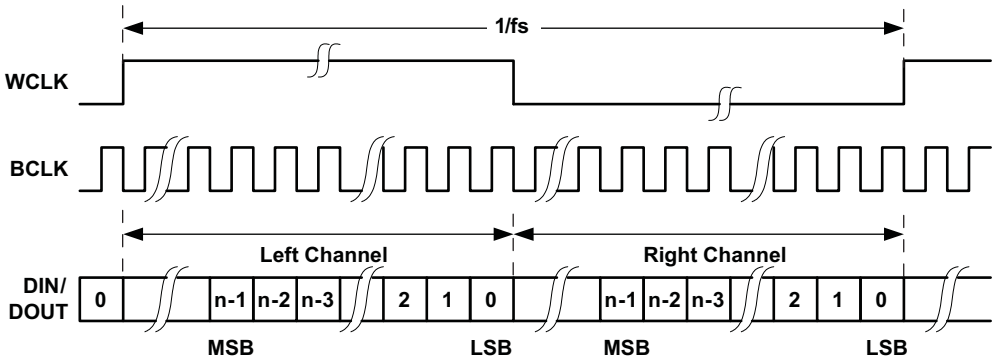


Figure 5-43. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

5.17.1.2 Left Justified Mode

The Audio Interface of the TLV320AIC3204 can be put into Left Justified Mode by programming Page 0, Register 27, D(7:6) = 11. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

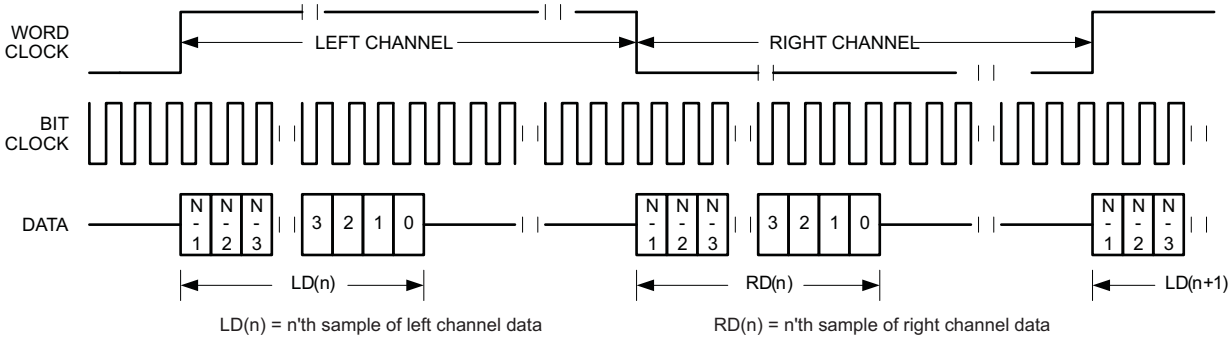


Figure 5-44. Timing Diagram for Left-Justified Mode

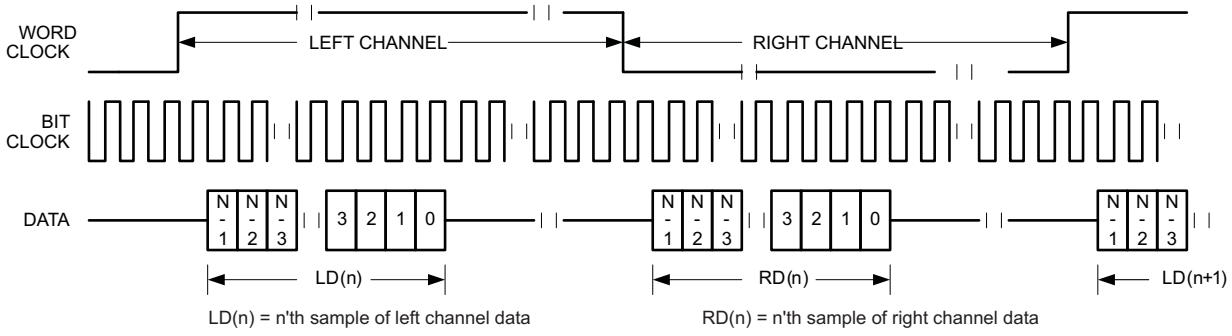


Figure 5-45. Timing Diagram for Left-Justified Mode with Offset=1

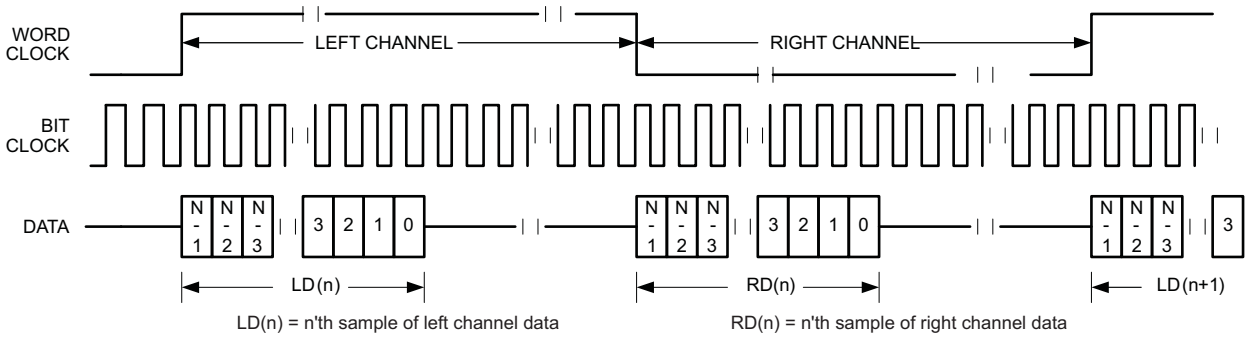


Figure 5-46. Timing Diagram for Left-Justified Mode with Offset=0 and inverted bit clock

For Left-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.3 I²S Mode

The Audio Interface of the TLV320AIC3204 can be put into Right Justified Mode by programming Page 0, Register 27, D(7:6) = to 00. In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

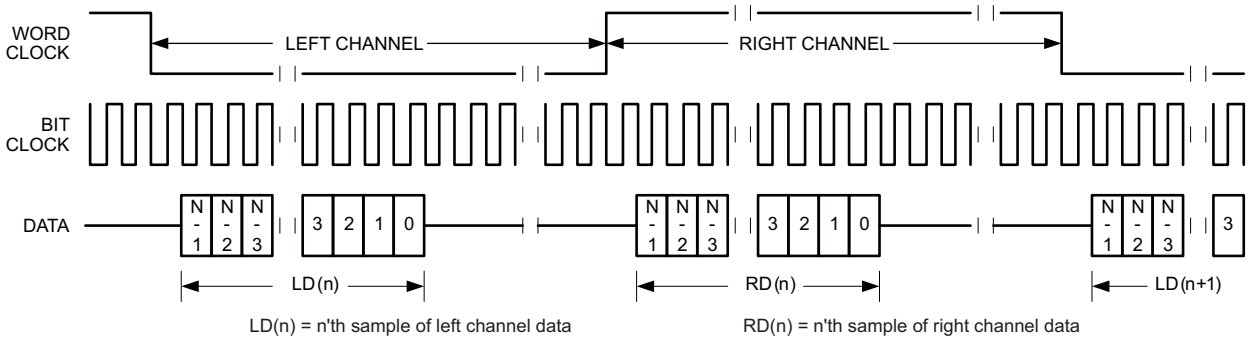


Figure 5-47. Timing Diagram for I²S Mode

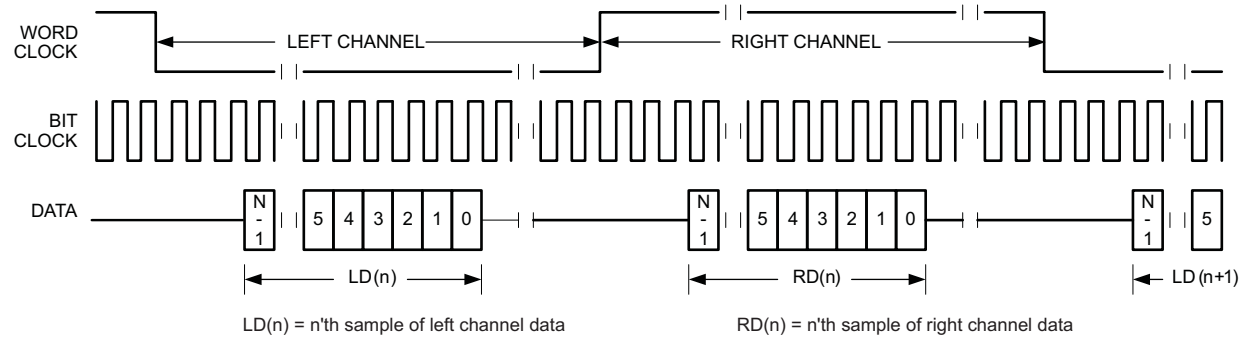


Figure 5-48. Timing Diagram for I²S Mode with offset=2

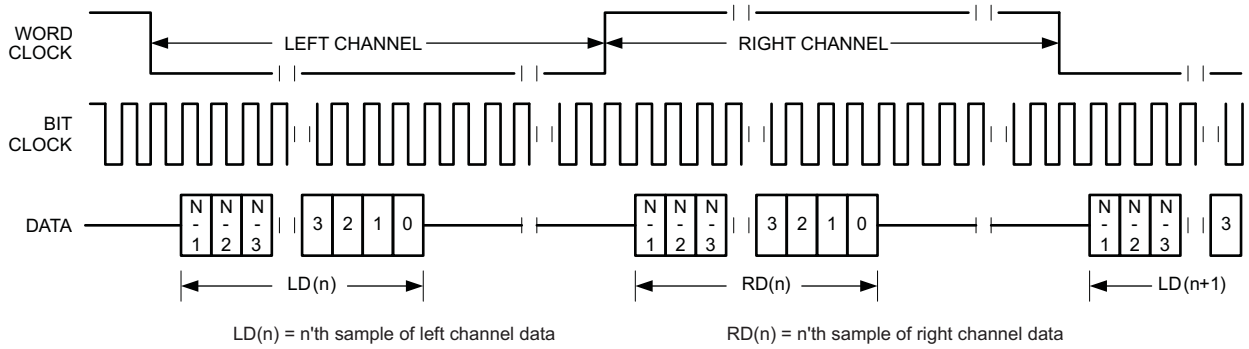


Figure 5-49. Timing Diagram for I²S Mode with offset=0 and bit clock invert

For I²S mode, the number of bit-clocks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.4 DSP Mode

The Audio Interface of the TLV320AIC3204 can be put into Right Justified Mode by programming Page 0, Register 27, D(7:6) = 01. In DSP mode, the falling edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

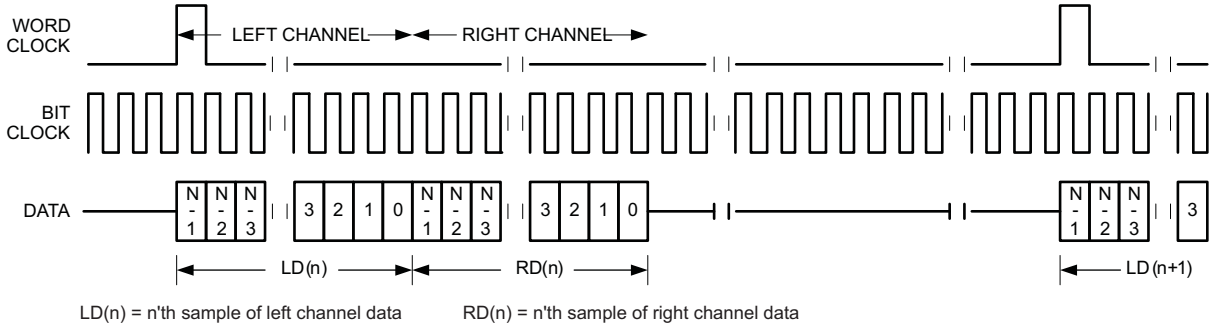


Figure 5-50. Timing Diagram for DSP Mode

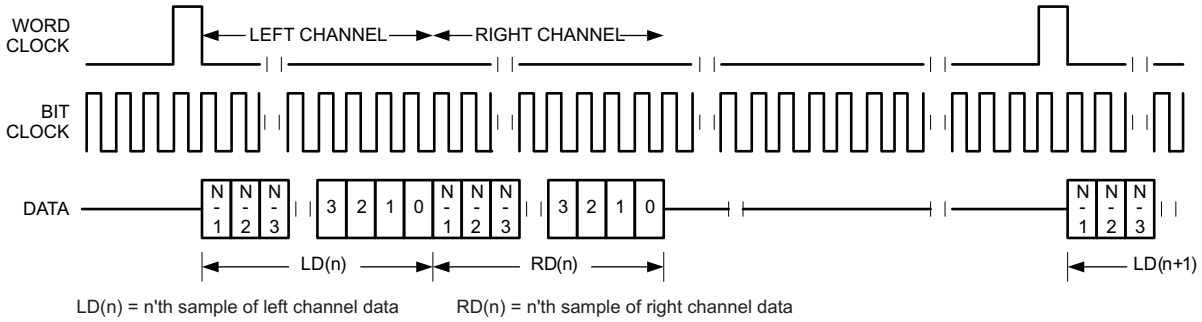


Figure 5-51. Timing Diagram for DSP Mode with offset = 1

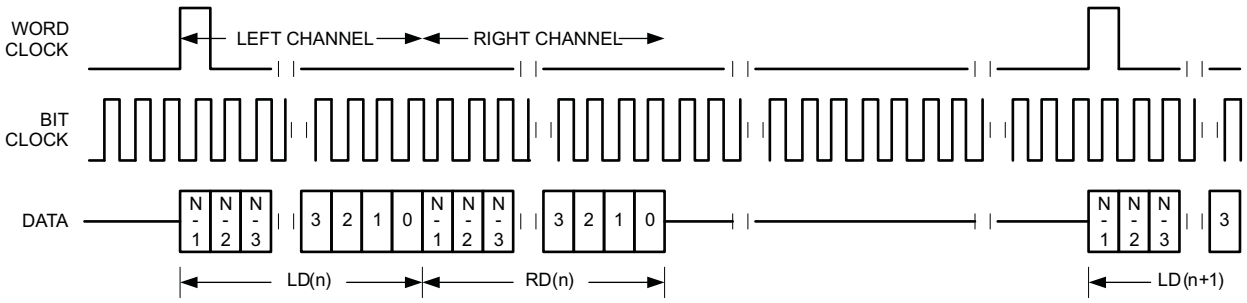


Figure 5-52. Timing Diagram for DSP Mode with offset = 1 and bit clock inverted

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

5.17.1.5 Secondary I^{2}S

The audio serial interface on the TLV320AIC3204 has an extensive IO control to allow communication with two independent processors for audio data. Each processor can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections.

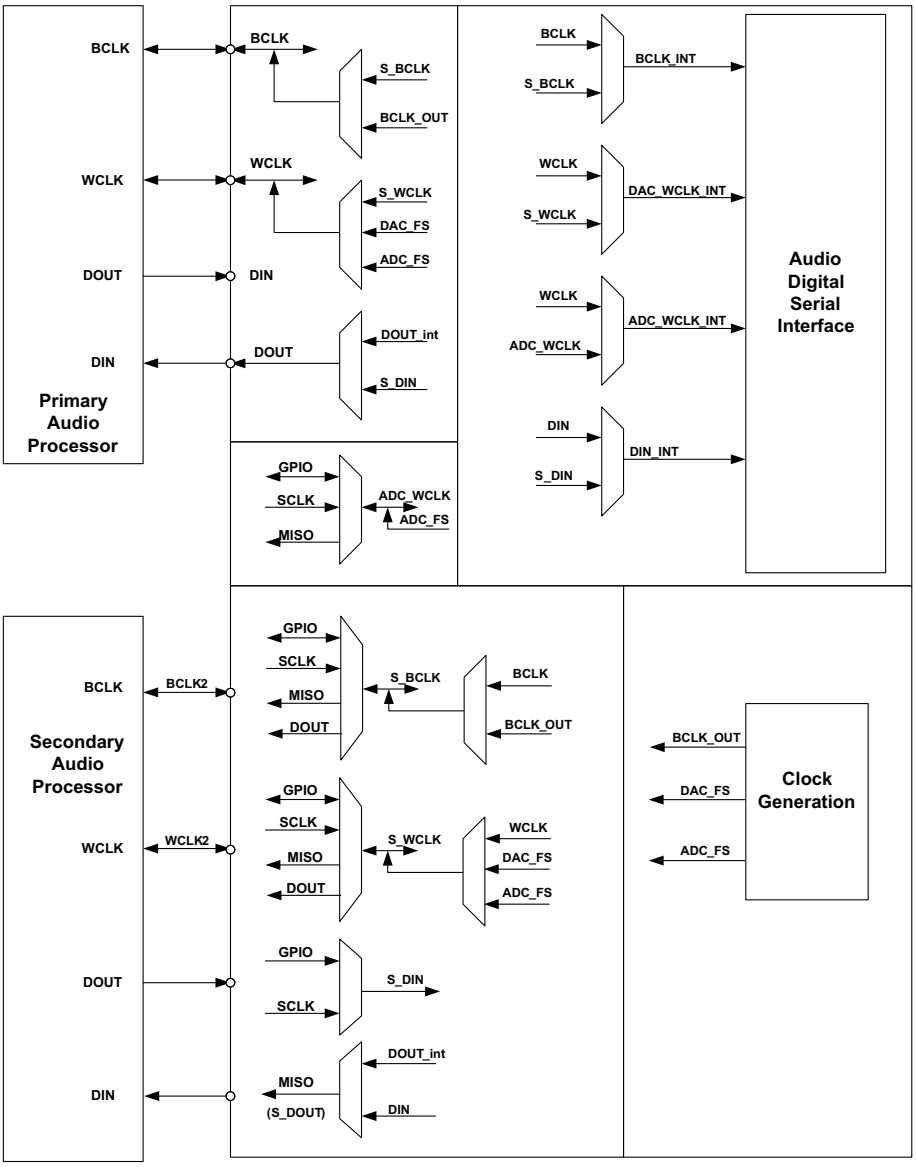


Figure 5-53. Audio Serial Interface Multiplexing

The secondary audio interface uses multifunction pins. For an overview on multifunction pins please see Section 5.2.5. Figure 5-53 illustrates possible audio interface routing. The multifunction pins SCLK and MISO are only available in I^2C communication mode.

This multiplexing capability allows the TLV320AIC3204 to communicate with two separate devices with independent I^2S/PCM busses, one at a time.

5.17.2 CONTROL INTERFACE

The TLV320AIC3204 control interface supports SPI or I^2C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^2C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

5.17.2.1 I²C CONTROL MODE

The TLV320AIC3204 supports the I²C control protocol, and will respond to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I²C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I²C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I²C devices can act as masters or slaves, but the TLV320AIC3204 can only act as a slave device.

An I²C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I²C bus in groups of eight bits. To send a bit on the I²C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver's shift register.

The I²C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I²C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I²C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I²C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not–acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3204 can also respond to and acknowledge a General Call, which consists of the master issuing a command with a slave address byte of 00H. This feature is disabled by default, but can be enabled via Page 0, Register 34, Bit D(5).

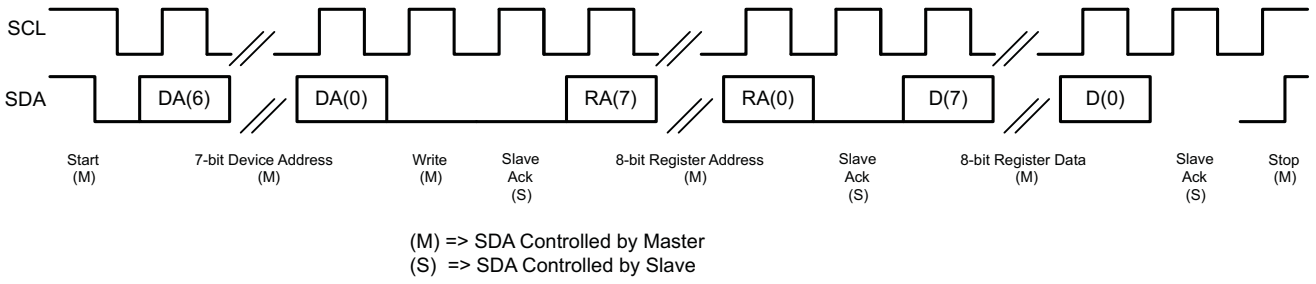


Figure 5-54. I²C Write

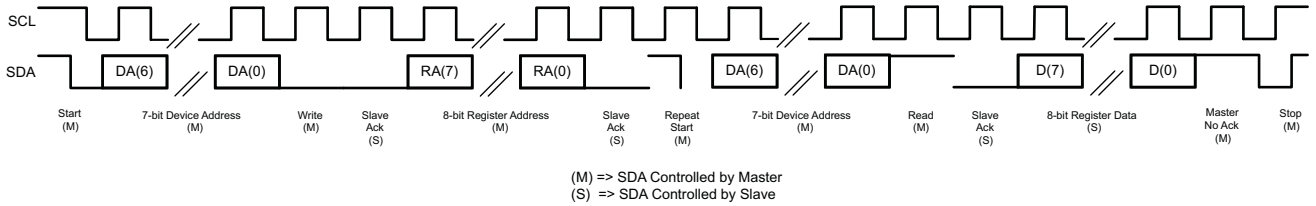


Figure 5-55. I²C Read

In the case of an I²C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I²C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

5.17.2.2 SPI DIGITAL INTERFACE

In the SPI control mode, the TLV320AIC3204 uses the pins SCL/SSZ=SSZ, SCLK=SCLK, MISO=MISO, SDA/MOSI=MOSI as a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3204) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The TLV320AIC3204 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The SSZ pin can remain low between transmissions; however, the TLV320AIC3204 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TLV320AIC3204 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI pin of the part prior to the data for that register. The command is structured as shown in Section 5.17.2.3. The first 7 bits specify the register address which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI pin and contains the data to be written to the register. Reading of registers is accomplished in similar fashion. The 8-bit command word sends the 7-bit register address, followed by R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO pin during the second 8 SCLK clocks in the frame.

Table 5.17.2.3.

COMMAND WORD

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

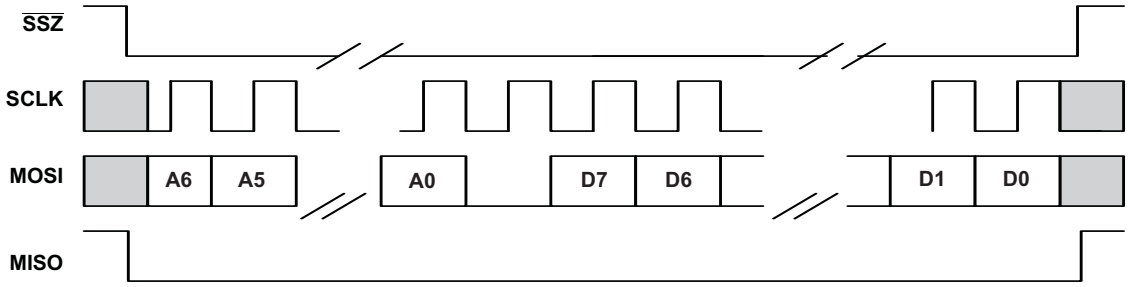


Figure 5-56. SPI Timing Diagram for Register Write

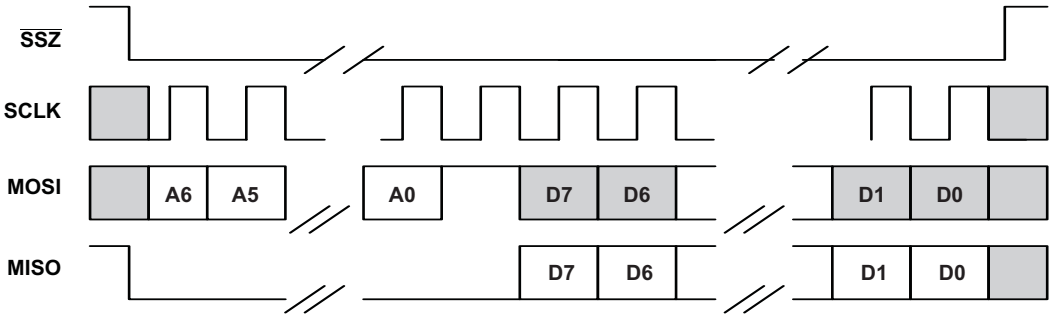


Figure 5-57. SPI Timing Diagram for Register Read

5.18 POWER

The TLV320AIC3204 has four power-supply connections which allow various optimizations for low system power. The four supply pins are LDOin, DVdd, AVdd and IOVDD.

- **IOVdd** - The IOVdd pin supplies the digital IO cells of the device. The voltage of IOVdd can range from 1.1 to 3.6V and is determined by the digital IO voltage of the rest of the system.
- **DVdd** - This pin is either a supply input to the device, or if the internal LDO is used it is used to connect an external capacitor. It supplies the digital core of the device. Lower DVdd voltages cause lower power dissipation. If efficient switched-mode power supplies are used in the system, system power can be optimized using low DVdd voltages. The device will offer full functionality up to the highest specified clock frequencies for DVdd values of 1.65 to 1.95V.
- **AVdd** - This pin is either a supply input to the device, or if the internal LDO is used it is used to connect an external capacitor. It supplies the analog core of the device. The analog core voltage (AVdd) may be in the range of 1.5 to 1.95V for specified performance. For AVdd voltages above 1.8V, the internal common mode voltage can be set to 0.9V (Pg 1, Reg 10, D(6)=0, default) resulting in 500mVrms full-scale voltage internally. For AVdd voltages below 1.8V, the internal common mode voltage should be set to 0.75V (Pg 1, Reg 10, D(6)=1), resulting in 375mVrms internal full scale voltage. At powerup, AVDD is weakly connected to DVDD. This coarse AVDD generation must be turned off by writing Pg 1, Reg 1, D(3) = 1 at the time AVDD is applied, either from internal LDO or through external LDO.
- **LDOin** - The LDOin pin serves two main functions. It serves as supply to internal LDOs as well as to the analog-output amplifiers of the device. The LDOin voltage can range from 1.9V to 3.6V. In conjunction with the two internal LDOs for AVdd and DVdd the device can run from a single supply.

For cases where high output voltages from the line out amplifiers (1Vrms) or high output power from the headphone amplifier is required, the LDOin voltage is used as a supply.

5.18.1 System Level Considerations

While there is flexibility in supplying the device through multiple options of power supplies, care must be taken to stay within safe areas when going to standby and shutdown modes.

In summary, the lowest shutdown current is achieved when all supplies to the device are turned off, implying that all settings must be reapplied to the device after bringing the power back up. In order to retain settings in the device, the DVdd voltage and either internally or externally the AVdd voltage also must be maintained. In this case the TLV320AIC3204 exhibits shutdown currents of below 1μA.(If DVdd is generated by internal LDO, add 50μA)

5.18.1.1 Supply from single voltage rail (1.9 to 3.6V)

The device can be powered directly from a single 3.3V rail through the LDOin pin. During operation the DVdd LDO is activated via the LDO_select pin, and the AVdd LDO is activated via control registers (Pg 1, Reg 2, D(0)=1).

5.18.1.1.1 Standby Mode (3.3V operation)

To put the device in standby mode, the AVdd and DVdd LDOs as well as the Reference Block (Pg 1, Reg 123, D(2:0) = 101) must stay on, and all other blocks powered down. This results in a standby current of approximately 180μA. In standby mode, the device responds quickly to playback requests.

5.18.1.1.2 Sleep Mode (3.3V operation)

In this mode all settings and memory content of the device are retained. To put the device into sleep mode, the DVdd LDO must remain powered up (LDO_select pin), the AVdd LDO must be powered down (Pg 1, Reg 2, D(0)=0), the crude AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0) and the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1). The sleep-mode power consumption is approximately 50μA

5.18.1.1.3 Shutdown Mode

To shutdown the device, the external supply can be turned off completely.

5.18.1.2 Supply from single voltage rail (1.8V).

If a single 1.8V rail is used, generating the 1.8V from a higher battery voltage via a DC-DC converter results in good system-level efficiency. In this setup, the line-output voltage is limited to 500mVrms, and the maximum headphone output power is 15mW into 16Ω.

The 1.8V rail can be connected directly to the DVdd pin (LDO_select pin connected to ground) and also supply the digital core voltage. Connecting the 1.8V rail to the AVdd pin will make the device function, but the achievable performance is a function of the voltage ripple typically found on DC-DC converter outputs. To achieve specified performance, an external low-input-voltage 1.6V LDO must be connected between the 1.8V rail and the AVdd input.

During operation, the DVdd and AVdd LDOs are deactivated (LDO_select pin and via control register Pg 1, Reg 2, D(0)=0). In this case the LDOin pin should be connected to DVdd.

5.18.1.2.1 Standby Mode (1.8V operation)

To put the device in standby mode, both external voltages (AVdd and DVdd) and the reference block inside the TLV320AIC3204 must stay on (Pg 1, Reg 123, D(2:0) = 101), all other blocks should be powered down. This results in standby current of approximately 50μA.

In standby mode the device responds very quickly to playback requests.

5.18.1.2.2 Sleep Mode (1.8V operation)

In this mode, all settings and memory content of the device is retained. To put the device into sleep mode, the external DVdd must remain powered up, the external AVdd LDO must be powered down, the crude AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0) and the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1). The device's sleep mode power consumption in this case is < 1µA

5.18.1.2.3 Shutdown Mode

To shut down the device, the external supplies can be turned off completely. If the 1.8V rail cannot be turned off, the crude AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0) and the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1). This results in a device shutdown current < 1µA.

5.18.1.3 Other Supply Options

There are other options to power the device. Apply the following rules:

- During normal operation all supply pins must be connected to a supply (via internal LDO or external)
- Whenever the LDOin supply is present,
  - DVdd supply must be present as well
  - If AVdd supply is not present, then the crude internal AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0)
- Whenever the DVdd supply is on, and either AVdd or LDOin or both supplies are off, the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1)

5.19 REFERENCE

All data converters require a DC reference voltage. The TLV320AIC3204 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with a good PSRR performance. This reference voltage must be filtered externally using a minimum 1µF capacitor connected from the REF pin to analog ground (AVss).

To achieve low power consumption, this reference block is powered down when all analog blocks inside the device are powered down. In this condition, the REF pin is 3-stated. On powerup of any analog block, the reference block is also powered up and the REF pin settles to its steady-state voltage after the settling time (a function of the de-coupling capacitor on the REF pin). This time is approximately equal to 1 second when using a 1µF decoupling capacitor. In the event that a faster power-up is required, either the reference block can be kept powered up (even when no other analog block is powered up) by programming Page 1, Register 123, D(2) = 1. However, in this case, an additional 125µA of current from DVdd and 105µA of current from AVdd is consumed. Additionally, to achieve a faster powerup, a fast-charge option is also provided where the charging time can be controlled between 40ms and 120ms by programming Page 1, Register 123, D(1:0). By default, the fast charge option is disabled.

5.20 SETTING DEVICE COMMON MODE

The TLV320AIC3204 allows the user to set the common mode voltage for analog inputs to 0.75V or 0.9V by programming Page 1, Register 10, D(6). The input common-mode voltage of 0.9V works best when the analog supply voltage is centered around 1.8V or above, and offers the highest possible performance. For analog supply voltages below 1.8V, a common mode voltage of 0.75V must be used.

Table 5-26. Input Common Mode voltage and Input Signal Swing

Input Common Mode Voltage (V)	AVdd (V)	Channel Gain (dB)	Single-Ended Input Swing for 0dBFS output signal (V_{RMS})	Differential Input Swing for 0dBFS output signal (V_{RMS})
0.75	>1.5	0	0.375	0.75
0.90	1.8 … 1.95	0	0.5	1.0

The choice of input common mode of 0.75V allows the use of PowerTune mode PTM_R1 which results in significantly lower power dissipation. (see Section 5.5) An input common-mode voltage of 0.9V allows the user to maximize the signal swings and SNR.

NOTE

The input common mode setting is common for ADC record, DAC playback and Analog Bypass path

5.21 DEVICE SPECIAL FUNCTIONS

5.21.1 Headset Detection

The TLV320AIC3204 includes extensive capability to monitor a headphone, microphone, or headset jack, to determine if a plug has been inserted into the jack, and then determine what type of headset/headphone is wired to the plug. The device also includes the capability to detect a button press, even, for example, when starting calls on mobile phones with headsets. This feature is available while using I^2C protocol for control interface. The figure shows the circuit configuration to enable this feature.

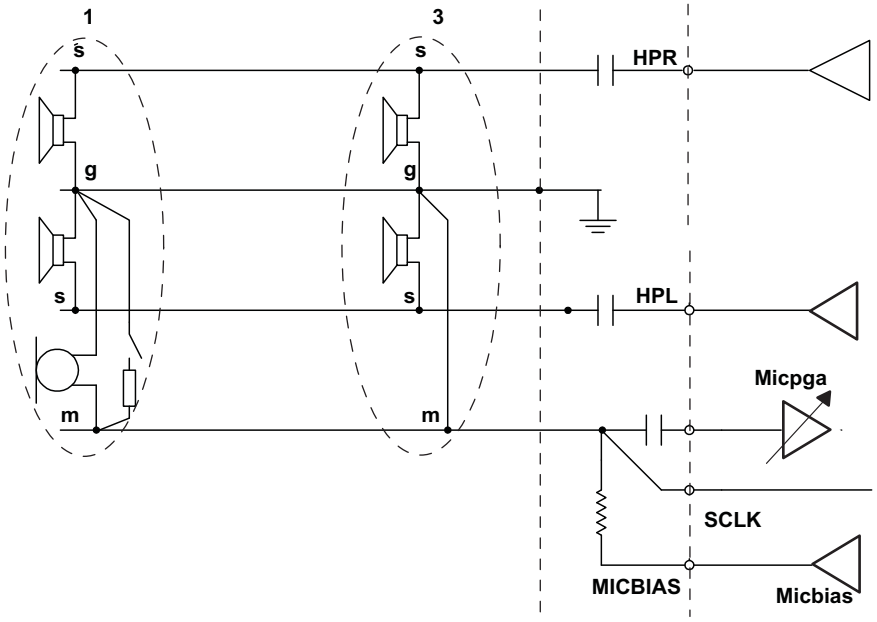


Figure 5-58. Jack Connections for Headset Detection

This feature is enabled by programming Page 0, Register 67, D(1). In order to avoid false detections due to mechanical vibrations in headset jacks or microphone buttons, a debounce function is provided for glitch rejection. For the case of headset insertion, a debounce function with a range of 32ms - 512ms is provided. This can be programmed via Page 0, Register 67, D(4:2). For improved button-press detection, the debounce function has a range of 8ms to 32ms by programming Page 0, Register 67, D(1:0).

The TLV320AIC3204 also provides feedback to user when a button press, or a headset insertion/removal event is detected through register readable flags as well as an interrupt on the IO pins. The value in Page 0, Register 45, D(5:4) provides the instantaneous state of button press and headset insertion. Page 0, Register 44, D(5) is a sticky (latched) flag that is set when the button-press event is detected. Page 0, Register 44, D(4) is a sticky flag which is set when the headset insertion or removal event is detected. These sticky flags are set by the event occurrence, and are reset only when read. This requires polling Page 0, Register 44. To avoid polling and the associated overhead, the TLV320AIC3204 also provides an interrupt feature where the events can trigger the INT1 and/or INT2 interrupts. These interrupt events can be routed to one of the digital output pins. Please refer to Section 5.21.2 for details.

The TLV320AIC3204 not only detects a headset insertion event, but also is able to distinguish between the different headsets inserted such as stereo headphones or cellular headphones. After the headset-detection event, the user can read Page 0, Register 67, D(6:5) to determine the type of headset inserted.

Table 5-27. Headset Detection Block Registers

Register	Description
Page 0, Register 67, D(1)	Headset Detection Enable/Disable
Page 0, Register 67, D(4:2)	Debounce Programmability for Headset Detection
Page 0, Register 67, D(1:0)	Debounce Programmability for Button Press
Page 0, Register 44, D(5)	Sticky Flag for Button Press Event
Page 0, Register 44, D(4)	Sticky Flag for Headset Insertion or Removal Event
Page 0, Register 45, D(5)	Status Flag for Button Press Event
Page 0, Register 45, D(4)	Status Flag for Headset Insertion and Removal
Page 0, Register 67, D(6:5)	Flags for type of Headset Detected

The headset detection block requires AVdd to be powered and Master Analog Power control in Page 1, Register 2, D(3) to be enabled. The headset detection feature in the TLV320AIC3204 is achieved with a very low power overhead, requiring less than 20µA of additional current from AVdd supply.

5.21.2 Interrupts

Some specific events in the TLV320AIC3204 which may require host processor intervention, can be used to trigger interrupts to the host processor. This avoids polling the status-flag registers continuously. The TLV320AIC3204 has two defined interrupts; INT1 and INT2 that can be configured by programming Page 0, Register 48 and 49. A user can configure the interrupts INT1 and INT2 to be triggered by one or many events such as

- Headset Detection
- Button Press
- DAC DRC Signal exceeding Threshold
- Noise detected by AGC
- Over-current condition in headphones
- Data Overflow in ADC and DAC Processing Blocks and Filters and
- DC Measurement Data Available

Each of these INT1 and INT2 interrupts can be routed to output pins like GPIO, DOUT and MISO by configuring the respective output control registers in Page 0, Register 52, 53 and 55. These interrupt signals can either be configured as a single pulse or a series of pulses by programming Page 0, Register 48, D(0) and Page 0, Register 49, D(0). If the user configures the interrupts as a series of pulses, the events will trigger the start of pulses that will stop when the flag registers in Page 0, Register 42, 44 and 45 are read by the user to determine the cause of the interrupt.

5.22 EXAMPLE SETUPS

The following example setups can be taken directly for the TLV320AIC3204 EVM setup.

The # marks a comment line, w marks an I^2C write command followed by the device address, the I^2C register address and the value.

5.22.1 Stereo DAC Playback with 48ksps Sample Rate and High Performance.

```
Assumption
AVdd = 1.8V, DVdd = 1.8V
MCLK = 12.288MHz
Ext C = 47uF
Based on C the wait time will change.
Wait time  = N*Rpop*C + 4* Offset ramp time
```

```
Default settings used.
PLL Disabled
DOSR 128
# Initialize to Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Power up the NDAC divider with value 1
w 30 0b 81
# Power up the MDAC divider with value 2
w 30 0c 82
# Program the OSR of DAC to 128
w 30 0d 00
w 30 0e 80
# Set the word length of Audio Interface to 20bits PTM_P4
w 30 1b 10
# Set the DAC Mode to PRB_P8
w 30 3c 08
# Select Page 1
w 30 00 01
# Disable Internal Crude AVdd in presence of external AVdd supply or before
#powering up internal AVdd LDO
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the REF charging time to 40ms
w 30 7b 01
# HP soft stepping settings for optimal pop performance at power up
# Rpop used is 6k with N = 6 & soft step = 20usec. This should work with 47uF coupling
# capacitor. Can try N=5,6 or 7 time constants as well. Trade-off delay vs “pop” sound.
w 30 14 25
# Set the Input Common Mode to 0.9V and Output Common Mode for Headphone to
# Input Common Mode
w 30 0a 00
# Route Left DAC to HPL
w 30 0c 08
# Route Right DAC to HPR
w 30 0d 08
# Set the DAC PTM mode to PTM_P3/4
w 30 03 00
w 30 04 00
# Set the HPL gain to 0dB
w 30 10 00
# Set the HPR gain to 0dB
w 30 11 00
# Power up HPL and HPR drivers
w 30 09 30
# Wait for 2.5 sec for soft stepping to take effect
# Else read Page 1, Register 63d, D(7:6). When = “11” soft-stepping is complete
# Select Page 0
w 30 00 00
# Power up the Left and Right DAC Channels with route the Left Audio digital data to
# Left Channel DAC and Right Audio digital data to Right Channel DAC
w 30 3f d6
# Unmute the DAC digital volume control
w 30 40 00
```

5.22.2 Stereo DAC Playback with 48ksps Sample Rate and Low Power Mode

```
Assumption
AVdd = 1.8V, DVdd = 1.8V
MCLK = 12.288MHz
Ext C = 47µF
Based on C the wait time will change.
Wait time  = N*Rpop*C + 4* Offset ramp time
Default settings used.
PLL Disabled
# Initialize to Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Power up the NDAC divide with value 1
w 30 0b 81
```

```
# Power up the MDAC divider with value 4
w 30 0c 84
# Program the OSR of DAC to 64
w 30 0d 00
w 30 0e 40
# Set the DAC Mode to PRB_P8
w 30 3c 08
# Select Page 1
w 30 00 01
# Disable Internal Crude AVdd in presence of external AVdd supply or before
# powering up internal AVdd LDO
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the REF charging time to 40ms
w 30 7b 01
# HP soft stepping settings for optimal pop performance at power up
# Rpop used is 6k with N = 6 & soft step = 20usec. This should work with 47uF coupling
# capacitor. Can try N=5,6 or 7 time constants as well. Trade-off delay vs “pop” sound.
w 30 14 25
# Set the Input Common Mode to 0.9V and Output Common Mode for Headphone to
# Input Common Mode
w 30 0a 00
# Route Left DAC to HPL
w 30 0c 08
# Route Right DAC to HPR
w 30 0d 08
# Set the DAC PTM mode to PTM_P1
w 30 03 08
w 30 04 08
# Set the HPL gain to 0dB
w 30 10 00
# Set the HPR gain to 0dB
w 30 11 00
# Power up HPL and HPR drivers
w 30 09 30
# Wait for 2.5 sec for soft stepping to take effect
# Else read Page 1, Register 63d, D(7:6). When = “11” soft-stepping is complete
# Select Page 0
w 30 00 00
# Power up the Left and Right DAC Channels with route the Left Audio digital data to
# Left Channel DAC and Right Audio digital data to Right Channel DAC
w 30 3f d6
# Unmute the DAC digital volume control
w 30 40 00
```

5.22.3 DAC Playback Through Class-D Headphone Amplifiers

```
Power Up
# Assumption DAC_FS = 48000Hz
# MCLK = 24.576MHz
# I2S Interface in Slave Mode

# Initialize to Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
# Power up the NDAC divider with value 1
w 30 0B 81
# Power up the MDAC divider with value 4
# For Class-D mode, MDAC = I*4
w 30 0C 84
# Program the OSR of DAC to 128
w 30 0D 00
w 30 0E 80
# Set the DAC Mode to PRB_P1v
w 30 3C 01

# Select Page 1
w 30 00 01
# Disable Internal Crude AVdd in presence of external AVdd supply or before
# powering up internal AVdd LDO
w 30 01 08
```

```
# Enable Master Analog Power Control
w 30 02 00
# Set the REF charging time to 40ms
w 30 7B 01
# HP soft stepping settings for optimal pop performance at power up
# Rpop used is 6k with N = 6 & soft step = 0
w 30 14 25
# Set the Input Common Mode to 0.9V and Output Common Mode for Headphone to
# Input Common Mode
w 30 0A 00
# Route Left DAC to HPL
w 30 0C 08
# Route Right DAC to HPR
w 30 0D 08
# Unmute HPL driver
w 30 10 00
# Unmute HPR driver
w 30 11 00
# Power up HPL and HPR drivers
w 30 09 30
# switch to Page 0
w 30 00 00


# Wait for soft stepping to take effect
# L&R DAC powerup Ldata-LDAC Rdata-RDAC
w 30 3F d4
# Left and Right DAC unmuted with indep. vol. ctrl
w 30 40 00

# Wait for DAC vol ctrl soft-stepping to complete
# Select Page 1

w 30 00 01
# Enable Class-D mode for HPL output
w 30 03 C0
# Enable Class-D mode for HPR output
w 30 04 C0
# Power down HPL and HPR drivers
w 30 09 00


Power Down
# Select Page 0
w 30 00 00
# Mute the DAC digital volume control
w 30 40 0d
# Power down the DAC
W 30 3F C0
# Disable Class-D mode for HPL output
w 30 03 00
# Disable Class-D mode for HPL output
w 30 04 00
```

5.22.4 Stereo ADC with 48ksps Sample Rate and High Performance

```
Assumption
AVdd = 1.8V, DVdd = 1.8V
MCLK = 12.288MHz
Default settings used.
PLL Disabled
I2S Interface with 16bit Word Length.
AOSR 128
PRB_R1
PTM_R4

# Initialize to Page 0
w 30 00 00
# S/W Reset to initialize all registers
w 30 01 01
# Power up NADC divider with value 1
w 30 12 81
# Power up MADC divider with value 2
```

```
w 30 13 82
# Program OSR for ADC to 128
w 30 14 80
# Select ADC PRB_R1
w 30 3d 01
# Select Page 1
w 30 00 01
# Disable Internal Crude AVdd in presence of external AVdd supply or before
# powering up internal AVdd LDO
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the input common mode to 0.9V
w 30 0a 00
# Select ADC PTM_R4
w 30 3d 00
# Set MicPGA startup delay to 3.1ms
w 30 47 32
# Set the REF charging time to 40ms
w 30 7b 01
# Route IN1L to LEFT_P with 20K input impedance
w 30 34 80
# Route Common Mode to LEFT_M with impedance of 20K
w 30 36 80
# Route IN1R to RIGHT_P with input impedance of 20K
w 30 37 80
# Route Common Mode to RIGHT_M with impedance of 20K
w 30 39 80
# Unmute Left MICPGA, Gain selection of 6dB to make channel gain 0dB
# Register of 6dB with input impedance of 20K => Channel Gain of 0dB
w 30 3b 0c
# Unmute Right MICPGA, Gain selection of 6dB to make channel gain 0dB
# Register of 6dB with input impedance of 20K => Channel Gain of 0dB
w 30 3c 0c
# Select Page 0
w 30 00 00
# Power up Left and Right ADC Channels
w 30 51 c0
# Unmute Left and Right ADC Digital Volume Control.
w 30 52 00
```

5.22.5 Stereo ADC with 48ksps Sample Rate and Low Power

```
Assumption
AVdd = 1.8V, DVdd = 1.8V
MCLK = 12.288MHz
Default settings used.
PLL Disabled
I2S Interface with 16bit Word Length.

# Initialize to Page 0
w 30 00 00
# S/W Reset to initialize all registers
w 30 01 01
# Power up NADC divider with value 1
w 30 12 81
# Power up MADC divider with value 4
w 30 13 84
# Program OSR for ADC to 64
w 30 14 40
# Select ADC PRB_R7
w 30 3d 07
# Select Page 1
w 30 00 01
# Disable Internal Crude AVdd in presence of external AVdd supply or before
#powering up internal AVdd LDO
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the input common mode to 0.75V
w 30 0a 40
# Select ADC PTM_R1
w 30 3d ff
```

```
# Set MicPGA startup delay to 3.1ms
w 30 47 32
# Set the REF charging time to 40ms
w 30 7b 01
# Route IN1L to LEFT_P with 20K input impedance
w 30 34 80
# Route Common Mode to LEFT_M with impedance of 20K
w 30 36 80
# Route IN1R to RIGHT_P with input impedance of 20K
w 30 37 80
# Route Common Mode to RIGHT_M with impedance of 20K
w 30 39 80
# Unmute Left MICPGA, Gain selection of 6dB to make channel gain 0dB
# Register of 6dB with input impedance of 20K => Channel Gain of 0dB
w 30 3b 0c

# Unmute Right MICPGA, Gain selection of 6dB to make channel gain 0dB
# Register of 6dB with input impedance of 20K => Channel Gain of 0dB
w 30 3c 0c
# Select Page 0
w 30 00 00
# Power up Left and Right ADC Channels
w 30 51 c0
# Unmute Left and Right ADC Digital Volume Control.
w 30 52 00
```

6 REGISTER MAP

The TLV320AIC3204 contains 38 pages of 8-bit registers, each page can contain up to 128 registers. The register pages are divided up based on functional blocks for this device. Page 0 is the default “home” page after hardware reset.

6.1 Register Map Summary

Table 6-1. Summary of Register Map

PAGE NO.	DESCRIPTION
0	Configuration for Serial Interface, Digital IO, Clocking
1	Configuration for Analog PGA’s, ADC, DAC, Output.Drivers, Volume controls etc
2-7	Reserved
8	ADC adaptive filtering control and Coefficient Buffer-A (0:29). Refer to Table 6-3 and Table 6-4 for more details.
9-10	ADC Coefficient Buffer-A (30:63). Refer to Table 6-3 and Table 6-4 for more details.
11-25	Reserved.
26-28	ADC Coefficient Buffer-B (0:63). Refer to Table 6-2 and Table 6-4 for more details.
29-43	Reserved.
44	DAC adaptive filtering control and Coefficient Buffer-A (0:29). Refer to Table 6-5 and Table 6-7 for more details.
45-46	DAC Coefficient BufferA (30:76). Refer Table 6-5 and Table 6-7 for more details.
47-61	Reserved.
62-64	DAC Coefficient BufferB C(0:76). Refer Table 6-6 and Table 6-7 for more details.

6.2 Register Map Details

6.2.1 Page 0 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.2 Page 0 / Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R	0000 000	Reserved, Write only default values
D0	W	0	Self clearing software reset bit 0: Don't care 1: Self clearing software reset

6.2.3 Page 0 / Register 2: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0XXX 0XXX	Reserved, Write only default values

6.2.4 Page 0 / Register 3: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values to this register

6.2.5 Page 0 / Register 4: Clock Setting Register 1, Multiplexers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved, Write only default values
D6	R/W	0	Select PLL Range 0: Low PLL Clock Range 1: High PLL Clock Range
D5–D4	R	00	Reserved, Write only default values any other value than reset value.
D3–D2	R/W	00	Select PLL Input Clock 00: MCLK pin is input to PLL 01: BCLK pin is input to PLL 10: GPIO pin is input to PLL 11: DIN pin is input to PLL
D1–D0	R/W	00	Select CODEC_CLKIN 00: MCLK pin is CODEC_CLKIN 01: BCLK pin is CODEC_CLKIN 10: GPIO pin is CODEC_CLKIN 11: PLL Clock is CODEC_CLKIN

6.2.6 Page 0 / Register 5: Clock Setting Register 2, PLL P&R Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Power Up 0: PLL is powered down 1: PLL is powered up
D6–D4	R/W	001	PLL divider P Value 000: P=8 001: P=1 010: P=2 … 110: P=6 111: P=7
D3–D0	R/W	0001	PLL divider R Value 000: Reserved, do not use 001: R=1 010: R=2 011: R=3 100: R=4 101…111: Reserved, do not use

6.2.7 Page 0 / Register 6: Clock Setting Register 3, PLL J Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values any value other than default
D5–D0	R/W	00 0100	PLL divider J value 00 0000…00 0011: Do not use 00 0100: J=4 00 0101: J=5 … 11 1110: J=62 11 1111: J=63

6.2.8 Page 0 / Register 7: Clock Setting Register 4, PLL D Values (MSB)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values any value other than default

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D0	R/W	00 0000	PLL divider D value (MSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: This register will be updated only when the Page-0, Reg-8 is written immediately after Page-0, Reg-7

6.2.9 Page 0 / Register 8: Clock Setting Register 5, PLL D Values (LSB)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL divider D value (LSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: Page-0, Reg-8 should be written immediately after Page-0, Reg-7

6.2.10 Page 0 / Register 9-10: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved, Write only default values.

6.2.11 Page 0 / Register 11: Clock Setting Register 6, NDAC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NDAC Divider Power Control 0: NDAC divider powered down 1: NDAC divider powered up
D6–D0	R/W	000 0001	NDAC Value 000 0000: NDAC=128 000 0001: NDAC=1 000 0010: NDAC=2 … 111 1110: NDAC=126 111 1111: NDAC=127 Note: Please check the clock frequency requirements in the Overview section

6.2.12 Page 0 / Register 12: Clock Setting Register 7, MDAC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MDAC Divider Power Control 0: MDAC divider powered down 1: MDAC divider powered up
D6–D0	R/W	000 0001	MDAC Value 000 0000: MDAC=128 000 0001: MDAC=1 000 0010: MDAC=2 … 111 1110: MDAC=126 111 1111: MDAC=127 Note: Please check the clock frequency requirements in the Overview section

6.2.13 Page 0 / Register 13: DAC OSR Setting Register 1, MSB Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	0000 00	Reserved. Write only default values
D1–D0	R/W	00	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register is updated when Page-0, Reg-14 is written to immediately after Page-0, Reg-13 Note: DOSR should be a multiple of 2 while using DAC Filter Type A, Multiple of 4 while using DAC Filter Type B and Multiple of 8 while using DAC Filter Type C

6.2.14 Page 0 / Register 14: DAC OSR Setting Register 2, LSB Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: Reserved. Do not use 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: Reserved. Do not use Note: This register should be written immediately after Page-0, Reg-13 Note: DOSR should be a multiple of 2 while using DAC Filter Type A, Multiple of 4 while using DAC Filter Type B and Multiple of 8 while using DAC Filter Type C

6.2.15 Page 0 / Register 15: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0010	Reserved. Write only default value

6.2.16 Page 0 / Register 16: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Write only default value

6.2.17 Page 0 / Register 17: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 1000	Reserved. Write only default values

6.2.18 Page 0 / Register 18: Clock Setting Register 8, NADC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NADC Clock Divider Power Control 0: NADC divider powered down, ADC_CLK is same as DAC_CLK 1: NADC divider powered up
D6–D0	R/W	000 0001	NADC Value 000 0000: NADC=128 000 0001: NADC=1 … 111 1110: NADC=126 111 1111: NADC=127 Note: Pls check the clock frequency requirements in the Overview section

6.2.19 Page 0 / Register 19: Clock Setting Register 9, MADC Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MADC Clock Divider Power Control 0: MADC divider powered down, ADC_MOD_CLK is same as DAC_MOD_CLK 1: MADC divider powered up
D6–D0	R/W	000 0001	MADC Value 000 0000: MADC=128 000 0001: MADC=1 … 111 1110: MADC=126 111 1111: MADC=127 Note: Pls check the clock frequency requirements in the Overview section

6.2.20 Page 0 / Register 20: ADC Oversampling (AOSR) Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001-0001 1111: Reserved. Do not use 0010 0000: ADC AOSR=32 (Use with PRB_R13 to PRB_R18, ADC Filter Type C) 0010 0001-0011 1111: Reserved.Do not use 0100 0000: AOSR=64 (Use with PRB_R1 to PRB_R12, ADC Filter Type A or B) 0100 0001-0111 1111: Reserved. Do not use 1000 0000: AOSR=128(Use with PRB_R1 to PRB_R6, ADC Filter Type A) 1000 0001-1111 1111: Reserved. Do not use

6.2.21 Page 0 / Register 21: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0001	Reserved. Write only default values

6.2.22 Page 0 / Register 22: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.23 Page 0 / Register 23: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0100	Reserved. Write only default values

6.2.24 Page 0 / Register 24: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.25 Page 0 / Register 25: Clock Setting Register 9, Multiplexers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2–D0	R/W	000	CDIV_CLKIN Clock Selection 000: CDIV_CLKIN= MCLK 001: CDIV_CLKIN= BCLK 010: CDIV_CLKIN=DIN 011: CDIV_CLKIN=PLL_CLK 100: CDIV_CLKIN=DAC_CLK 101: CDIV_CLKIN=DAC_MOD_CLK 110: CDIV_CLKIN=ADC_CLK 111: CDIV_CLKIN=ADC_MOD_CLK

6.2.26 Page 0 / Register 26: Clock Setting Register 10, CLKOUT M divider value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	CLKOUT M divider power control 0: CLKOUT M divider powered down 1: CLKOUT M divider powered up
D6–D0	R/W	000 0001	CLKOUT M divider value 000 0000: CLKOUT M divider = 128 000 0001: CLKOUT M divider = 1 000 0010: CLKOUT M divider = 2 … 111 1110: CLKOUT M divider = 126 111 1111: CLKOUT M divider = 127 Note: Please check the clock frequencies in the Overview section

6.2.27 Page 0 / Register 27: Audio Interface Setting Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Interface Selection 00: Audio Interface = I2S 01: Audio Interface = DSP 10: Audio Interface = RJF 11: Audio Interface = LJF
D5–D4	R/W	00	Audio Data Word length 00: Data Word length = 16 bits 01: Data Word length = 20 bits 10: Data Word length = 24 bits 11: Data Word length = 32 bits
D3	R/W	0	BCLK Direction Control 0: BCLK is input to the device 1: BCLK is output from the device
D2	R/W	0	WCLK Direction Control 0: WCLK is input to the device 1: WCLK is output from the device
D1	R	0	Reserved. Write only default value
D0	R/W	0	DOUT High Impendance Output Control 0: DOUT will not be high impedance while Audio Interface is active 1: DOUT will be high impedance after data has been transferred

6.2.28 Page 0 / Register 28: Audio Interface Setting Register 2, Data offset setting

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Data Offset Value 0000 0000: Data Offset = 0 BCLK's 0000 0001: Data Offset = 1 BCLK's … 1111 1110: Data Offset = 254 BCLK's 1111 1111: Data Offset = 255 BCLK's

6.2.29 Page 0 / Register 29: Audio Interface Setting Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only default values
D5	R/W	0	Loopback control 0: No Loopback 1: Audio Data in is routed to Audio Data out
D4	R/W	0	Loopback control 0: No Loopback 1: Stereo ADC output is routed to Stereo DAC input
D3	R/W	0	Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D2	R/W	0	Primary BCLK and Primary WCLK Power control 0: Primary BCLK and Primary WCLK buffers are powered up when they are used in clock generation even when the codec is powered down 1: Priamry BCLK and Primary WCLK buffers are powered down when the codec is powered down
D1–D0	R/W	00	BDIV_CLKIN Multiplexer Control 00: BDIV_CLKIN = DAC_CLK 01: BDIV_CLKIN = DAC_MOD_CLK 10: BDIV_CLKIN = ADC_CLK 11: BDIV_CLKIN = ADC_MOD_CLK

6.2.30 Page 0 / Register 30: Clock Setting Register 11, BCLK N Divider

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK N Divider Power Control 0: BCLK N divider powered down 1: BCLK N divider powered up
D6–D0	R/W	000 0001	BCLK N Divider value 0000 0000: BCLK N divider = 128 0000 0001: BCLK N divider = 1 … 1111 1110: BCLK N divider = 126 1111 1111: BCLK N divider = 127

6.2.31 Page 0 / Register 31: Audio Interface Setting Register 4, Secondary Audio Interface

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6–D5	R/W	00	Secondary Bit Clock Multiplexer 00: Secondary Bit Clock = GPIO 01: Secondary Bit Clock = SCLK 10: Secondary Bit Clock = MISO 11: Secondary Bit Clock = DOUT
D4–D3	R/W	00	Secondary Word Clock Multiplexer 00: Secondary Word Clock = GPIO 01: Secondary Word Clock = SCLK 10: Secondary Word Clock = MISO 11: Secondary Word Clock = DOUT
D2–D1	R/W	00	ADC Word Clock Multiplexer 00: ADC Word Clock = GPIO 01: ADC Word Clock = SCLK 10: ADC Word Clock = MISO 11: Do not use
D0	R/W	0	Secondary Data Input Multiplexer 0: Secondary Data Input = GPIO 1: Secondary Data Input = SCLK

6.2.32 Page 0 / Register 32: Audio Interface Setting Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3	R/W	0	Primary / Secondary Bit Clock Control 0: Primary Bit Clock(BCLK) is used for Audio Interface and Clocking 1: Secondary Bit Clock is used for Audio Interface and Clocking
D2	R/W	0	Primary / Secondary Word Clock Control 0: Primary Word Clock(WCLK) is used for Audio Interface 1: Secondary Word Clock is used for Audio Interface
D1	R/W	0	ADC Word Clock Control 0: ADC Word Clock is same as DAC Word Clock 1: ADC Word Clock is Secondary ADC Word Clock
D0	R/W	0	Audio Data In Control 0: DIN is used for Audio Data In 1: Secondary Data In is used for Audio Data In

6.2.33 Page 0 / Register 33: Audio Interface Setting Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK Output Control 0: BCLK Output = Generated Primary Bit Clock 1: BCLK Output = Secondary Bit Clock Input
D6	R/W	0	Secondary Bit Clock Output Control 0: Secondary Bit Clock = BCLK input 1: Secondary Bit Clock = Generated Primary Bit Clock
D5–D4	R/W	00	WCLK Output Control 00: WCLK Output = Generated DAC_FS 01: WCLK Output = Generated ADC_FS 10: WCLK Output = Secondary Word Clock Input 11: Do not use
D3–D2	R/W	00	Secondary Word Clock Output Control 00: Secondary Word Clock output = WCLK input 01: Secondary Word Clock output = Generated DAC_FS 10: Secondary Word Clock output = Generated ADC_FS 11: Do not use
D1	R/W	0	Primary Data Out output control 0: DOUT output = Data Output from Serial Interface 1: DOUT output = Secondary Data Input (Loopback)
D0	R/W	0	Secondary Data Out output control 0: Secondary Data Output = DIN input (Loopback) 1: Secondary Data Output = Data output from Serial Interface

6.2.34 Page 0 / Register 34: Digital Interface Misc. Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R	0	Reserved. Write only default value
D5	R/W	0	I2C General Call Address Configuration 0: I2C General Call Address will be ignored 1: I2C General Call Address accepted
D4–D0	R	0 0000	Reserved. Write only default values

6.2.35 Page 0 / Register 35: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default value

6.2.36 Page 0 / Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status Flag 0: Gain Applied in Left ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Left ADC PGA is equal to Programmed Gain in Control Register
D6	R	0	Left ADC Power Status Flag 0: Left ADC Powered Down 1: Left ADC Powered Up
D5	R	0	Left AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Left AGC is not saturated 1: Gain in Left ADC is equal to maximum allowed gain in Left AGC
D4	R	0	Reserved. Write only default value
D3	R	0	Right ADC PGA Status Flag 0: Gain Applied in Right ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Right ADC PGA is equal to Programmed Gain in Control Register
D2	R	0	Right ADC Power Status Flag 0: Right ADC Powered Down 1: Right ADC Powered Up
D1	R	0	Right AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Right AGC is not saturated 1: Gain in Right ADC is equal to maximum allowed gain in Right AGC
D0	R	0	Reserved. Write only default value

6.2.37 Page 0 / Register 37: DAC Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status Flag 0: Left DAC Powered Down 1: Left DAC Powered Up
D6	R	0	Left Line Output Driver(LOL) Power Status Flag 0: LOL Powered Down 1: LOL Powered Up
D5	R	0	Left Headphone Driver (HPL) Power Status Flag 0: HPL Powered Down 1: HPL Powered Up
D4	R	0	Reserved. Write only default values
D3	R	0	Right DAC Power Status Flag 0: Right DAC Powered Down 1: Right DAC Powered Up
D2	R	0	Right Line Output Driver(LOR) Power Status Flag 0: LOR Powered Down 1: LOR Powered Up
D1	R	0	Right Headphone Driver (HPR) Power Status Flag 0: HPR Powered Down 1: HPR Powered Up
D0	R	0	Reserved. Write only default values

6.2.38 Page 0 / Register 38: DAC Flag Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R	0	Left DAC PGA Status Flag 0: Gain applied in Left DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Left DAC PGA is equal to Gain programmed in Control Register
D3–D1	R	000	Reserved. Write only default values
D0	R	0	Right DAC PGA Status Flag 0: Gain applied in Right DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Right DAC PGA is equal to Gain programmed in Control Register

6.2.39 Page 0 / Register 39-41: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.40 Page 0 / Register 42: Sticky Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left DAC 1: Overflow has happened in Left DAC since last read of this register
D6	R	0	Right DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right DAC 1: Overflow has happened in Right DAC since last read of this register
D5–D4	R	00	Reserved. Write only default values
D3	R	0	Left ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left ADC 1: Overflow has happened in Left ADC since last read of this register
D2	R	0	Right ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right ADC 1: Overflow has happened in Right ADC since last read of this register
D1–D0	R	00	Reserved. Write only default values

6.2.41 Page 0 / Register 43: Interrupt Flag Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. 0: No overflow in Left DAC 1: Overflow condition is present in Left ADC at the time of reading the register
D6	R	0	Right DAC Overflow Status. 0: No overflow in Right DAC 1: Overflow condition is present in Right DAC at the time of reading the register
D5–D4	R	00	Reserved. Write only default values
D3	R	0	Left ADC Overflow Status. 0: No overflow in Left ADC 1: Overflow condition is present in Left ADC at the time of reading the register
D2	R	0	Right ADC Overflow Status. 0: No overflow in Right ADC 1: Overflow condition is present in Right ADC at the time of reading the register
D1–D0	R	0	Reserved. Write only default values

6.2.42 Page 0 / Register 44: Sticky Flag Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Over Current Detect Flag 0: Over Current not detected on HPL 1: Over Current detected on HPL (will be cleared when the register is read)
D6	R	0	HPR Over Current Detect Flag 0: Over Current not detected on HPR 1: Over Current detected on HPR (will be cleared when the register is read)
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected (will be cleared when the register is read)
D4	R	0	Headset Insertion/Removal Detect Flag 0: Insertion/Removal event not detected 1: Insertion/Removal event detected (will be cleared when the register is read)
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D1–D0	R	00	Reserved. Write only default values

6.2.43 Page 0 / Register 45: Sticky Flag Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved.
D6	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D5	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D4–D3	R	00	Reserved. Write only default values
D2	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D1	R	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D0	R	0	Reserved. Write only default values

6.2.44 Page 0 / Register 46: Interrupt Flag Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Over Current Detect Flag 0: Over Current not detected on HPL 1: Over Current detected on HPL
D6	R	0	HPR Over Current Detect Flag 0: Over Current not detected on HPR 1: Over Current detected on HPR
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected
D4	R	0	Headset Insertion/Removal Detect Flag 0: Headset removal detected 1: Headset insertion detected
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D1–D0	R	00	Reserved. Write only default values

6.2.45 Page 0 / Register 47: Interrupt Flag Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold
D4–D3	R	00	Reserved. Write only default values
D2	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D1	R	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D0	R	0	Reserved. Write only default values

6.2.46 Page 0 / Register 48: INT1 Interrupt Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT1 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT1 interrupt 1: Headset Insertion even will generate a INT1 interrupt
D6	R/W	0	INT1 Interrupt for Button Press Event 0: Button Press event will not generate a INT1 interrupt 1: Button Press event will generate a INT1 interrupt
D5	R/W	0	INT1 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT1 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT1 interrupt. Read Page-0, Register-44 to distinguish between Left or Right Channel
D4	R/W	0	INT1 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT1 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT1 interrupt. Read Page-0, Register-45 to distinguish between Left or Right Channel
D3	R/W	0	INT1 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT1 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT1 interrupt. Read Page-0, Register-44 to distinguish between HPL and HPR
D2	R/W	0	INT1 Interrupt for overflow event 0: ADC or DAC data overflows does not result in a INT1 interrupt 1: ADC or DAC data overflow will result in a INT1 interrupt. Read Page-0, Register-42 to distinguish between ADC or DAC data overflow
D1	R/W	0	INT1 Interrupt for DC Measurement 0: DC Measurement data available will not generate INT1 interrupt 1: DC Measurement data available will generate INT1 interrupt
D0	R/W	0	INT1 pulse control 0: INT1 is active high interrupt of 1 pulse of approx. 2ms duration 1: INT1 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read Page-0, Reg-42d, 44d or 45d

6.2.47 Page 0 / Register 49: INT2 Interrupt Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT2 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT2 interrupt 1: Headset Insertion even will generate a INT2 interrupt
D6	R/W	0	INT2 Interrupt for Button Press Event 0: Button Press event will not generate a INT2 interrupt 1: Button Press event will generate a INT2 interrupt
D5	R/W	0	INT2 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT2 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT2 interrupt. Read Page-0, Register-44 to distinguish between Left or Right Channel

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R/W	0	INT2 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT2 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT2 interrupt. Read Page-0, Register-45 to distinguish between Left or Right Channel
D3	R/W	0	INT2 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT2 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT2 interrupt. Read Page-0, Register-44 to distinguish between HPL and HPR
D2	R/W	0	INT2 Interrupt for overflow event 0: ADC or DAC data overflows does not result in a INT1 interrupt 1: ADC or DAC data overflow will result in a INT1 interrupt. Read Page-0, Register-42 to distinguish between ADC or DAC data overflow
D1	R/W	0	INT2 Interrupt for DC Measurement 0: DC Measurement data available will not generate INT2 interrupt 1: DC Measurement data available will generate INT2 interrupt
D0	R/W	0	INT2 pulse control 0: INT2 is active high interrupt of 1 pulse of approx. 2ms duration 1: INT2 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read Page-0, Reg-42d, 44d and 45d

6.2.48 Page 0 / Register 50-51: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.49 Page 0 / Register 52: GPIO/MFP5 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D2	R/W	0000	GPIO Control 0000: GPIO input/output disabled. 0001: GPIO input is used for secondary audio interface, digital microphone input or clock input. Configure other registers to choose the functionality of GPIO input 0010: GPIO is general purpose input 0011: GPIO is general purpose output 0100: GPIO output is CLKOUT 0101: GPIO output is INT1 0110: GPIO output is INT2 0111: GPIO output is ADC_WCLK for Audio Interface 1000: GPIO output is secondary bit-clock for Audio Interface 1001: GPIO output is secondary word-clock for Audio Interface 1010: GPIO output is clock for digital microphone 1011-1111: Reserved. Do not use.
D1	R	X	GPIO Input Pin state, used along with GPIO as general purpose input
D0	R/W	0	GPIO as general purpose output control 0: GPIO pin is driven to '0' in general purpose output mode 1: GPIO pin is driven to '1' in general purpose output mode

6.2.50 Page 0 / Register 53: DOUT/MFP2 Function Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	1	DOUT Bus Keeper Control 0: DOUT Bus Keeper Enabled 1: DOUT Bus Keeper Disabled

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D1	R/W	001	DOUT MUX Control 000: DOUT disabled 001: DOUT is Primary DOUT 010: DOUT is General Purpose Output 011: DOUT is CLKOUT 100: DOUT is INT1 101: DOUT is INT2 110: DOUT is Secondary BCLK 111: DOUT is Secondary WCLK
D0	R/W	0	DOUT as General Purpose Output 0: DOUT General Purpose Output is '0' 1: DOUT General Purpose Output is '1'

6.2.51 Page 0 / Register 54: DIN/MFP1 Function Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0 0000	Reserved. Write only reserved values
D2–D1	R/W	01	DIN function control 00: DIN pin is disabled 01: DIN is enabled for Primary Data Input or Digital Microphone Input or General Purpose Clock input 10: DIN is used as General Purpose Input 11: Reserved. Do not use
D0	R	X	Value of DIN input pin. To be used when for General Purpose Input

6.2.52 Page 0 / Register 55: MISO/MFP4 Function Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D1	R/W	0001	MISO function control 0000: MISO buffer disabled 0001: MISO is used for data output in SPI interface, is disabled for I2C interface 0010: MISO is General Purpose Output 0011: MISO is CLKOUT output 0100: MISO is INT1 output 0101: MISO is INT2 output 0110: MISO is ADC Word Clock output 0111: MISO is clock output for Digital Microphone 1000: MISO is Secondary Data Output for Audio Interface 1001: MISO is Secondary Bit Clock for Audio Interface 1010: MISO is Secondary Word Clock for Audio Interface 1011-1111: Reserved. Do not use
D0	R/W	0	Value to be driven on MISO pin when used as General Purpose Output

6.2.53 Page 0 / Register 56: SCLK/MFP3 Function Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0 0000	Reserved. Write only default values
D2–D1	R/W	01	SCLK function control 00: SCLK pin is disabled 01: SCLK pin is enabled for SPI clock in SPI Interface mode or when in I2C Interface enabled for Secondary Data Input or Secondary Bit Clock Input or Secondary Word Clock or Secondary ADC Word Clock or Digital Microphone Input 10: SCLK is enabled as General Purpose Input 11: Reserved. Do not use
D0	R	X	Value of SCLK input pin when used as General Purpose Input

6.2.54 Page 0 / Register 57-59: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.55 Page 0 / Register 60: DAC Signal Processing Block Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0001	Selects the ADC (recording) signal processing block 0 0000: Reserved. Do not use 0 0001: DAC Signal Processing Block PRB_P1 0 0010: DAC Signal Processing Block PRB_P2 0 0011: DAC Signal Processing Block PRB_P3 0 0100: DAC Signal Processing Block PRB_P4 … 1 1000: DAC Signal Processing Block PRB_P24 1 1001: DAC Signal Processing Block PRB_P25 1 1010-1 1111: Reserved. Do not use Note; Please check the overview section for description of the Signal Processing Modes

6.2.56 Page 0 / Register 61: ADC Signal Processing Block Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0001	0 0000: Reserved. Do not use 0 0001: ADC Singal Processing Block PRB_R1 0 0010: ADC Signal Processing Block PRB_R2 0 0011: ADC Signal Processing Block PRB_R3 0 0100: ADC Signal Processing Block PRB_R4 … 1 0001: ADC Signal Processing Block PRB_R17 1 0010: ADC Signal Processing Block PRB_R18 1 0010-1 1111: Reserved. Do not use Note: Please check the overview section for description of the Signal Processing Modes

6.2.57 Page 0 / Register 62: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.58 Page 0 / Register 63: DAC Channel Setup Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Channel Power Control 0: Left DAC Channel Powered Down 1: Left DAC Channel Powered Up
D6	R/W	0	Right DAC Channel Power Control 0: Right DAC Channel Powered Down 1: Right DAC Channel Powered Up
D5–D4	R/W	01	Left DAC Data path Control 00: Left DAC data is disabled 01: Left DAC data Left Channel Audio Interface Data 10: Left DAC data is Right Channel Audio Interface Data 11: Left DAC data is Mono Mix of Left and Right Channel Audio Interface Data
D3–D2	R/W	01	Right DAC Data path Control 00: Right DAC data is disabled 01: Right DAC data Right Channel Audio Interface Data 10: Right DAC data is Left Channel Audio Interface Data 11: Right DAC data is Mono Mix of Left and Right Channel Audio Interface Data

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	DAC Channel Volume Control's Soft-Step control 00: Soft-Stepping is 1 step per 1 DAC Word Clock 01: Soft-Stepping is 1 step per 2 DAC Word Clocks 10: Soft-Stepping is disabled 11: Reserved. Do not use

6.2.59 Page 0 / Register 64: DAC Channel Setup Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right Modulator Output Control 0: When Right DAC Channel is powered down, the data is zero. 1: When Right DAC Channel is powered down, the Right DAC Modulator output data is inverted version of Left DAC Modulator Output. Can be used when differential mono output is used
D6–D4	R/W	000	DAC Auto Mute Control 000: Auto Mute disabled 001: DAC is auto muted if input data is DC for more than 100 consecutive inputs 010: DAC is auto muted if input data is DC for more than 200 consecutive inputs 011: DAC is auto muted if input data is DC for more than 400 consecutive inputs 100: DAC is auto muted if input data is DC for more than 800 consecutive inputs 101: DAC is auto muted if input data is DC for more than 1600 consecutive inputs 110: DAC is auto muted if input data is DC for more than 3200 consecutive inputs 111: DAC is auto muted if input data is DC for more than 6400 consecutive inputs
D3	R/W	1	Left DAC Channel Mute Control 0: Left DAC Channel not muted 1: Left DAC Channel muted
D2	R/W	1	Right DAC Channel Mute Control 0: Right DAC Channel not muted 1: Right DAC Channel muted
D1–D0	R/W	00	DAC Master Volume Control 00: Left and Right Channel have independent volume control 01: Left Channel Volume is controlled by Right Channel Volume Control setting 10: Right Channel Volume is controlled by Left Channel Volume Control setting 11: Reserved. Do not use

6.2.60 Page 0 / Register 65: Left DAC Channel Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Left DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB … 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use

6.2.61 Page 0 / Register 66: Right DAC Channel Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Right DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB … 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use

6.2.62 Page 0 / Register 67: Headset Detection Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset Detection Disabled 1: Headset Detection Enabled
D6–D5	R	00	Headset Type Flag 00: Headset not detected 01: Stereo Headset detected 10: Reserved 11: Stereo + Cellular Headset detected
D4–D2	R/W	000	Headset Detection Debounce Programmability 000: Debounce Time = 16ms 001: Debounce Time = 32ms 010: Debounce Time = 64ms 011: Debounce Time = 128ms 100: Debounce Time = 256ms 101: Debounce Time = 512ms 110-111: Reserved. Do not use Note: All times are typical values
D1–D0	R/W	00	Headset Button Press Debounce Programmability 00: Debounce disabled 01: Debounce Time = 8ms 10: Debounce Time = 16ms 11: Debounce Time = 32ms Note: All times are typical values

6.2.63 Page 0 / Register 68: DRC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R/W	0	DRC Enable Control 0: Left Channel DRC disabled 1: Left Channel DRC enabled
D5	R/W	0	DRC Enable Control 0: Right Channel DRC disabled 1: Right Channel DRC enabled
D4–D2	R/W	011	DRC Threshold control 000: DRC Threshold = -3dBFS 001: DRC Threshold = -6dBFS 010: DRC Threshold = -9dBFS 011: DRC Threshold = -12dBFS 100: DRC Threshold = -15dBFS 101: DRC Threshold = -18dBFS 110: DRC Threshold = -21dBFS 111: DRC Threshold = -24dBFS

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	11	DRC Hysteresis Control 00: DRC Hysteresis = 0dB 01: DRC Hysteresis = 1dB 10: DRC Hysteresis = 2dB 11: DRC Hysteresis = 3dB

6.2.64 Page 0 / Register 69: DRC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6–D3	R/W	0111	DRC Hold Programmability 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks ... 1110: DRC Hold Time = 4*32768 DAC Word Clocks 1111: DRC Hold Time = 5*32768 DAC Word Clocks
D2–D0	R/W	000	Reserved. Write only default values

6.2.65 Page 0 / Register 70: DRC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	DRC Attack Rate control 0000: DRC Attack Rate = 4.0dB per DAC Word Clock 0001: DRC Attack Rate = 2.0dB per DAC Word Clock 0010: DRC Attack Rae = 1.0dB per DAC Word Clock … 1110: DRC Attack Rate = 2.4414e-4dB per DAC Word Clock 1111: DRC Attack Rate = 1.2207e-4dB per DAC Word Clock
D3–D0	R/W	0000	DRC Decay Rate control 0000: DRC Decay Rate = 1.5625e-2dB per DAC Word Clock 0001: DRC Decay Rate = 7.8125e-3dB per DAC Word Clock 0010: DRC Decay Rae = 3.9062e-3dB per DAC Word Clock … 1110: DRC Decay Rate = 9.5367e-7dB per DAC Word Clock 1111: DRC Decay Rate = 4.7683e-7dB per DAC Word Clock

6.2.66 Page 0 / Register 71: Beep Generator Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep Generator Disabled 1: Beep Generator Enabled. This bit will self clear after the beep has been generated.
D6	R	0	Reserved. Write only default value
D5–D0	R/W	00 0000	Left Channel Beep Volume Control 00 0000: Left Channel Beep Volume = 0dB 00 0001: Left Channel Beep Volume = -1dB … 11 1110: Left Channel Beep Volume = -62dB 11 1111: Left Channel Beep Volume = -63dB

6.2.67 Page 0 / Register 72: Beep Generator Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Beep Generator Master Volume Control Setting 00: Left and Right Channels have independent Volume Settings 01: Left Channel Beep Volume is the same as programmed for Right Channel 10: Right Channel Beep Volume is the same as programmed for Left Channel 11: Reserved. Do not use
D5–D0	R	00 0000	Right Channel Beep Volume Control 00 0000: Right Channel Beep Volume = 0dB 00 0001: Right Channel Beep Volume = -1dB … 11 1110: Right Channel Beep Volume = -62dB 11 1111: Right Channel Beep Volume = -63dB

6.2.68 Page 0 / Register 73: Beep Generator Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Programmed value is Beep Sample Length(23:16)

6.2.69 Page 0 / Register 74: Beep Generator Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Programmed value is Beep Sample Length(15:8)

6.2.70 Page 0 / Register 75: Beep Generator Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	Programmed value is Beep Sample Length(7:0)

6.2.71 Page 0 / Register 76: Beep Generator Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0001 0000	Programmed Value is Beep Sin(x)(15:8), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.72 Page 0 / Register 77: Beep Generator Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1101 1000	Programmed Value is Beep Sin(x)(7:0), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.73 Page 0 / Register 78: Beep Generator Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	Programmed Value is Beep Cos(x)(15:8), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.74 Page 0 / Register 79: Beep Generator Register 9

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	Programmed Value is Beep Cos(x)(7:0), where Cos(x) = cos(2*p*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

6.2.75 Page 0 / Register 80: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.76 Page 0 / Register 81: ADC Channel Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Channel ADC Power Control 0: Left Channel ADC is powered down 1: Left Channel ADC is powered up
D6	R/W	0	Right Channel ADC Power Control 0: Right Channel ADC is powered down 1: Right Channel ADC is powered up
D5–D4	R/W	00	Digital Microphone Input Configuration 00: GPIO serves as Digital Microphone Input 01: SCLK serves as Digital Microphone Input 10: DIN serves as Digital Microphone Input 11: Reserved. Do not use
D3	R/W	0	Left Channel Digital Microphone Power Control 0: Left Channel ADC not configured for Digital Microphone 1: Left Channel ADC configured for Digital Microphone
D2	R/W	0	Right Channel Digital Microphone Power Control 0: Right Channel ADC not configured for Digital Microphone 1: Right Channel ADC configured for Digital Microphone
D1–D0	R/W	00	ADC Volume Control Soft-Stepping Control 00: ADC Volume Control changes by 1 gain step per ADC Word Clock 01: ADC Volume Control changes by 1 gain step per two ADC Word Clocks 10: ADC Volume Control Soft-Stepping disabled 11: Reserved. Do not use

6.2.77 Page 0 / Register 82: ADC Fine Gain Adjust Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC Channel Mute Control 0: Left ADC Channel Un-muted 1: Left ADC Channel Muted
D6–D4	R/W	000	Left ADC Channel Fine Gain Adjust 000: Left ADC Channel Fine Gain = 0dB 001: Left ADC Channel Fine Gain = -0.1dB 010: Left ADC Channel Fine Gain = -0.2dB 011: Left ADC Channel Fine Gain = -0.3dB 100: Left ADC Channel Fine Gain = -0.4dB 101-111: Reserved. Do not use
D3	R/W	1	Right ADC Channel Mute Control 0: Right ADC Channel Un-muted 1: Right ADC Channel Muted
D2–D0	R/W	000	Right ADC Channel Fine Gain Adjust 000: Right ADC Channel Fine Gain = 0dB 001: Right ADC Channel Fine Gain = -0.1dB 010: Right ADC Channel Fine Gain = -0.2dB 011: Right ADC Channel Fine Gain = -0.3dB 100: Right ADC Channel Fine Gain = -0.4dB 101-111: Reserved. Do not use

6.2.78 Page 0 / Register 83: Left ADC Channel Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	Left ADC Channel Volume Control 100 0000-110 1000: Reserved. Do not use 110 0111: Left ADC Channel Volume = -12dB 110 0110: Left ADC Channel Volume = -11.5dB 110 0101: Left ADC Channel Volume = -11.0dB … 111 1111: Left ADC Channel Volume = -0.5dB 000 0000: Left ADC Channel Volume = 0.0dB 000 0001: Left ADC Channel Volume = 0.5dB ... 010 0110: Left ADC Channel Volume = 19.0dB 010 0111: Left ADC Channel Volume = 19.5dB 010 1000: Left ADC Channel Volume = 20.0dB 010 1001-011 1111: Reserved. Do not use

6.2.79 Page 0 / Register 84: Right ADC Channel Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6–D0	R/W	000 0000	Right ADC Channel Volume Control 100 0000-110 1000: Reserved. Do not use 110 0111: Right ADC Channel Volume = -12dB 110 0110: Right ADC Channel Volume = -11.5dB 110 0101: Right ADC Channel Volume = -11.0dB … 111 1111: Right ADC Channel Volume = -0.5dB 000 0000: Right ADC Channel Volume = 0.0dB 000 0001: Right ADC Channel Volume = 0.5dB ... 010 0110: Right ADC Channel Volume = 19.0dB 010 0111: Right ADC Channel Volume = 19.5dB 010 1000: Right ADC Channel Volume = 20.0dB 010 1001-011 1111: Reserved. Do not use

6.2.80 Page 0 / Register 85: ADC Phase Adjust Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	ADC Phase Compensation Control 1000 0000-1111 1111: Left ADC Channel Data is delayed with respect to Right ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section. 0000 0000: Left and Right ADC Channel data are not delayed with respect to each other 0000 0001-0111 1111: Right ADC Channel Data is delayed with respect to Left ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section.

6.2.81 Page 0 / Register 86: Left Channel AGC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left Channel AGC Disabled 1: Left Channel AGC Enabled
D6–D4	R/W	000	Left Channel AGC Target Level Setting 000: Left Channel AGC Target Level = -5.5dBFS 001: Left Channel AGC Target Level = -8.0dBFS 010: Left Channel AGC Target Level = -10.0dBFS 011: Left Channel AGC Target Level = -12.0dBFS 100: Left Channel AGC Target Level = -14.0dBFS 101: Left Channel AGC Target Level = -17.0dBFS 110: Left Channel AGC Target Level = -20.0dBFS 111: Left Channel AGC Target Level = -24.0dBFS
D3–D2	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	Left Channel AGC Gain Hysteresis Control 00: Left Channel AGC Gain Hysteresis is disabled 01: Left Channel AGC Gain Hysteresis is 0.5dB 10: Left Channel AGC Gain Hysteresis is 1.0dB 11: Left Channel AGC Gain Hysteresis is 1.5dB

6.2.82 Page 0 / Register 87: Left Channel AGC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left Channel AGC Hysteresis Setting 00: Left Channel AGC Hysteresis is 1.0dB 01: Left Channel AGC Hysteresis is 2.0dB 10: Left Channel AGC Hysteresis is 4.0dB 11: Left Channel AGC Hysteresis is disabled
D5–D1	R/W	0 0000	Left Channel AGC Noise Threshold 0 0000: Left Channel AGC Noise Gate disabled 0 0001: Left Channel AGC Noise Threshold is -30dB 0 0010: Left Channel AGC Noise Threshold is -32dB 0 0011: Left Channel AGC Noise Threshold is -34dB … 1 1101: Left Channel AGC Noise Threshold is -86dB 1 1110: Left Channel AGC Noise Threshold is -88dB 1 1111: Left Channel AGC Noise Threshold is -90dB
D0	R	0	Reserved. Write only default value

6.2.83 Page 0 / Register 88: Left Channel AGC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6–D0	R/W	111 1111	Left Channel AGC Maximum Gain Setting 000 0000: Left Channel AGC Maximum Gain = 0.0dB 000 0001: Left Channel AGC Maximum Gain = 0.5dB 000 0010: Left Channel AGC Maximum Gain = 1.0dB … 111 0011: Left Channel AGC Maximum Gain = 57.5dB 111 0100-111 1111: Left Channel AGC Maximum Gain = 58.0dB

6.2.84 Page 0 / Register 89: Left Channel AGC Control Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0 0000	Left Channel AGC Attack Time Setting 0 0000: Left Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Left Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Left Channel AGC Attack Time = 5*32 ADC Word Clocks … 1 1101: Left Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Left Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Left Channel AGC Attack Time = 63*32 ADC Word Clocks
D2–D0	R/W	000	Left Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.85 Page 0 / Register 90: Left Channel AGC Control Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0 0000	Left Channel AGC Decay Time Setting 0 0000: Left Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Left Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Left Channel AGC Decay Time = 5*512 ADC Word Clocks … 1 1101: Left Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Left Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Left Channel AGC Decay Time = 63*512 ADC Word Clocks
D2–D0	R/W	000	Left Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.86 Page 0 / Register 91: Left Channel AGC Control Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4–D0	R/W	0 0000	Left Channel AGC Noise Debounce Time Setting 0 0001: Left Channel AGC Noise Debounce Time = 0 0 0010: Left Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Left Channel AGC Noise Debounce Time = 8 ADC Word Clocks … 0 1010: Left Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Left Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Left Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Left Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Left Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Left Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Left Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

6.2.87 Page 0 / Register 92: Left Channel AGC Control Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3–D0	R/W	0000	Left Channel AGC Signal Debounce Time Setting 0001: Left Channel AGC Signal Debounce Time = 0 0010: Left Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Left Channel AGC Signal Debounce Time = 8 ADC Word Clocks … 1001: Left Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Left Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Left Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Left Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Left Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Left Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Left Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

6.2.88 Page 0 / Register 93: Left Channel AGC Control Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel AGC Gain Flag 1111 0100: Left Channel AGC Gain = -12.0dB 1111 0101: Left Channel AGC Gain = -11.5dB 1111 0110: Left Channel AGC Gain = -11.0dB … 0000 0000: Left Channel AGC Gain = 0.0dB … 0111 0010: Left Channel AGC Gain = 57.0dB 0111 0011: Left Channel AGC Gain = 57.5dB 0111 0100: Left Channel AGC Gain = 58.0dB

6.2.89 Page 0 / Register 94: Right Channel AGC Control Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right Channel AGC Disabled 1: Right Channel AGC Enabled
D6–D4	R/W	000	Right Channel AGC Target Level Setting 000: Right Channel AGC Target Level = -5.5dBFS 001: Right Channel AGC Target Level = -8.0dBFS 010: Right Channel AGC Target Level = -10.0dBFS 011: Right Channel AGC Target Level = -12.0dBFS 100: Right Channel AGC Target Level = -14.0dBFS 101: Right Channel AGC Target Level = -17.0dBFS 110: Right Channel AGC Target Level = -20.0dBFS 111: Right Channel AGC Target Level = -24.0dBFS
D3–D2	R	00	Reserved. Write only default values
D1–D0	R/W	00	Right Channel AGC Gain Hysteresis Control 00: Right Channel AGC Gain Hysteresis is disabled 01: Right Channel AGC Gain Hysteresis is 0.5dB 10: Right Channel AGC Gain Hysteresis is 1.0dB 11: Right Channel AGC Gain Hysteresis is 1.5dB

6.2.90 Page 0 / Register 95: Right Channel AGC Control Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Right Channel AGC Hysteresis Setting 00: Right Channel AGC Hysteresis is 1.0dB 01: Right Channel AGC Hysteresis is 2.0dB 10: Right Channel AGC Hysteresis is 4.0dB 11: Right Channel AGC Hysteresis is disabled
D5–D1	R/W	0 0000	Right Channel AGC Noise Threshold 0 0000: Right Channel AGC Noise Gate disabled 0 0001: Right Channel AGC Noise Threshold is -30dB 0 0010: Right Channel AGC Noise Threshold is -32dB 0 0011: Right Channel AGC Noise Threshold is -34dB … 1 1101: Right Channel AGC Noise Threshold is -86dB 1 1110: Right Channel AGC Noise Threshold is -88dB 1 1111: Right Channel AGC Noise Threshold is -90dB
D0	R	0	Reserved. Write only default value

6.2.91 Page 0 / Register 96: Right Channel AGC Control Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	111 1111	Right Channel AGC Maximum Gain Setting 000 0000: Right Channel AGC Maximum Gain = 0.0dB 000 0001: Right Channel AGC Maximum Gain = 0.5dB 000 0010: Right Channel AGC Maximum Gain = 1.0dB … 111 0011: Right Channel AGC Maximum Gain = 57.5dB 111 0100-111 1111: Right Channel AGC Maximum Gain = 58.0dB

6.2.92 Page 0 / Register 97: Right Channel AGC Control Register 4

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0 0000	Right Channel AGC Attack Time Setting 0 0000: Right Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Right Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Right Channel AGC Attack Time = 5*32 ADC Word Clocks … 1 1101: Right Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Right Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Right Channel AGC Attack Time = 63*32 ADC Word Clocks
D2–D0	R/W	000	Right Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.93 Page 0 / Register 98: Right Channel AGC Control Register 5

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0 0000	Right Channel AGC Decay Time Setting 0 0000: Right Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Right Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Right Channel AGC Decay Time = 5*512 ADC Word Clocks … 1 1101: Right Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Right Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Right Channel AGC Decay Time = 63*512 ADC Word Clocks
D2–D0	R/W	000	Right Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 … 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

6.2.94 Page 0 / Register 99: Right Channel AGC Control Register 6

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D0	R/W	0 0000	Right Channel AGC Noise Debounce Time Setting 0 0001: Right Channel AGC Noise Debounce Time = 0 0 0010: Right Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Right Channel AGC Noise Debounce Time = 8 ADC Word Clocks … 0 1010: Right Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Right Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Right Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Right Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Right Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Right Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Right Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

6.2.95 Page 0 / Register 100: Right Channel AGC Control Register 7

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3–D0	R/W	0000	Right Channel AGC Signal Debounce Time Setting 0001: Right Channel AGC Signal Debounce Time = 0 0010: Right Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Right Channel AGC Signal Debounce Time = 8 ADC Word Clocks … 1001: Right Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Right Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Right Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Right Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Right Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Right Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Right Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

6.2.96 Page 0 / Register 101: Right Channel AGC Control Register 8

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel AGC Gain Flag 1111 0100: Right Channel AGC Gain = -12.0dB 1111 0101: Right Channel AGC Gain = -11.5dB 1111 0110: Right Channel AGC Gain = -11.0dB … 0000 0000: Right Channel AGC Gain = 0.0dB … 0111 0010: Right Channel AGC Gain = 57.0dB 0111 0011: Right Channel AGC Gain = 57.5dB 0111 0100: Right Channel AGC Gain = 58.0dB

6.2.97 Page 0 / Register 102: DC Measurement Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DC Measurement Mode disabled for Left ADC Channel 1: DC Measurement Mode enabled for Left ADC Channel
D6	R/W	0	0: DC Measurement Mode disabled for Right ADC Channel 1: DC Measurement Mode enabled for Right ADC Channel
D5	R/W	0	0: DC Measurement is done using 1st order moving average filter with averaging of 2^D 1: DC Measurement is done with 1sr order Low-pass IIR filter with coefficients as a function of D

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D0	R/W	0 0000	DC Measurement D setting 0 0000: Reserved. Do not use 0 0001: DC Measurement D parameter = 1 0 0010: DC Measurement D parameter = 2 .. 1 0011: DC Measurement D parameter = 19 1 0100: DC Measurement D parameter = 20 1 0101-1 1111: Reserved. Do not use

6.2.98 Page 0 / Register 103: DC Measurement Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6	R/W	0	0: Left and Right Channel DC measurement result update enabled 1: Left and Right Channel DC measurement result update disabled i.e. new results will be updated while old results are being read
D5	R/W	0	0: For IIR based DC measurement, measurement value is the instantaneous output of IIR filter 1: For IIR based DC measurement, the measurement value is updated before periodic clearing of IIR filter
D4–D0	R/W	0 0000	IIR based DC Measurement, averaging time setting 0 0000: Infinite average is used 0 0001: Averaging time is 2^1 ADC Modulator clocks 0 0010: Averaging time is 2^2 ADC Modulator clocks … 1 0011: Averaging time is 2^19 ADC Modulator clocks 1 0100: Averaging time is 2^20 ADC Modulator clocks 1 0101-1 1111: Reserved. Do not use

6.2.99 Page 0 / Register 104: Left Channel DC Measurement Output Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (23:16)

6.2.100 Page 0 / Register 105: Left Channel DC Measurement Output Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (15:8)

6.2.101 Page 0 / Register 106: Left Channel DC Measurement Output Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Left Channel DC Measurement Output (7:0)

6.2.102 Page 0 / Register 107: Right Channel DC Measurement Output Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (23:16)

6.2.103 Page 0 / Register 108: Right Channel DC Measurement Output Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (15:8)

6.2.104 Page 0 / Register 109: Right Channel DC Measurement Output Register 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Right Channel DC Measurement Output (7:0)

6.2.105 Page 0 / Register 110-127: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.106 Page 1 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.107 Page 1 / Register 1: Power Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3	R/W	0	0: AVDD will be weakly connected to DVDD. Use when DVDD is powered, but AVDD LDO is powered down and AVDD is not externally powered 1: Disabled weak connection of AVDD with DVDD
D2–D0	R	000	Reserved. Write only default values

6.2.108 Page 1 / Register 2: LDO Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	DVDD LDO Control 00: DVDD LDO output is nominally 1.72V 01: DVDD LDO output is nominally 1.67V 10: DVDD LDO output is nominally 1.77V 11: Do not use
D5–D4	R/W	00	AVDD LDO Control 00: AVDD LDO output is nominally 1.72V 01: AVDD LDO output is nominally 1.67V 10: AVDD LDO output is nominally 1.77V 11: Do not use
D3	R/W	1	Analog Block Power Control 0: Analog Blocks Enabled 1: Analog Blocks Disabled
D2	R	0	DVDD LDO Over Current Detect 0: Over Current not detected for DVDD LDO 1: Over Current detected for DVDD LDO
D1	R	0	AVDD LDO Over Current Detect 0: Over Current not detected for AVDD LDO 1: Over Current detected for AVDD LDO
D0	R/W	0	AVDD LDO Power Control 0: AVDD LDO Powered down 1: AVDD LDO Powered up

6.2.109 Page 1 / Register 3: Playback Configuration Register 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Left DAC routing to HPL uses Class-AB driver 01-10: Reserved. Do not use 11: Left DAC routing to HPL uses Class-D driver
D5	R	0	Reserved. Write only default value
D4–D2	R/W	000	Left DAC PTM Control 000: Left DAC in mode PTM_P3, PTM_P4 001: Left DAC in mode PTM_P2 010: Left DAC in mode PTM_P1 011-111: Reserved. Do not use
D1–D0	R	00	Reserved. Write only default value

6.2.110 Page 1 / Register 4: Playback Configuration Register 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Right DAC routing to HPL uses Class-AB driver 01-10: Reserved. Do not use 11: Right DAC routing to HPL uses Class-D driver
D5	R	0	Reserved. Write only default value
D4–D2	R/W	000	Right DAC PTM Control 000: Right DAC in mode PTM_P3, PTM_P4 001: Right DAC in mode PTM_P2 010: Right DAC in mode PTM_P1 011-111: Reserved. Do not use
D1–D0	R	00	Reserved. Write only default value

6.2.111 Page 1 / Register 5-8: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.112 Page 1 / Register 9: Output Driver Power Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default value
D5	R/W	0	0: HPL is powered down 1: HPL is powered up
D4	R/W	0	0: HPR is powered down 1: HPR is powered up
D3	R/W	0	0: LOL is powered down 1: LOL is powered up
D2	R/W	0	0: LOR is powered down 1: LOR is powered up
D1	R/W	0	0: Left Mixer Amplifier(MAL) is powered down 1: Left Mixer Amplifier(MAL) is powered up
D0	R/W	0	0: Right Mixer Amplifier(MAR) is powered down 1: Right Mixer Amplifier(MAR) is powered up

6.2.113 Page 1 / Register 10: Common Mode Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	0	0: Full Chip Common Mode is 0.9V 1: Full Chip Common Mode is 0.75V

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D4	R/W	00	00: Output Common Mode for HPL & HPR is same as full-chip common mode 01: Output Common Mode for HPL & HPR is 1.25V 10: Output Common Mode for HPL & HPR is 1.5V 11: Output Common Mode for HPL & HPR is 1.65V
D3	R/W	0	0: Output Common Mode for LOL & LOR is same as full-chip common mode 1: Output Common Mode for LOL & LOR is 1.65V and output is powered by LDOIN
D2	R	0	Reserved. Write only default value
D1	R/W	0	0: Output of HPL & HPR is powered with AVDD supply 1: Output of HPL & HPR is powered with LDOIN supply
D0	R/W	0	0: When Page-1, Reg-10, D1=1, then LDOIN input range is 1.5V to 1.95V 1: When Page-1, Reg-10, D1=1, then LDOIN input range is 1.8V to 3.6V

6.2.114 Page 1 / Register 11: Over Current Protection Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	1	0: Over Current detection is disabled for HPL & HPR 1: Over Current detection is enabled for HPL & HPR
D3–D1	R/W	000	000: No debounce is used for Over Current detection 001: Over Current detection is debounced by 8ms 010: Over Current detection is debounce by 16ms 011: Over Current detection is debounced by 32ms 100: Over Current detection is debounced by 64ms 101: Over Current detection is debounced by 128ms 110: Over Current detection is debounced by 256ms 111: Over Current detection is debounced by 512ms
D0	R/W	0	0: Output current will be limited if over current condition is detected 1: Output driver will be powered down if over current condition is detected

6.2.115 Page 1 / Register 12: HPL Routing Selection Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3	R/W	0	0: Left Channel DAC reconstruction filter's positive terminal is not routed to HPL 1: Left Channel DAC reconstruction filter's positive terminal is routed to HPL
D2	R/W	0	0: IN1L is not routed to HPL 1: IN1L is routed to HPL
D1	R/W	0	0: MAL output is not routed to HPL 1: MAL output is routed to HPL
D0	R/W	0	0: MAR output is not routed to HPL 1: MAR output is routed to HPL

6.2.116 Page 1 / Register 13: HPR Routing Selection Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	0	0: Left Channel DAC reconstruction filter's negative terminal is not routed to HPR 1: Left Channel DAC reconstruction filter's negative terminal is routed to HPR
D3	R/W	0	0: Right Channel DAC reconstruction filter's positive terminal is not routed to HPR 1: Right Channel DAC reconstruction filter's positive terminal is routed to HPR
D2	R/W	0	0: IN1R is not routed to HPR 1: IN1R is routed to HPR
D1	R/W	0	0: MAR output is not routed to HPR 1: MAR output is routed to HPR

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	0: HPL output is not routed to HPR 1: HPL output is routed to HPR (use when HPL&HPR output is powered by AVDD)

6.2.117 Page 1 / Register 14: LOL Routing Selection Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R	000	Reserved. Write only default values
D4	R/W	0	0: Right Channel DAC reconstruction filter's negative terminal is not routed to LOL 1: Right Channel DAC reconstruction filter's negative terminal is routed to LOL
D3	R/W	0	0: Left Channel DAC reconstruction filter output is not routed to LOL 1: Left Channel DAC reconstruction filter output is routed to LOL
D2	R	0	Reserved. Write only default value.
D1	R/W	0	0: MAL output is not routed to LOL 1: MAL output is routed to LOL
D0	R/W	0	0: LOR output is not routed to LOL 1: LOR output is routed to LOL(use when LOL&LOR output is powered by AVDD)

6.2.118 Page 1 / Register 15: LOR Routing Selection Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R	0000	Reserved. Write only default values
D3	R/W	0	0: Right Channel DAC reconstruction filter output is not routed to LOR 1: Right Channel DAC reconstruction filter output is routed to LOR
D2	R	0	Reserved. Write only default value.
D1	R/W	0	0: MAR output is not routed to LOR 1: MAR output is routed to LOR
D0	R	0	Reserved. Write only default value.

6.2.119 Page 1 / Register 16: HPL Driver Gain Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: HPL driver is not muted 1: HPL driver is muted
D5–D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: HPL driver gain is -6dB (Note: It is not possible to mute HPL while programmed to -6dB) 11 1011: HPL driver gain is -5dB 11 1100: HPL driver gain is -4dB … 00 0000: HPL driver gain is 0dB ... 01 1011: HPL driver gain is 27dB 01 1100: HPL driver gain is 28dB 01 1101: HPL driver gain is 29dB 01 1110-01 1111: Reserved. Do not use Note: These gains are not valid while using the driver in Class-D mode

6.2.120 Page 1 / Register 17: HPR Driver Gain Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: HPR driver is not muted 1: HPR driver is muted

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: HPR driver gain is -6dB (Note: It is not possible to mute HPR while programmed to -6dB) 11 1011: HPR driver gain is -5dB 11 1100: HPR driver gain is -4dB … 00 0000: HPR driver gain is 0dB ... 01 1011: HPR driver gain is 27dB 01 1100: HPR driver gain is 28dB 01 1101: HPR driver gain is 29dB 01 1110-01 1111: Reserved. Do not use Note: These gains are not valid while using the driver in Class-D mode

6.2.121 Page 1 / Register 18: LOL Driver Gain Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: LOL driver is not muted 1: LOL driver is muted
D5–D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: LOL driver gain is -6dB 11 1011: LOL driver gain is -5dB 11 1100: LOL driver gain is -4dB … 00 0000: LOL driver gain is 0dB ... 01 1011: LOL driver gain is 27dB 01 1100: LOL driver gain is 28dB 01 1101: LOL driver gain is 29dB 01 1110-01 1111: Reserved. Do not use

6.2.122 Page 1 / Register 19: LOR Driver Gain Setting Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: LOR driver is not muted 1: LOR driver is muted
D5–D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: LOR driver gain is -6dB 11 1011: LOR driver gain is -5dB 11 1100: LOR driver gain is -4dB … 00 0000: LOR driver gain is 0dB ... 01 1011: LOR driver gain is 27dB 01 1100: LOR driver gain is 28dB 01 1101: LOR driver gain is 29dB 01 1110-01 1111: Reserved. Do not use

6.2.123 Page 1 / Register 20: Headphone Driver Startup Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Soft routing step time is 0ms 01: Soft routing step time is 50ms 10: Soft routing step time is 100ms 11: Soft routing step time is 200ms

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D2	R/W	0000	0000: Slow power up of headphone amp's is disabled 0001: Headphone amps power up slowly in 0.5 time constants 0010: Headphone amps power up slowly in 0.625 time constants 0011; Headphone amps power up slowly in 0.725 time constants 0100: Headphone amps power up slowly in 0.875 time constants 0101: Headphone amps power up slowly in 1.0 time constants 0110: Headphone amps power up slowly in 2.0 time constants 0111: Headphone amps power up slowly in 3.0 time constants 1000: Headphone amps power up slowly in 4.0 time constants 1001: Headphone amps power up slowly in 5.0 time constants 1010: Headphone amps power up slowly in 6.0 time constants 1011: Headphone amps power up slowly in 7.0 time constants 1100: Headphone amps power up slowly in 8.0 time constants 1101: Headphone amps power up slowly in 16.0 time constants (do not use for Rchg=25K) 1110: Headphone amps power up slowly in 24.0 time constants (do not use for Rchg=25K) 1111: Headphone amps power up slowly in 32.0 time constants (do not use for Rchg=25K) Note: Time constants assume 47uF decoupling cap
D1–D0	R/W	00	00: Headphone amps power up time is determined with 25K resistance 01: Headphone amps power up time is determined with 6K resistance 10: Headphone amps power up time is determined with 2K resistance 11: Reserved. Do not use

6.2.124 Page 1 / Register 21: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.125 Page 1 / Register 22: IN1L to HPL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	IN1L to HPL Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = -0.5dB 000 0010: Volume Control = -1.0dB 000 0011: Volume Control = -1.5dB 000 0100: Volume Control = -2.0dB 000 0101: Volume Control = -2.5dB 000 0110: Volume Control = -3.0dB 000 0111: Volume Control = -3.5dB 000 1000: Volume Control = -4.0dB 000 1001: Volume Control = -4.5dB 000 1010: Volume Control = -5.0dB 000 1011: Volume Control = -5.5dB 000 1100: Volume Control = -6.0dB 000 1101: Volume Control = -7.0dB 000 1110: Volume Control = -8.0dB 000 1111: Volume Control = -8.5dB 001 0000: Volume Control = -9.0dB 001 0001: Volume Control = -9.5dB 001 0010: Volume Control = -10.0dB 001 0011: Volume Control = -10.5dB 001 0100: Volume Control = -11.0dB 001 0101: Volume Control = -11.5dB 001 0110: Volume Control = -12.0dB 001 0111: Volume Control = -12.5dB 001 1000: Volume Control = -13.0dB 001 1001: Volume Control = -13.5dB 001 1010: Volume Control = -14.0dB 001 1011: Volume Control = -14.5dB 001 1100: Volume Control = -15.0dB 001 1101: Volume Control = -15.5dB 001 1110: Volume Control = -16.0dB 001 1111: Volume Control = -16.5dB 010 0000: Volume Control = -17.1dB 010 0001: Volume Control = -17.5dB 010 0010: Volume Control = -18.1dB 010 0011: Volume Control = -18.6dB 010 0100: Volume Control = -19.1dB 010 0101: Volume Control = -19.6dB 010 0110: Volume Control = -20.1dB 010 0111: Volume Control = -20.6dB 010 1000: Volume Control = -21.1dB 010 1001: Volume Control = -21.6dB 010 1010: Volume Control = -22.1dB 010 1011: Volume Control = -22.6dB 010 1100: Volume Control = -23.1dB 010 1101: Volume Control = -23.6dB 010 1110: Volume Control = -24.1dB 010 1111: Volume Control = -24.6dB 011 0000: Volume Control = -25.1dB 011 0001: Volume Control = -25.6dB 011 0010: Volume Control = -26.1dB 011 0011: Volume Control = -26.6dB 011 0100: Volume Control = -27.1dB 011 0101: Volume Control = -27.6dB 011 0110: Volume Control = -28.1dB 011 0111: Volume Control = -28.6dB 011 1000: Volume Control = -29.1dB 011 1001: Volume Control = -29.6dB 011 1010: Volume Control = -30.1dB 011 1011: Volume Control = -30.6dB 011 1100: Volume Control = -31.1dB 011 1100: Volume Control = -31.6dB 011 1101: Volume Control = -32.1dB 011 1110: Volume Control = -32.6dB 011 1111: Volume Control = -33.1dB 100 0000: Volume Control = -33.6dB 100 0001: Volume Control = -34.1dB

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -34.6dB 100 0011: Volume Control = -35.2dB 100 0100: Volume Control = -35.7dB 100 0101: Volume Control = -36.2dB 100 0110: Volume Control = -36.7dB 100 0111: Volume Control = -37.2dB 100 1000: Volume Control = -37.7dB 100 1001: Volume Control = -38.2dB 100 1010: Volume Control = -38.7dB 100 1011: Volume Control = -39.2dB 100 1100: Volume Control = -39.7dB 100 1101: Volume Control = -40.2dB 100 1110: Volume Control = -40.7dB 100 1111: Volume Control = -41.2dB 101 0000: Volume Control = -41.7dB 101 0001: Volume Control = -42.1dB 101 0010: Volume Control = -42.7dB 101 0011: Volume Control = -43.2dB 101 0100: Volume Control = -43.8dB 101 0101: Volume Control = -44.3dB 101 0110: Volume Control = -44.8dB 101 0111: Volume Control = -45.2dB 101 1000: Volume Control = -45.8dB 101 1001: Volume Control = -46.2dB 101 1010: Volume Control = -46.7dB 101 1011: Volume Control = -47.4dB 101 1100: Volume Control = -47.9dB 101 1101: Volume Control = -48.2dB 101 1110: Volume Control = -48.7dB 101 1111: Volume Control = -49.3dB 110 0000: Volume Control = -50.0dB 110 0001: Volume Control = -50.3dB 110 0010: Volume Control = -51.0dB 110 0011: Volume Control = -51.42dB 110 0100: Volume Control = -51.82dB 110 0101: Volume Control = -52.3dB 110 0110: Volume Control = -52.7dB 110 0111: Volume Control = -53.7dB 110 1000: Volume Control = -54.2dB 110 1001: Volume Control = -55.4dB 110 1010: Volume Control = -56.7dB 110 1011: Volume Control = -58.3dB 110 1100: Volume Control = -60.2dB 110 1101: Volume Control = -62.7dB 110 1110: Volume Control = -64.3dB 110 1111: Volume Control = -66.2dB 111 0000: Volume Control = -68.7dB 111 0001: Volume Control = -72.3dB 111 0010: Volume Control = MUTE 111 0011-111 1111: Reserved. Do not use

6.2.126 Page 1 / Register 23: IN1R to HPR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0000	IN1R to HPR Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = -0.5dB 000 0010: Volume Control = -1.0dB 000 0011: Volume Control = -1.5dB 000 0100: Volume Control = -2.0dB 000 0101: Volume Control = -2.5dB 000 0110: Volume Control = -3.0dB 000 0111: Volume Control = -3.5dB 000 1000: Volume Control = -4.0dB 000 1001: Volume Control = -4.5dB 000 1010: Volume Control = -5.0dB 000 1011: Volume Control = -5.5dB 000 1100: Volume Control = -6.0dB 000 1101: Volume Control = -7.0dB 000 1110: Volume Control = -8.0dB 000 1111: Volume Control = -8.5dB 001 0000: Volume Control = -9.0dB 001 0001: Volume Control = -9.5dB 001 0010: Volume Control = -10.0dB 001 0011: Volume Control = -10.5dB 001 0100: Volume Control = -11.0dB 001 0101: Volume Control = -11.5dB 001 0110: Volume Control = -12.0dB 001 0111: Volume Control = -12.5dB 001 1000: Volume Control = -13.0dB 001 1001: Volume Control = -13.5dB 001 1010: Volume Control = -14.0dB 001 1011: Volume Control = -14.5dB 001 1100: Volume Control = -15.0dB 001 1101: Volume Control = -15.5dB 001 1110: Volume Control = -16.0dB 001 1111: Volume Control = -16.5dB 010 0000: Volume Control = -17.1dB 010 0001: Volume Control = -17.5dB 010 0010: Volume Control = -18.1dB 010 0011: Volume Control = -18.6dB 010 0100: Volume Control = -19.1dB 010 0101: Volume Control = -19.6dB 010 0110: Volume Control = -20.1dB 010 0111: Volume Control = -20.6dB 010 1000: Volume Control = -21.1dB 010 1001: Volume Control = -21.6dB 010 1010: Volume Control = -22.1dB 010 1011: Volume Control = -22.6dB 010 1100: Volume Control = -23.1dB 010 1101: Volume Control = -23.6dB 010 1110: Volume Control = -24.1dB 010 1111: Volume Control = -24.6dB 011 0000: Volume Control = -25.1dB 011 0001: Volume Control = -25.6dB 011 0010: Volume Control = -26.1dB 011 0011: Volume Control = -26.6dB 011 0100: Volume Control = -27.1dB 011 0101: Volume Control = -27.6dB 011 0110: Volume Control = -28.1dB 011 0111: Volume Control = -28.6dB 011 1000: Volume Control = -29.1dB 011 1001: Volume Control = -29.6dB 011 1010: Volume Control = -30.1dB 011 1011: Volume Control = -30.6dB 011 1100: Volume Control = -31.1dB 011 1100: Volume Control = -31.6dB 011 1101: Volume Control = -32.1dB 011 1110: Volume Control = -32.6dB 011 1111: Volume Control = -33.1dB 100 0000: Volume Control = -33.6dB 100 0001: Volume Control = -34.1dB

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -34.6dB 100 0011: Volume Control = -35.2dB 100 0100: Volume Control = -35.7dB 100 0101: Volume Control = -36.2dB 100 0110: Volume Control = -36.7dB 100 0111: Volume Control = -37.2dB 100 1000: Volume Control = -37.7dB 100 1001: Volume Control = -38.2dB 100 1010: Volume Control = -38.7dB 100 1011: Volume Control = -39.2dB 100 1100: Volume Control = -39.7dB 100 1101: Volume Control = -40.2dB 100 1110: Volume Control = -40.7dB 100 1111: Volume Control = -41.2dB 101 0000: Volume Control = -41.7dB 101 0001: Volume Control = -42.1dB 101 0010: Volume Control = -42.7dB 101 0011: Volume Control = -43.2dB 101 0100: Volume Control = -43.8dB 101 0101: Volume Control = -44.3dB 101 0110: Volume Control = -44.8dB 101 0111: Volume Control = -45.2dB 101 1000: Volume Control = -45.8dB 101 1001: Volume Control = -46.2dB 101 1010: Volume Control = -46.7dB 101 1011: Volume Control = -47.4dB 101 1100: Volume Control = -47.9dB 101 1101: Volume Control = -48.2dB 101 1110: Volume Control = -48.7dB 101 1111: Volume Control = -49.3dB 110 0000: Volume Control = -50.0dB 110 0001: Volume Control = -50.3dB 110 0010: Volume Control = -51.0dB 110 0011: Volume Control = -51.42dB 110 0100: Volume Control = -51.82dB 110 0101: Volume Control = -52.3dB 110 0110: Volume Control = -52.7dB 110 0111: Volume Control = -53.7dB 110 1000: Volume Control = -54.2dB 110 1001: Volume Control = -55.4dB 110 1010: Volume Control = -56.7dB 110 1011: Volume Control = -58.3dB 110 1100: Volume Control = -60.2dB 110 1101: Volume Control = -62.7dB 110 1110: Volume Control = -64.3dB 110 1111: Volume Control = -66.2dB 111 0000: Volume Control = -68.7dB 111 0001: Volume Control = -72.3dB 111 0010: Volume Control = MUTE 111 0011-111 1111: Reserved. Do not use

6.2.127 Page 1 / Register 24: MAL Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D0	R/W	00 0000	MAL Volume Control 00 0000: Volume Control = 0.0dB 00 0001: Volume Control = -0.4dB 00 0010: Volume Control = -0.9dB 00 0011: Volume Control = -1.3dB 00 0100: Volume Control = -1.8dB 00 0101: Volume Control = -2.3dB 00 0110: Volume Control = -2.9dB 00 0111: Volume Control = -3.3dB 00 1000: Volume Control = -3.9dB 00 1001: Volume Control = -4.3dB 00 1010: Volume Control = -4.8dB 00 1011: Volume Control = -5.2dB 00 1100: Volume Control = -5.8dB 00 1101: Volume Control = -6.3dB 00 1110: Volume Control = -6.6dB 00 1111: Volume Control = -7.2dB 01 0000: Volume Control = -7.8dB 01 0001: Volume Control = -8.2dB 01 0010: Volume Control = -8.5dB 01 0011: Volume Control = -9.3dB 01 0100: Volume Control = -9.7dB 01 0101: Volume Control = -10.1dB 01 0110: Volume Control = -10.6dB 01 0111: Volume Control = -11.0dB 01 1000: Volume Control = -11.5dB 01 1001: Volume Control = -12.0dB 01 1010: Volume Control = -12.6dB 01 1011: Volume Control = -13.2dB 01 1100: Volume Control = -13.8dB 01 1101: Volume Control = -14.5dB 01 1110: Volume Control = -15.3dB 01 1111: Volume Control = -16.1dB 10 0000: Volume Control = -17.0dB 10 0001: Volume Control = -18.1dB 10 0010: Volume Control = -19.2dB 10 0011: Volume Control = -20.6dB 10 0100: Volume Control = -22.1dB 10 0101: Volume Control = -24.1dB 10 0110: Volume Control = -26.6dB 10 0111: Volume Control = -30.1dB 10 1000: Volume Control = MUTE 10 1001-11 1111: Reserved. Do no use

6.2.128 Page 1 / Register 25: MAR Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D0	R/W	00 0000	MAR Volume Control 00 0000: Volume Control = 0.0dB 00 0001: Volume Control = -0.4dB 00 0010: Volume Control = -0.9dB 00 0011: Volume Control = -1.3dB 00 0100: Volume Control = -1.8dB 00 0101: Volume Control = -2.3dB 00 0110: Volume Control = -2.9dB 00 0111: Volume Control = -3.3dB 00 1000: Volume Control = -3.9dB 00 1001: Volume Control = -4.3dB 00 1010: Volume Control = -4.8dB 00 1011: Volume Control = -5.2dB 00 1100: Volume Control = -5.8dB 00 1101: Volume Control = -6.3dB 00 1110: Volume Control = -6.6dB 00 1111: Volume Control = -7.2dB 01 0000: Volume Control = -7.8dB 01 0001: Volume Control = -8.2dB 01 0010: Volume Control = -8.5dB 01 0011: Volume Control = -9.3dB 01 0100: Volume Control = -9.7dB 01 0101: Volume Control = -10.1dB 01 0110: Volume Control = -10.6dB 01 0111: Volume Control = -11.0dB 01 1000: Volume Control = -11.5dB 01 1001: Volume Control = -12.0dB 01 1010: Volume Control = -12.6dB 01 1011: Volume Control = -13.2dB 01 1100: Volume Control = -13.8dB 01 1101: Volume Control = -14.5dB 01 1110: Volume Control = -15.3dB 01 1111: Volume Control = -16.1dB 10 0000: Volume Control = -17.0dB 10 0001: Volume Control = -18.1dB 10 0010: Volume Control = -19.2dB 10 0011: Volume Control = -20.6dB 10 0100: Volume Control = -22.1dB 10 0101: Volume Control = -24.1dB 10 0110: Volume Control = -26.6dB 10 0111: Volume Control = -30.1dB 10 1000: Volume Control = MUTE 10 1001-11 1111: Reserved. Do no use

6.2.129 Page 1 / Register 26-50: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.130 Page 1 / Register 51: MICBIAS Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	0	0: MICBIAS powered down 1: MICBIAS powered up
D5–D4	R/W	00	MICBIAS Output Voltage Configuration 00: MICBIAS = 1.04V (CM=0.75V) or MICBIAS = 1.25V(CM=0.9V) 01: MICBIAS = 1.425V(CM=0.75V) or MICBIAS = 1.7V(CM=0.9V) 10: MICBIAS = 2.075V(CM=0.75V) or MICBIAS = 2.5V(CM=0.9V) 11: MICBIAS is switch to power supply
D3	R/W	0	0: MICBIAS voltage is generated from AVDD 1: MICBIAS voltage is generated from LDOIN

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2–D0	R	000	Reserved. Write only default value.

6.2.131 Page 1 / Register 52: Left MICPGA Positive Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	IN1L to Left MICPGA positive terminal selection 00: IN1L is not routed to Left MICPGA 01: IN1L is routed to Left MICPGA with 10K resistance 10: IN1L is routed to Left MICPGA with 20K resistance 11: IN1L is routed to Left MICPGA with 40K resistance
D5–D4	R/W	00	IN2L to Left MICPGA positive terminal selection 00: IN2L is not routed to Left MICPGA 01: IN2L is routed to Left MICPGA with 10K resistance 10: IN2L is routed to Left MICPGA with 20K resistance 11: IN2L is routed to Left MICPGA with 40K resistance
D3–D2	R/W	00	IN3L to Left MICPGA positive terminal selection 00: IN3L is not routed to Left MICPGA 01: IN3L is routed to Left MICPGA with 10K resistance 10: IN3L is routed to Left MICPGA with 20K resistance 11: IN3L is routed to Left MICPGA with 40K resistance
D1–D0	R/W	00	IN1R to Left MICPGA positive terminal selection 00: IN1R is not routed to Left MICPGA 01: IN1R is routed to Left MICPGA with 10K resistance 10: IN1R is routed to Left MICPGA with 20K resistance 11: IN1R is routed to Left MICPGA with 40K resistance

6.2.132 Page 1 / Register 53: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.133 Page 1 / Register 54: Left MICPGA Negative Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CM to Left MICPGA (CM1L) positive terminal selection 00: CM is not routed to Left MICPGA 01: CM is routed to Left MICPGA via CM1L with 10K resistance 10: CM is routed to Left MICPGA via CM1L with 20K resistance 11: CM is routed to Left MICPGA via CM1L with 40K resistance
D5–D4	R/W	00	IN2R to Left MICPGA positive terminal selection 00: IN2R is not routed to Left MICPGA 01: IN2R is routed to Left MICPGA with 10K resistance 10: IN2R is routed to Left MICPGA with 20K resistance 11: IN2R is routed to Left MICPGA with 40K resistance
D3–D2	R/W	00	IN3R to Left MICPGA positive terminal selection 00: IN3R is not routed to Left MICPGA 01: IN3R is routed to Left MICPGA with 10K resistance 10: IN3R is routed to Left MICPGA with 20K resistance 11: IN3R is routed to Left MICPGA with 40K resistance
D1–D0	R/W	00	CM to Left MICPGA (CM2L) positive terminal selection 00: CM is not routed to Left MICPGA 01: CM is routed to Left MICPGA via CM2L with 10K resistance 10: CM is routed to Left MICPGA via CM2L with 20K resistance 11: CM is routed to Left MICPGA via CM2L with 40K resistance

6.2.134 Page 1 / Register 55: Right MICPGA Positive Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	IN1R to Right MICPGA positive terminal selection 00: IN1R is not routed to Right MICPGA 01: IN1R is routed to Right MICPGA with 10K resistance 10: IN1R is routed to Right MICPGA with 20K resistance 11: IN1R is routed to Right MICPGA with 40K resistance
D5–D4	R/W	00	IN2R to Right MICPGA positive terminal selection 00: IN2R is not routed to Right MICPGA 01: IN2R is routed to Right MICPGA with 10K resistance 10: IN2R is routed to Right MICPGA with 20K resistance 11: IN2R is routed to Right MICPGA with 40K resistance
D3–D2	R/W	00	IN3R to Right MICPGA positive terminal selection 00: IN3R is not routed to Right MICPGA 01: IN3R is routed to Right MICPGA with 10K resistance 10: IN3R is routed to Right MICPGA with 20K resistance 11: IN3R is routed to Right MICPGA with 40K resistance
D1–D0	R/W	00	IN2L to Right MICPGA positive terminal selection 00: IN2L is not routed to Right MICPGA 01: IN2L is routed to Right MICPGA with 10K resistance 10: IN2L is routed to Right MICPGA with 20K resistance 11: IN2L is routed to Right MICPGA with 40K resistance

6.2.135 Page 1 / Register 56: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.136 Page 1 / Register 57: Right MICPGA Negative Terminal Input Routing Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	CM to Right MICPGA (CM1R) positive terminal selection 00: CM is not routed to Right MICPGA 01: CM is routed to Right MICPGA via CM1R with 10K resistance 10: CM is routed to Right MICPGA via CM1R with 20K resistance 11: CM is routed to Right MICPGA via CM1R with 40K resistance
D5–D4	R/W	00	IN1L to Right MICPGA positive terminal selection 00: IN1L is not routed to Right MICPGA 01: IN1L is routed to Right MICPGA with 10K resistance 10: IN1L is routed to Right MICPGA with 20K resistance 11: IN1L is routed to Right MICPGA with 40K resistance
D3–D2	R/W	00	IN3L to Right MICPGA positive terminal selection 00: IN3L is not routed to Right MICPGA 01: IN3L is routed to Right MICPGA with 10K resistance 10: IN3L is routed to Right MICPGA with 20K resistance 11: IN3L is routed to Right MICPGA with 40K resistance
D1–D0	R/W	00	CM to Right MICPGA (CM2R) positive terminal selection 00: CM is not routed to Right MICPGA 01: CM is routed to Right MICPGA via CM2R with 10K resistance 10: CM is routed to Right MICPGA via CM2R with 20K resistance 11: CM is routed to Right MICPGA via CM2R with 40K resistance

6.2.137 Page 1 / Register 58: Floating Input Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: IN1L input is not weakly connected to common mode 1: IN1L input is weakly driven to common mode. Use when not routing IN1L to Left and Right MICPGA and HPL

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6	R/W	0	0: IN1R input is not weakly connected to common mode 1: IN1R input is weakly driven to common mode. Use when not routing IN1L to Left and Right MICPGA and HPR
D5	R/W	0	0: IN2L input is not weakly connected to common mode 1: IN2L input is weakly driven to common mode. Use when not routing IN2L to Left and Right MICPGA
D4	R/W	0	0: IN2R input is not weakly connected to common mode 1: IN2R input is weakly driven to common mode. Use when not routing IN2R to Left and Right MICPGA
D3	R/W	0	0: IN3L input is not weakly connected to common mode 1: IN3L input is weakly driven to common mode. Use when not routing IN3L to Left and Right MICPGA
D2	R/W	0	0: IN3R input is not weakly connected to common mode 1: IN3R input is weakly driven to common mode. Use when not routing IN3R to Left and Right MICPGA
D1–D0	R	00	Reserved. Write only default values

6.2.138 Page 1 / Register 59: Left MICPGA Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Left MICPGA Gain is enabled 1: Left MICPGA Gain is set to 0dB
D6–D0	R/W	000 0000	Left MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB … 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use

6.2.139 Page 1 / Register 60: Right MICPGA Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right MICPGA Gain is enabled 1: Right MICPGA Gain is set to 0dB
D6–D0	R/W	000 0000	Right MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB … 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use

6.2.140 Page 1 / Register 61: ADC Power Tune Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: PTM_R4 (Default) 0110 0100: PTM_R3 1011 0110: PTM_R2 1111 1111: PTM_R1

6.2.141 Page 1 / Register 62: ADC Analog Volume Control Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R	00 0000	Reserved. Write only default values
D1	R	0	Left Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D0	R	0	Right Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume

6.2.142 Page 1 / Register 63: DAC Analog Gain Control Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	HPR Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	LOL Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	LOR Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3	R	0	IN1L to HPL Bypass Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D2	R	0	IN1R to HPR Bypass Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D1	R	0	MAL Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D0	R	0	MAR Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume

6.2.143 Page 1 / Register 64-70: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.144 Page 1 / Register 71: Analog Input Quick Charging Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R	00	Reserved. Write only default values
D5–D0	R/W	00 0000	Analog inputs power up time 00 0000: Default. Use one of the values give below 11 0001: Analog inputs power up time is 3.1 ms 11 0010: Analog inputs power up time is 6.4 ms 11 0011: Analog inputs power up time is 1.6 ms Others: Do not use

6.2.145 Page 1 / Register 72-122: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.146 Page 1 / Register 123: Reference Power-up Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0 0000	Reserved. Write only default values
D2–D0	R/W	000	Reference Power Up configuration 000: Reference will power up slowly when analog blocks are powered up 001: Reference will power up in 40ms when analog blocks are powered up 010: Reference will power up in 80ms when analog blocks are powered up 011: Reference will power up in 120ms when analog blocks are powered up 100: Force power up of reference. Power up will be slow 101: Force power up of reference. Power up time will be 40ms 110: Force power up of reference. Power up time will be 80ms 111: Force power up of reference. Power up time will be 120ms

6.2.147 Page 1 / Register 124-127: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.148 Page 8 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.149 Page 8 / Register 1: ADC Adaptive Filter Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved. Write only default values
D2	R/W	0	ADC Adaptive Filtering Control 0: Adaptive Filtering disabled for ADC 1: Adaptive Filtering enabled for ADC
D1	R	0	ADC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-A and control interface accesses ADC Coefficient Buffer-B 1: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-B and control interface accesses ADC Coefficient Buffer-A
D0	R/W	0	ADC Adaptive Filter Buffer Switch control 0: ADC Coefficient Buffers will not be switched at next frame boundary 1: ADC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

6.2.150 Page 8 / Register 1-7: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.151 Page 8 / Register 8-127: ADC Coefficients Buffer-A C(0:29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients C0 through C29 of ADC Coefficient Buffer-A. Refer Table ?? for details When Page-8, Reg-01d, D2='0' the read write access to these registers is allowed only when ADC channel is powered down

6.2.152 Page 9-16 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.153 Page 9-16 / Register 1-7: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.154 Page 9-16 / Register 8-127: ADC Coefficients Buffer-A C(30:255)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients ADC Coefficient Buffer-A. Refer Table ?? for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

6.2.155 Page 26-34 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.156 Page 26-34 / Register 1-7: Reserved.

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.157 Page 26-34 / Register 8-127: ADC Coefficients Buffer-B C(0:255)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficient Buffer-B. Refer Table ?? for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

6.2.158 Page 44 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.159 Page 44 / Register 1: DAC Adaptive Filter Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R	0000 0	Reserved. Write only default values
D2	R/W	0	DAC Adaptive Filtering Control 0: Adaptive Filtering disabled for DAC 1: Adaptive Filtering enabled for DAC
D1	R	0	DAC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC accesses DAC Coefficient Buffer-A and control interface accesses DAC Coefficient Buffer-B 1: In adaptive filter mode, DAC accesses DAC Coefficient Buffer-B and control interface accesses DAC Coefficient Buffer-A

(continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	DAC Adaptive Filter Buffer Switch control 0: DAC Coefficient Buffers will not be switched at next frame boundary 1: DAC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

6.2.160 Page 44 / Register 1-7: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.161 Page 44 / Register 8-127: DAC Coefficients Buffer-A C(0:29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients C0 through C29 of DAC Coefficient Buffer-A. Refer Table ?? for details When Page-44, Reg-01d, D2='0' the read write access to these registers is allowed only when DAC channel is powered down

6.2.162 Page 45-52 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.163 Page 45-52 / Register 1-7: Reserved.

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.164 Page 45-52 / Register 8-127: DAC Coefficients Buffer-A C(30:255)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients DAC Coefficient Buffer-A. Refer Table ?? for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

6.2.165 Page 62-70 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

6.2.166 Page 62-70 / Register 1-7: Reserved.

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. Write only default values

6.2.167 Page 62-70 / Register 8-127: DAC Coefficients Buffer-B C(0:255)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	xxxx xxxx	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table ?? for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

6.3 ADC Coefficients A+B

Table 6-2. ADC Coefficient Buffer-A Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	8	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C29	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C59	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C63	10	20	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 6-3. ADC Coefficient Buffer-B Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	26	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	26	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C29	26	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	27	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C59	27	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	27	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…		..	..	..	..	..
C63	28	20	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

6.4 ADC Defaults

Table 6-4. Default values of ADC Coefficients in Buffers A and B

ADC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	00170000H
C2	00170000H
C3	7DD30000H
C4	7FFFFF00H
C5,C6	00000000H
C7	7FFFFF00H
C8,..,C11	00000000H

Table 6-4. Default values of ADC Coefficients in Buffers A and B (continued)

ADC Buffer-A,B Coefficients	Default Value at reset
C12	7FFFFF00H
C13,..,C16	00000000H
C17	7FFFFF00H
C18,..,C21	00000000H
C22	7FFFFF00H
C23,..,C26	00000000H
C27	7FFFFF00H
C28,..,C35	00000000H
C36	7FFFFF00H
C37,C38	00000000H
C39	7FFFFF00H
C40,..,C43	00000000H
C44	7FFFFF00H
C45,..,C48	00000000H
C49	7FFFFF00H
C50,..,C53	00000000H
C54	7FFFFF00H
C55,..,C58	00000000H
C59	7FFFFF00H
C60,..,C63	00000000H

6.5 DAC Coefficients A+B

Table 6-5. DAC Coefficient Buffer-A Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	44	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	44	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..
C29	44	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	45	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..
C59	45	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	46	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..
C76	46	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 6-6. DAC Coefficient Buffer-B Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	62	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	62	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..
C29	62	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	63	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..

Table 6-6. DAC Coefficient Buffer-B Map (continued)

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C59	63	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	64	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
…	..	..	..	..	..	..
C76	64	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

6.6 DAC Defaults

Table 6-7. Default values of DAC Coefficients in Buffers A and B

DAC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	7FFFFF00H
C2,..,C5	00000000H
C6	7FFFFF00H
C7,..,C10	00000000H
C11	7FFFFF00H
C12,..,C15	00000000H
C16	7FFFFF00H
C17,..,C20	00000000H
C21	7FFFFF00H
C22,..,C25	00000000H
C26	7FFFFF00H
C27,..,C30	00000000H
C31,C32	00000000H
C33	7FFFFF00H
C34,..,C37	00000000H
C38	7FFFFF00H
C39,..,C42	00000000H
C43	7FFFFF00H
C44,..,C47	00000000H
C48	7FFFFF00H
C49,..,C52	00000000H
C53	7FFFFF00H
C54,..,C57	00000000H
C58	7FFFFF00H
C59,..,C64	00000000H
C65	7FFFFF00H
C66,C67	00000000H
C68	7FFFFF00H
C69,C70	00000000H
C71	7FF70000H
C72	10090000H
C73	7FEF0000H
C74,C75	00110000H
C76	7FDE0000H

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV320A3204IRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLV320AIC3204IRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TLV320AIC3204IRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

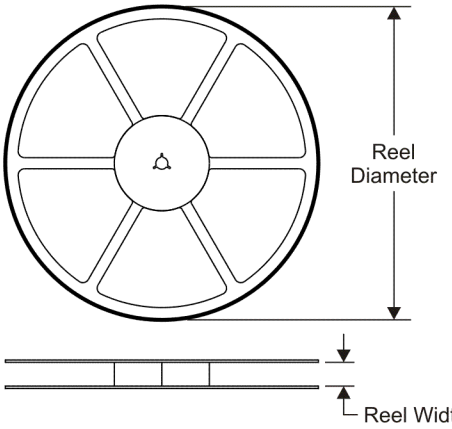
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

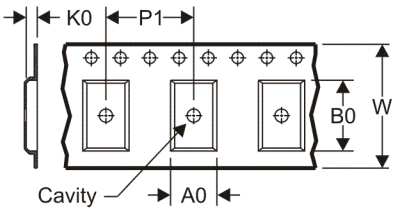
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

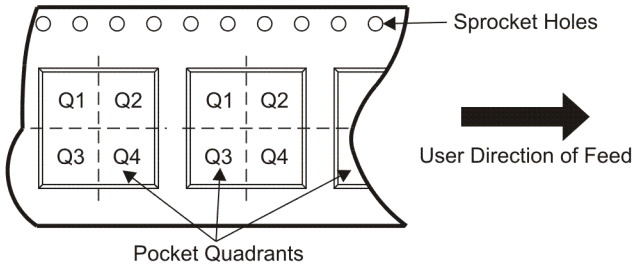


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

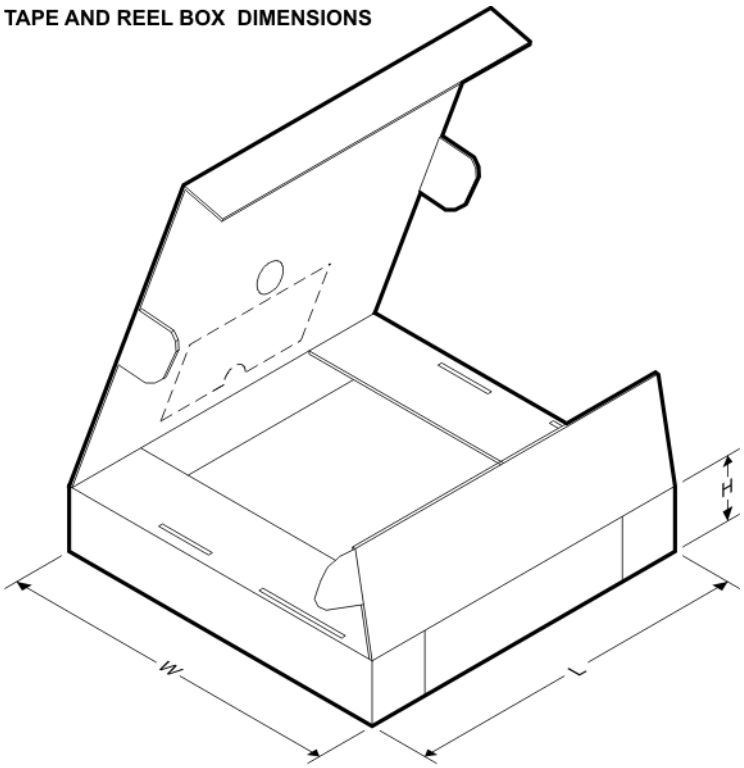
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3204IRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC3204IRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC3204IRHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC3204IRHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

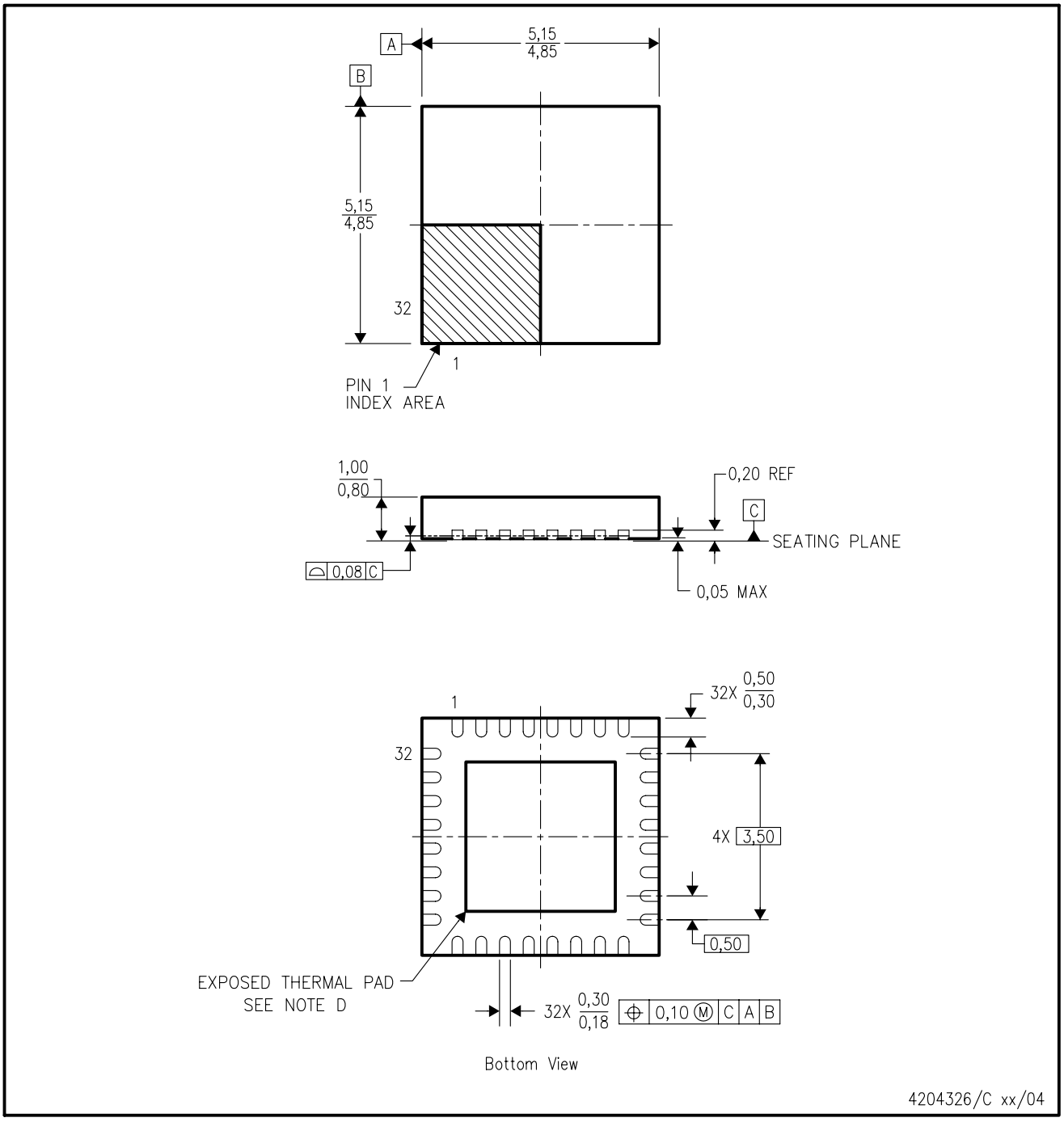
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3204IRHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TLV320AIC3204IRHBR	QFN	RHB	32	3000	346.0	346.0	29.0
TLV320AIC3204IRHBT	QFN	RHB	32	250	190.5	212.7	31.8
TLV320AIC3204IRHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

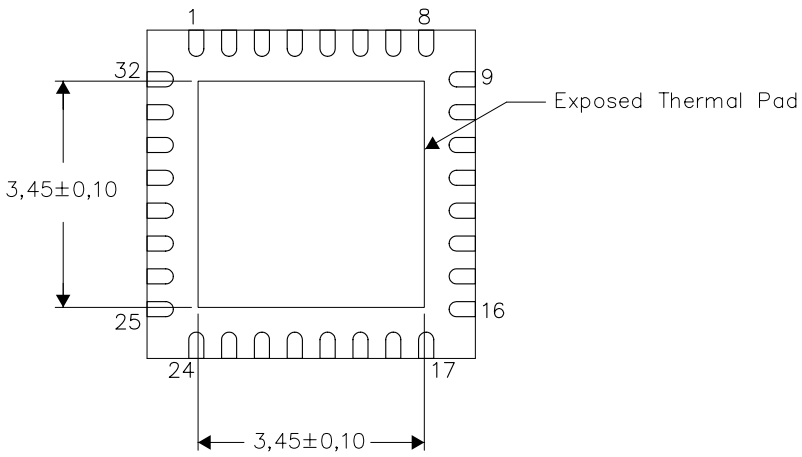
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



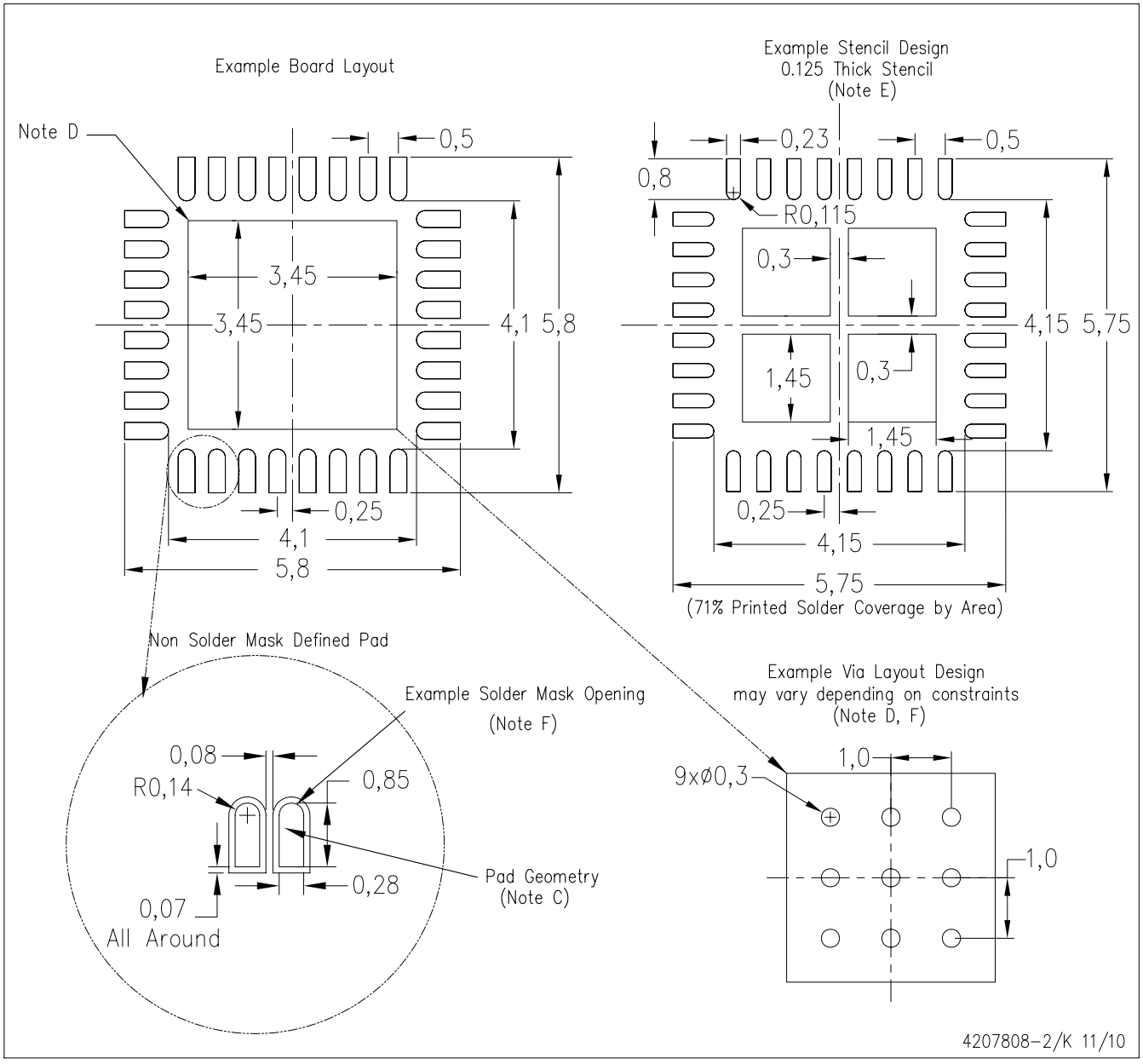
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/Q 11/10

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265