FAIRCHILD SEMICONDUCTOR™

June 1999
Revised June 2005

74LVT162240 • 74LVTH162240
Low Voltage 16-Bit Inverting Buffer/Line Driver with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

General Description

The LVT162240 and LVTH162240 contain sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVT162240 and LVTH162240 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162240 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These inverting buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162240 and LVTH162240 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162240), also available without bushold feature (74LVT162240)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Functionally compatible with the 74 series 162240
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

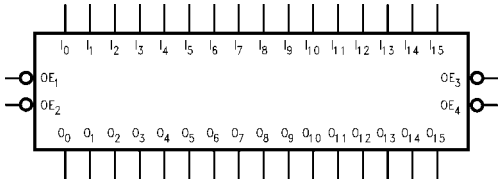
Ordering Code:

Order Number	Package Number	Package Description
74LVT162240MEA (Note 1)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162240MTD (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBE]
74LVTH162240MEX (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBE]
74LVTH162240MTX (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

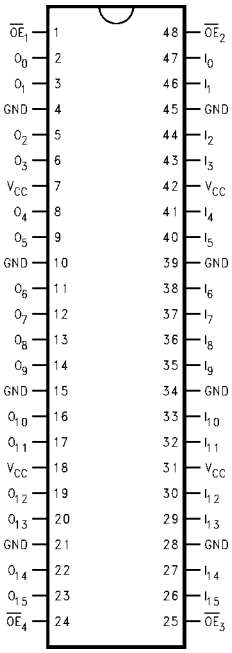
Note 1: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Note 2: Use this Order Number to receive devices in Tape and Reel.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active LOW)
I_0–I_{15}	Inputs
$\overline{O}_0$–$\overline{O}_{15}$	3-STATE Outputs

Truth Table

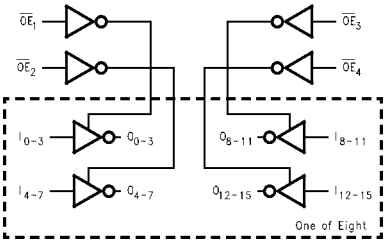
Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z
Inputs		**Outputs**
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z
Inputs		**Outputs**
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z
Inputs		**Outputs**
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The LVT162240 and LVTH162240 contain sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		−12	mA
I_{OL}	LOW-Level Output Current		12	mA
T_A	Free Air Operating Temperature	−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
				Min	Typ (Note 5)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6			0.8	V	$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC}−0.2			V	I_{OH} = −100 µA
			3.0	2.0				I_{OH} = −12 mA
V_{OL}	Output LOW Voltage		2.7			0.2	V	I_{OL} = 100 µA
			3.0			0.8		I_{OL} = 12 mA
$I_{I(HOLD)}$ (Note 6)	Bushold Input Minimum Drive		3.0	75			µA	V_I = 0.8V
				−75				V_I = 2.0V
$I_{I(OD)}$ (Note 6)	Bushold Input Over-Drive Current to Change State		3.0	500			µA	(Note 7)
				−500				(Note 8)
I_I	Input Current		3.6			10	µA	V_I = 5.5V
		Control Pins	3.6			±1		V_I = 0V or V_{CC}
		Data Pins	3.6			−5		V_I = 0V
						1		V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0			±100	µA	0V ≤ V_I or V_O ≤ 5.5V
$I_{PU/PD}$	Power Up/Down 3-STATE Current		0–1.5V			±100	µA	V_O = 0.5V to 3.0V V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6			−5	µA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current		3.6			5	µA	V_O = 3.0V
I_{OZH^+}	3-STATE Output Leakage Current		3.6			10	µA	V_{CC} < V_O ≤ 5.5V
I_{CCH}	Power Supply Current		3.6			0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current		3.6			5	mA	Outputs LOW
I_{CCZ}	Power Supply Current		3.6			0.19	mA	Outputs Disabled

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 5)	Max		
I_{CCZ+}	Power Supply Current	3.6			0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 9)	3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 5: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 6: Applies to bushold versions only (74LVTH162240).

Note 7: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 8: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 9: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 10)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 11)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 11)

Note 10: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 11: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 12)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.0	1.0	4.8	ns
t_{PHL}		1.0		4.0	1.0	4.6	
t_{PZH}	Output Enable Time	1.0		4.8	1.0	5.7	ns
t_{PZL}		1.0		4.9	1.0	6.1	
t_{PHZ}	Output Disable Time	2.0		4.9	2.0	5.4	ns
t_{PLZ}		2.0		4.5	2.0	4.5	
t_{OSHL}	Output to Output Skew			1.0		1.0	ns
t_{OSLH}	(Note 13)						

Note 12: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

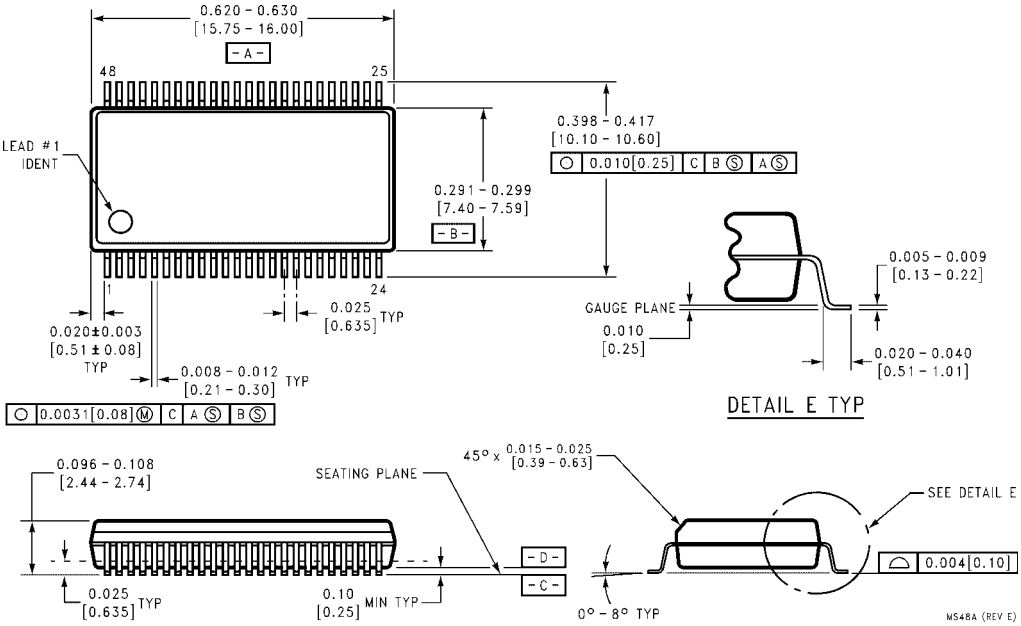
Note 13: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 14)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

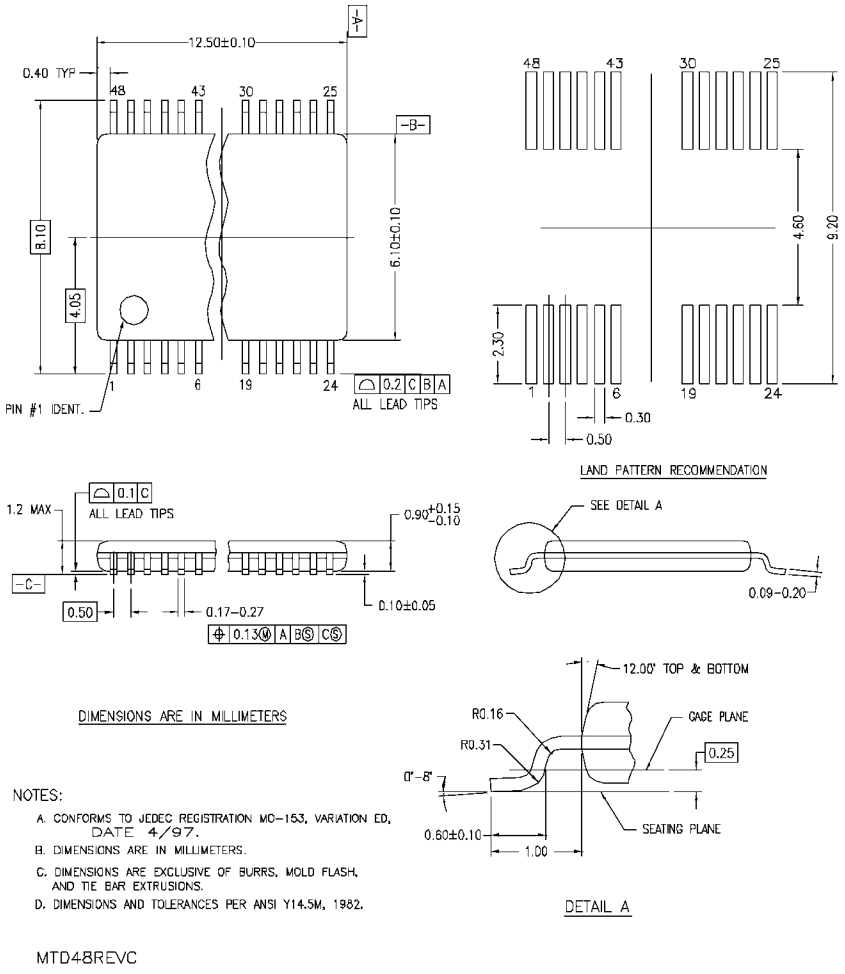
Note 14: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com