

Low-Power BiCMOS Current-Mode PWM

FEATURES

- 100 μ A Typical Starting Supply Current
- 500 μ A Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

DESCRIPTION

The UCC1800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

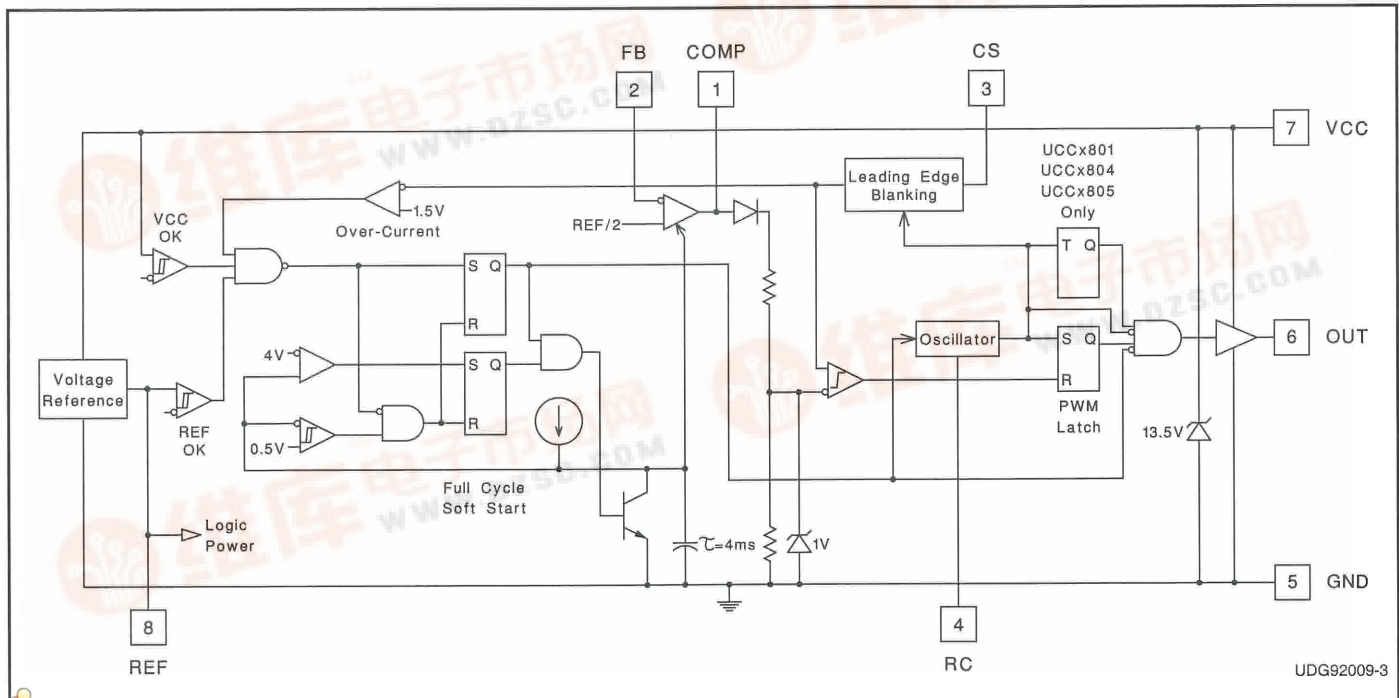
These devices have the same pin configuration as the UC1842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC1800/1/2/3/4/5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC1803 and UCC1805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC1802 and UCC1804 make these ideal choices for use in off-line power supplies.

The UCC180x series is specified for operation from -55°C to $+125^{\circ}\text{C}$, the UCC280x series is specified for operation from -40°C to $+85^{\circ}\text{C}$, and the UCC380x series is specified for operation from 0°C to $+70^{\circ}\text{C}$.

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx800	100%	5V	7.2V	6.9V
UCCx801	50%	5V	9.4V	7.4V
UCCx802	100%	5V	12.5V	8.3V
UCCx803	100%	4V	4.1V	3.6V
UCCx804	50%	5V	12.5V	8.3V
UCCx805	50%	4V	4.1V	3.6V

BLOCK DIAGRAM



UDG92009-3

[查询"UCC1805-SP"供应商](#)

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} Voltage (Note 2) 12.0V
 V_{CC} Current (Note 2) 30.0mA
 OUT Current ±1.0A
 OUT Energy (Capacitive Load) 20.0μJ
 Analog Inputs (FB, CS, RC, COMP)
 -0.3V to the lesser of 6.3V or V_{CC} + 0.3
 Power Dissipation at T_A < +25°C (N or J Package) 1.0W
 Power Dissipation at T_A < +25°C (D Package) 0.65W
 Power Dissipation at T_A < +25°C (L Package) 1.375W
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10 Seconds) +300°C

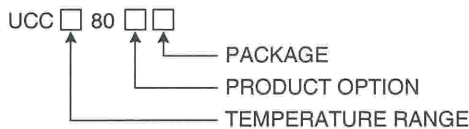
Note 1: Values beyond which damage may occur. All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitorde databook for information regarding thermal specifications and limitations of packages.

Note 2: In normal operation V_{CC} is powered through a current limiting resistor. Absolute maximum of 12V applies when V_{CC} is driven from a low impedance source such that I_{CC} does not exceed 30mA (which includes gate drive current requirement). The resistor should be sized so that the V_{CC} voltage, under operating conditions is below 12V but above the turn off threshold.

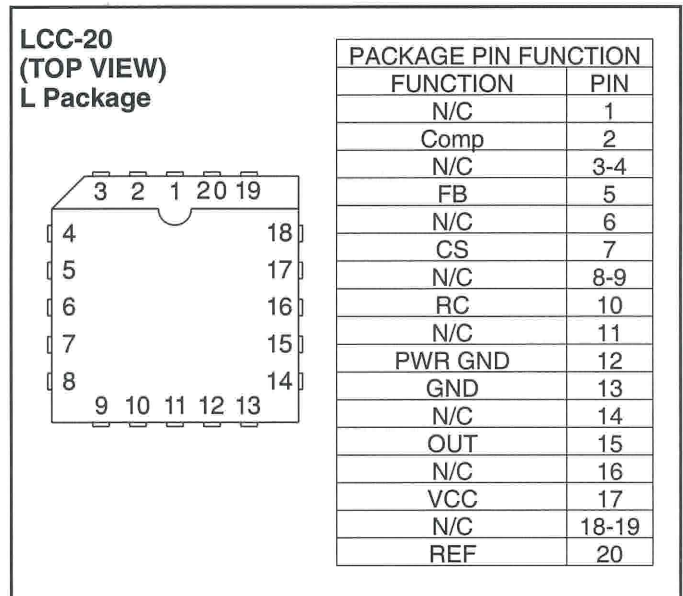
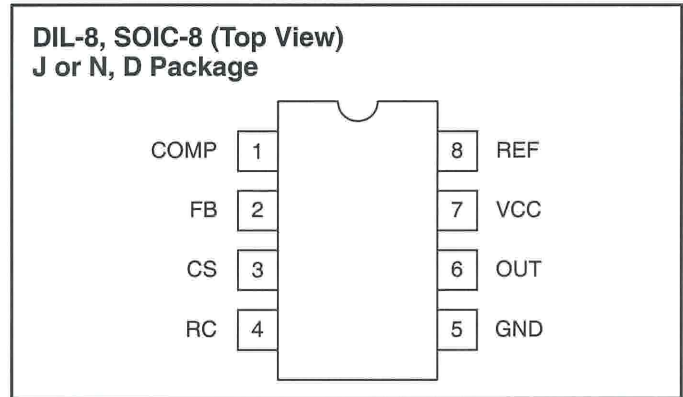
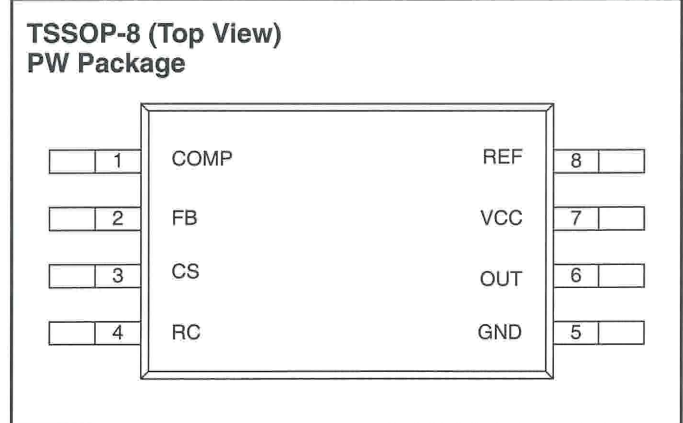
TEMPERATURE AND PACKAGE SELECTION

	Temperature Range	Available Packages
UCC180X	-55°C to +125°C	J, L
UCC280X	-40°C to +85°C	N, D, PW
UCC380X	0°C to +70°C	N, D, PW

ORDERING INFORMATION



CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for UCC180x; $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for UCC280x; $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for UCC380x; $V_{CC}=10\text{V}$ (Note 3); $RT=100\text{k}$ from REF to RC; $CT=330\text{pF}$ from RC to GND; 0.1 F capacitor from V_{CC} to GND; 0.1 F capacitor from V_{REF} to GND. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	$T_J=+25^{\circ}\text{C}$, $I=0.2\text{mA}$, UCCx800/1/2/4	4.925	5.00	5.075	4.925	5.00	5.075	V
	$T_J=+25^{\circ}\text{C}$, $I=0.2\text{mA}$, UCCx803/5	3.94	4.00	4.06	3.94	4.00	4.06	
Load Regulation	$0.2\text{mA} < I < 5\text{mA}$		10	30		10	25	mV
Line Regulation	$T_J=+25^{\circ}\text{C}$, $V_{CC}=10\text{V}$ to Clamp ($I_{VCC}=25\text{mA}$)			1.9			1.9	mV/V
	$T_J=-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC}=10\text{V}$ to Clamp ($I_{VCC}=25\text{mA}$)			2.5			2.1	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	4.88	5.00	5.10	4.88	5.00	5.10	V
	UCCx803/5 (Note 7)	3.90	4.00	4.08	3.90	4.00	4.08	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_J=+25^{\circ}\text{C}$ (Note 9)		130			130		μV
Long Term Stability	$T_A=+125^{\circ}\text{C}$, 1000 Hours (Note 9)		5			5		mV
Output Short Circuit		-5		-35	-5		-35	mA
Oscillator Section								
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	40	46	52	40	46	52	kHz
	UCCx803/5 (Note 4)	26	31	36	26	31	36	
Temperature Stability	(Note 9)		2.5			2.5		%
Amplitude peak-to-peak		2.25	2.40	2.55	2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45			2.45		V
Error Amplifier Section								
Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.44	2.50	2.56	2.44	2.50	2.56	V
	COMP=2.0V; UCCx803/5	1.95	2.0	2.05	1.95	2.0	2.05	
Input Bias Current		-1		1	-1		1	μA
Open Loop Voltage Gain		60	80		60	80		dB
COMP Sink Current	FB=2.7V, COMP=1.1V	0.3		3.5	0.4		2.5	mA
COMP Source Current	FB=1.8V, COMP=REF-1.2V	-0.2	-0.5	-0.8	-0.2	-0.5	-0.8	mA
Gain Bandwidth Product	(Note 9)		2			2		MHz
PWM Section								
Maximum Duty Cycle	UCCx800/2/3	97	99	100	97	99	100	%
	UCCx801/4/5	48	49	50	48	49	50	
Minimum Duty Cycle	COMP=0V			0			0	%
Current Sense Section								
Gain	(Note 5)	1.10	1.65	1.80	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP=5V (Note 6)	0.9	1.0	1.1	0.9	1.0	1.1	V
Input Bias Current		-200		200	-200		200	nA
CS Blank Time		50	100	150	50	100	150	ns
Over-Current Threshold		1.42	1.55	1.68	1.42	1.55	1.68	V
COMP to CS Offset	CS=0V	0.45	0.90	1.35	0.45	0.90	1.35	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for UCC180x; $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for UCC280x; $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for UCC380x; $V_{CC}=10\text{V}$ (Note 3); $RT=100\text{k}$ from REF to RC; $CT=330\text{pF}$ from RC to GND; $0.1 \mu\text{F}$ capacitor from V_{CC} to GND; $0.1 \mu\text{F}$ capacitor from V_{REF} to GND. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
Output Section								
OUT Low Level	I=20mA, all parts		0.1	0.4		0.1	0.4	V
	I=200mA, all parts		0.35	0.90		0.35	0.90	V
	I=50mA, VCC=5V, UCCx803/5		0.15	0.40		0.15	0.40	V
	I=20mA, VCC=0V, all parts		0.7	1.2		0.7	1.2	V
OUT High V_{SAT} (V_{CC} -OUT)	I=-20mA, all parts		0.15	0.40		0.15	0.40	V
	I=-200mA, all parts		1.0	1.9		1.0	1.9	V
	I=-50mA, VCC=5V, UCCx803/5		0.4	0.9		0.4	0.9	V
Rise Time	$C_L=1\text{nF}$		41	70		41	70	ns
Fall Time	$C_L=1\text{nF}$		44	75		44	75	ns
Undervoltage Lockout Section								
Start Threshold (Note 8)	UCCx800	6.6	7.2	7.8	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	8.6	9.4	10.2	V
	UCCx802/4	11.5	12.5	13.5	11.5	12.5	13.5	V
	UCCx803/5	3.7	4.1	4.5	3.7	4.1	4.5	V
Stop Threshold (Note 8)	UCCx1800	6.3	6.9	7.5	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8.0	6.8	7.4	8.0	V
	UCCx802/4	7.6	8.3	9.0	7.6	8.3	9.0	V
	UCCx803/5	3.2	3.6	4.0	3.2	3.6	4.0	V
Undervoltage Lockout Section (cont.)								
Start to Stop Hysteresis	UCCx800	0.12	0.3	0.48	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	1.6	2	2.4	V
	UCCx802/4	3.5	4.2	5.1	3.5	4.2	5.1	V
	UCCx803/5	0.2	0.5	0.8	0.2	0.5	0.8	V
Soft Start Section								
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V		4	10		4	10	ms
Overall Section								
Start-up Current	$V_{CC} < \text{Start Threshold}$		0.1	0.2		0.1	0.2	mA
Operating Supply Current	FB=0V, CS=0V		0.5	1.0		0.5	1.0	mA
VCC Internal Zener Voltage	$I_{CC}=10\text{mA}$ (Note 8), (Note 10)	12	13.5	15	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx802/4 (Note 8)	0.5	1.0		0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.

Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency.

Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.

Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \leq V_{CS} \leq 0.8\text{V}$.

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.

Note 7: Total Variation includes temperature stability and load regulation.

Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.

Note 9: Guaranteed by design. Not 100% tested in production.

Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3800 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

CS: CS is the input to the current sense comparators. The UCC3800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding $\pm 750\text{mA}$. OUT is actively held low when V_{CC} is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to V_{CC} . The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best

performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

$$\text{UCCx800/1/2/4: } F = \frac{1.5}{R \cdot C}$$

$$\text{UCCx803, UCCx805: } F = \frac{10}{R \cdot C}$$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

To prevent noise problems, bypass V_{CC} to GND with a ceramic capacitor as close to the V_{CC} pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When V_{CC} is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1 μF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

V_{CC} : V_{CC} is the power input connection for this device. In normal operation V_{CC} is powered through a current limiting resistor. Although quiescent V_{CC} current is very low, total supply current will be higher, depending on OUT current. Total V_{CC} current is the sum of quiescent V_{CC} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F.$$

There should be a minimum of 1.0 μF in parallel with a 0.1 μF ceramic capacitor from V_{CC} to ground located close to the device

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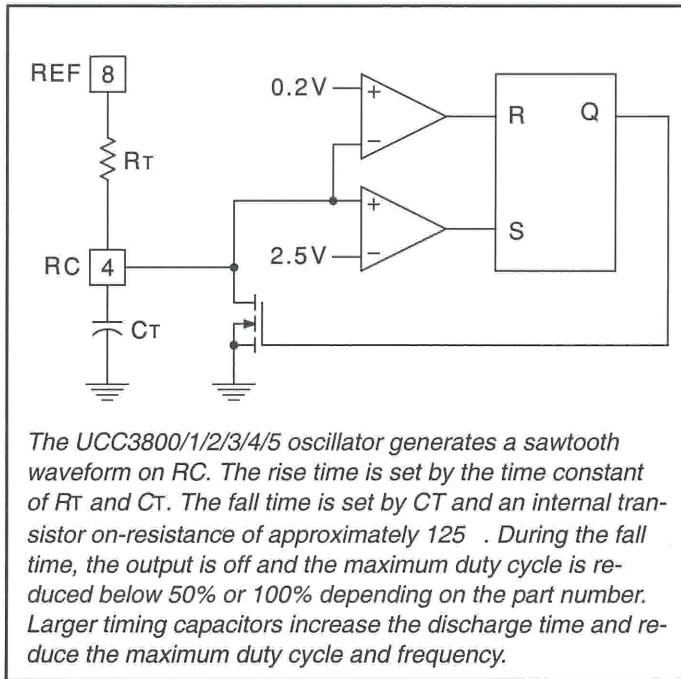


Figure 1. Oscillator.

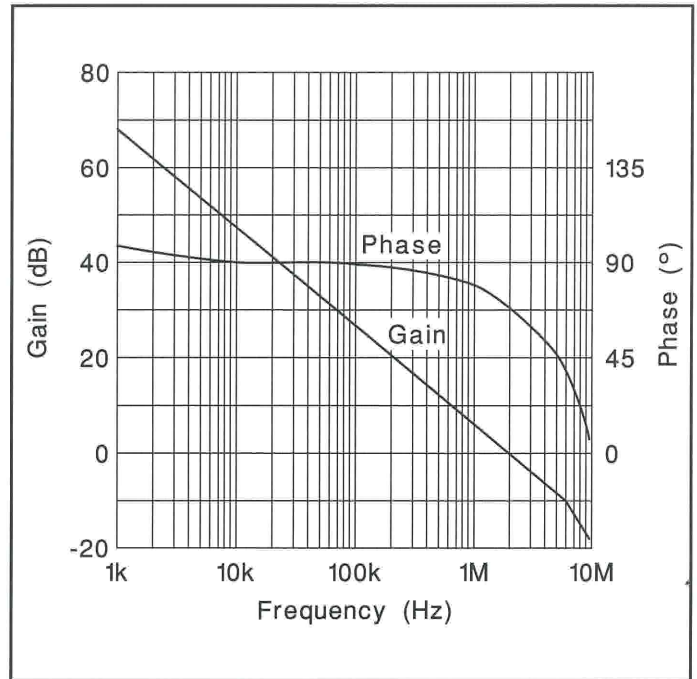


Figure 2. Error amplifier gain/phase response.

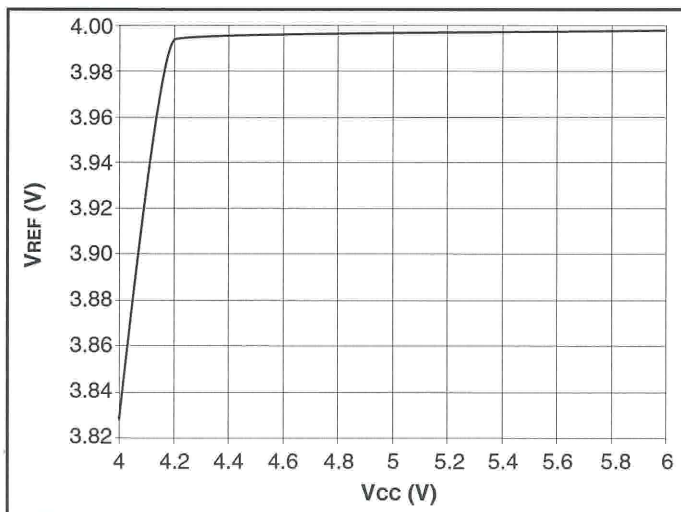


Figure 3. UCC1803/5 V_{REF} vs. V_{CC} ; $I_{LOAD} = 0.5mA$.

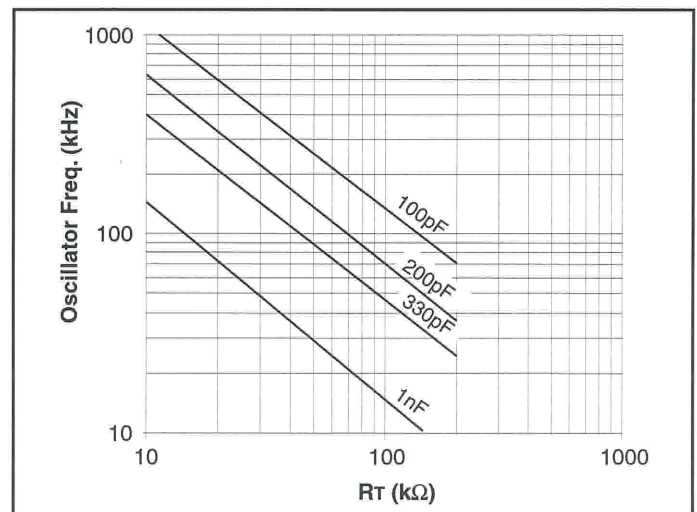


Figure 4. UCC1800/1/2/4 oscillator frequency vs. R_T and C_T .

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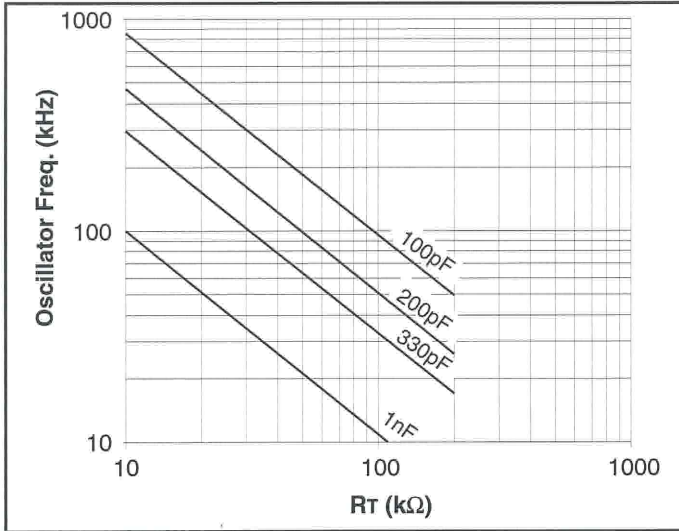


Figure 5. UCC1803/5 oscillator frequency vs. R_T and C_T .

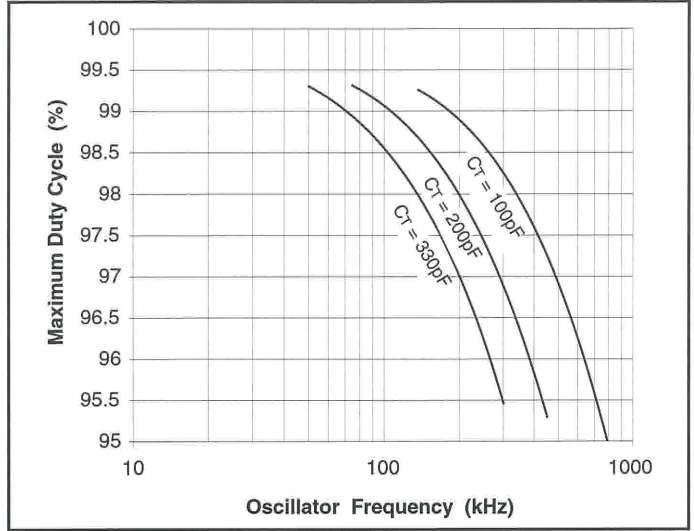


Figure 6. UCC1800/2/3 maximum duty cycle vs. oscillator frequency.

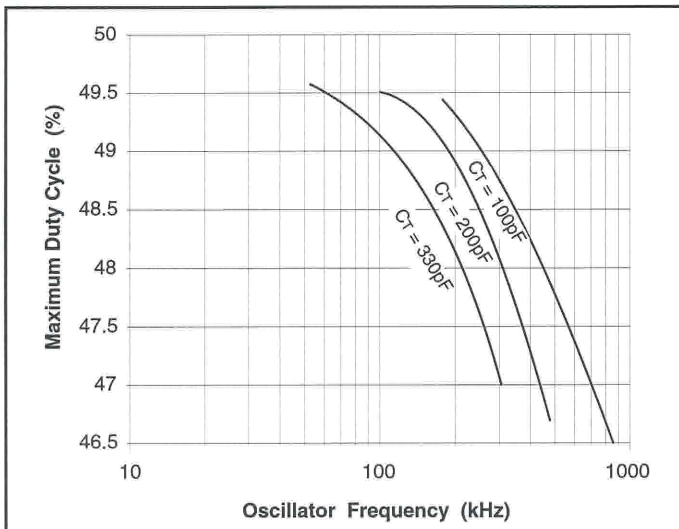


Figure 7. UCC1801/4/5 maximum duty cycle vs. oscillator frequency.

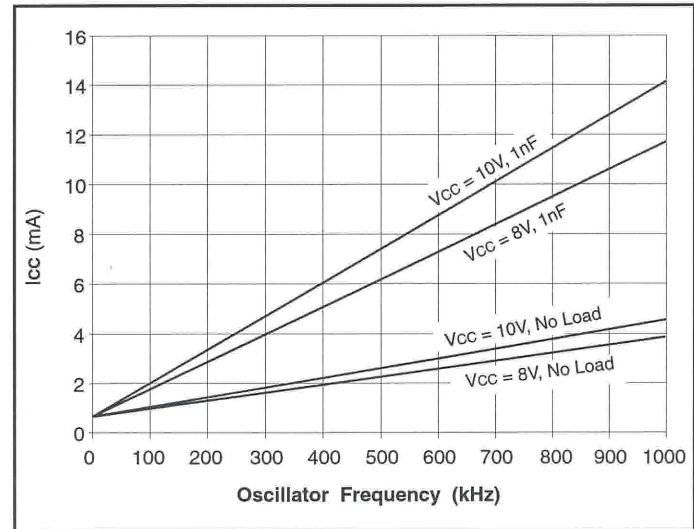


Figure 8. UCC1800 I_{CC} vs. oscillator frequency.

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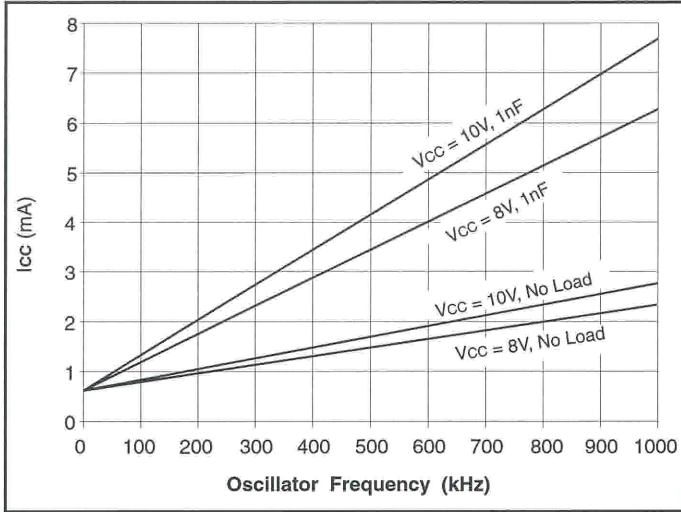


Figure 8. UCC1805 ICC vs. oscillator frequency.

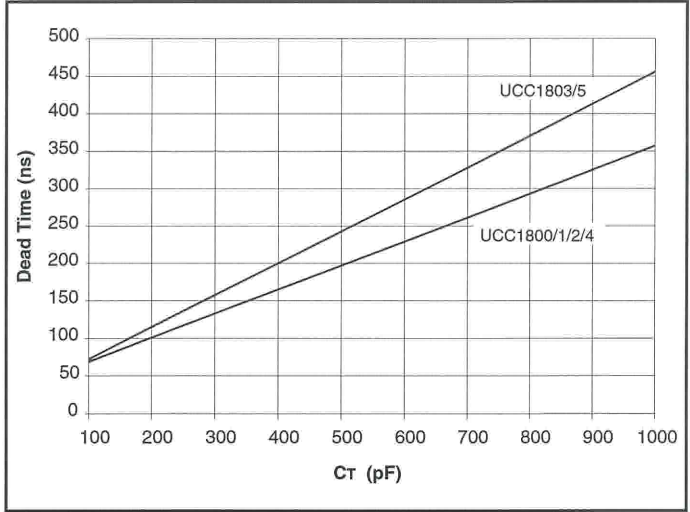


Figure 9. Dead time vs. C_T , $R_T = 100k$.

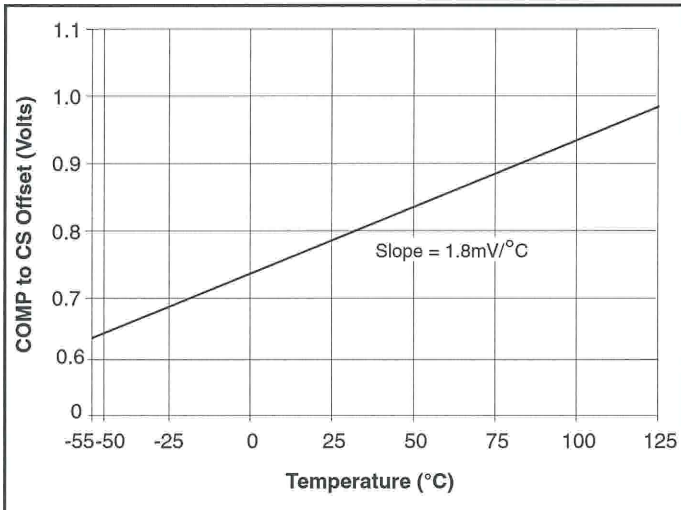


Figure 10. COMP to CS offset vs. temperature, CS = 0V.

REVISION HISTORY

8/2010 Revision A to Revision B

Updated Abs Max Table to read:

Analog Inputs (FB, CS, RC, COMP).....-0.3V to the lesser of 6.3V or VCC + 0.3V

From: Analog Inputs (FB, CS).....-0.3V to 6.3V



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PACKAG

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Pe
5962-9451301MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
5962-9451302MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
5962-9451303MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
5962-9451304MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
5962-9451305MPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
5962-9451305VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1800J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1800J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1800L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg
UCC1801J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1801J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1802J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1802J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1803J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1803J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1804J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1804J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC1805J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC1805J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC2800D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2800DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2800DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2800DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2800N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2800NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2800PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2800PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2801D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2801DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2801DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2801DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2801N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2801NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2801PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2801PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC2801QDRQ1G4	ACTIVE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2802D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2802DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2802DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2802DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2802J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC2802N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2802NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2802PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2802PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2803D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2803DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2803DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2803DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2803J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg
UCC2803N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2803NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2803PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC2803PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2803PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2803PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2804D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2804D/70021	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
UCC2804DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2804DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2804DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2804N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2804NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2804PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2804PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2804PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2804PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2805D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2805DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2805DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC2805DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC2805N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2805NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC2805PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC2805PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3800D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3800DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3800DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3800DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3800N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3800NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3800PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3800PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3801D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3801DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3801DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3801DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3801N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3801NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC3801PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3801PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3801PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3801PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3802D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3802DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3802DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3802DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3802N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3802NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3802PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3802PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3803D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3803DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3803DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3803DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3803N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3803NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC3803PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3803PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3803PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3803PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3804D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3804DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3804DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3804DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3804N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3804NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3804PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3804PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3804PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3804PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3805D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3805DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3805DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3805DTR/81222G4	PREVIEW	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pea
UCC3805DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
UCC3805N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3805NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg
UCC3805PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600
UCC3805PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-2600

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com> for more information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for high temperature applications.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (unless otherwise designated as "Green (RoHS & no Br/Sb) flame retardant" in homogeneous material).

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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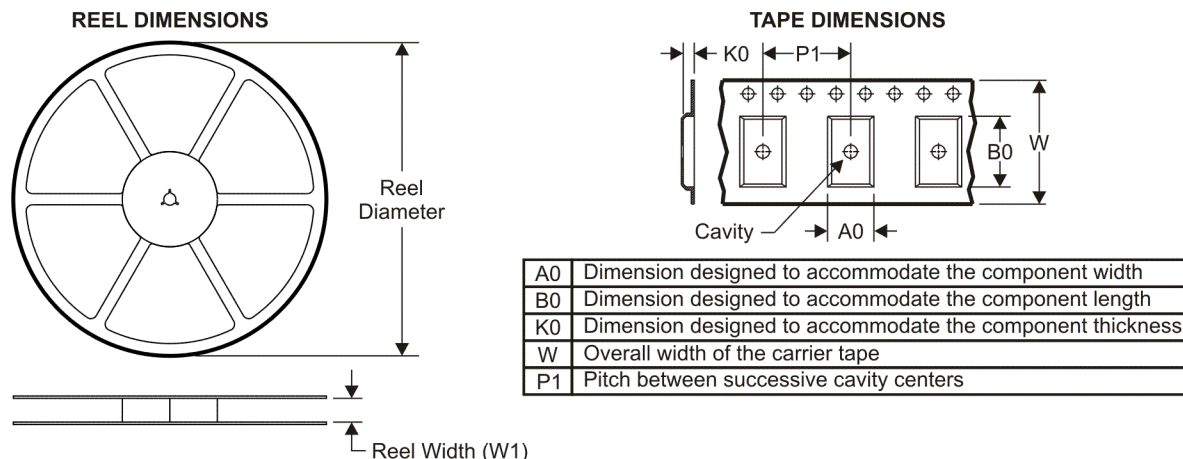
OTHER QUALIFIED VERSIONS OF UCC1800, UCC1801, UCC1802, UCC1803, UCC1804, UCC1805, UCC1805-SP, UCC2800, UCC2801, UCC2802, UCC2803, UCC2803M, UCC2804, UCC2805, UCC3800, UCC3801, UCC3802, UCC3803, UCC3804, UCC3805 :

- Catalog: [UCC3800](#), [UCC3801](#), [UCC3802](#), [UCC3803](#), [UCC3804](#), [UCC3805](#), [UCC1805](#), [UCC2802](#), [UCC2803](#)
- Automotive: [UCC2800-Q1](#), [UCC2801-Q1](#), [UCC2802-Q1](#), [UCC2802-Q1](#), [UCC2803-Q1](#), [UCC2803-Q1](#), [UCC2804-Q1](#), [UCC2805-Q1](#)
- Enhanced Product: [UCC2800-EP](#), [UCC2801-EP](#), [UCC2802-EP](#), [UCC2802-EP](#), [UCC2803-EP](#), [UCC2803-EP](#), [UCC2804-EP](#), [UCC2805-EP](#)
- Military: [UCC2802M](#), [UCC2803M](#), [UCC1800](#), [UCC1801](#), [UCC1802](#), [UCC1803](#), [UCC1804](#), [UCC1805](#)
- Space: [UCC1805-SP](#)

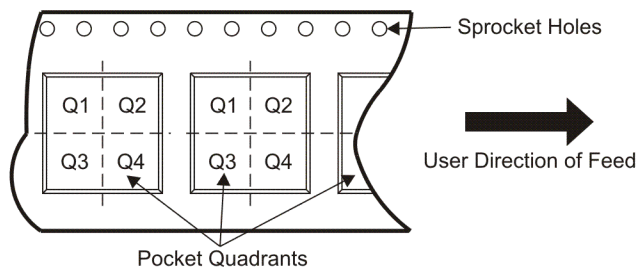
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

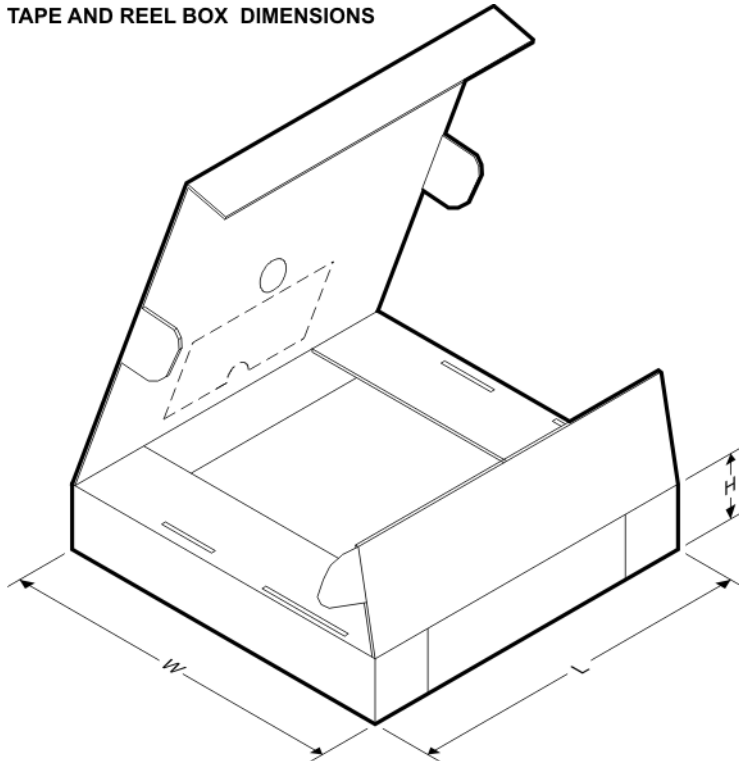


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2800DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2801DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2802DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2803DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2803PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2804DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2804PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC2805DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3800DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3801DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3801PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3802DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3803DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3803PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3804DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3804PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3805DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

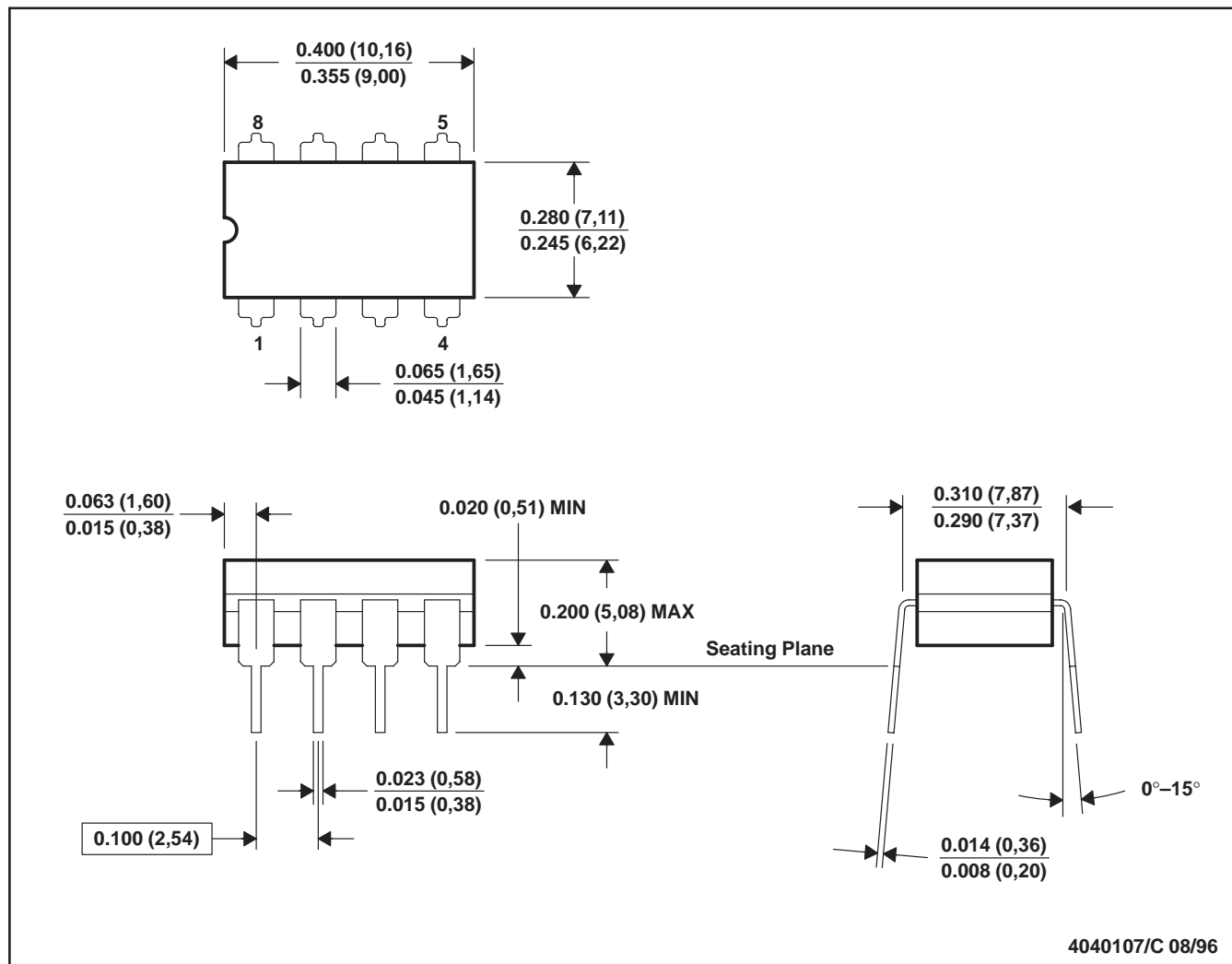
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2800DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2801DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2802DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2803DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2803PWTR	TSSOP	PW	8	2000	346.0	346.0	29.0
UCC2804DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC2804PWTR	TSSOP	PW	8	2000	346.0	346.0	29.0
UCC2805DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3800DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3801DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3801PWTR	TSSOP	PW	8	2000	346.0	346.0	29.0
UCC3802DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3803DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3803PWTR	TSSOP	PW	8	2000	346.0	346.0	29.0
UCC3804DTR	SOIC	D	8	2500	340.5	338.1	20.6
UCC3804PWTR	TSSOP	PW	8	2000	346.0	346.0	29.0
UCC3805DTR	SOIC	D	8	2500	340.5	338.1	20.6

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

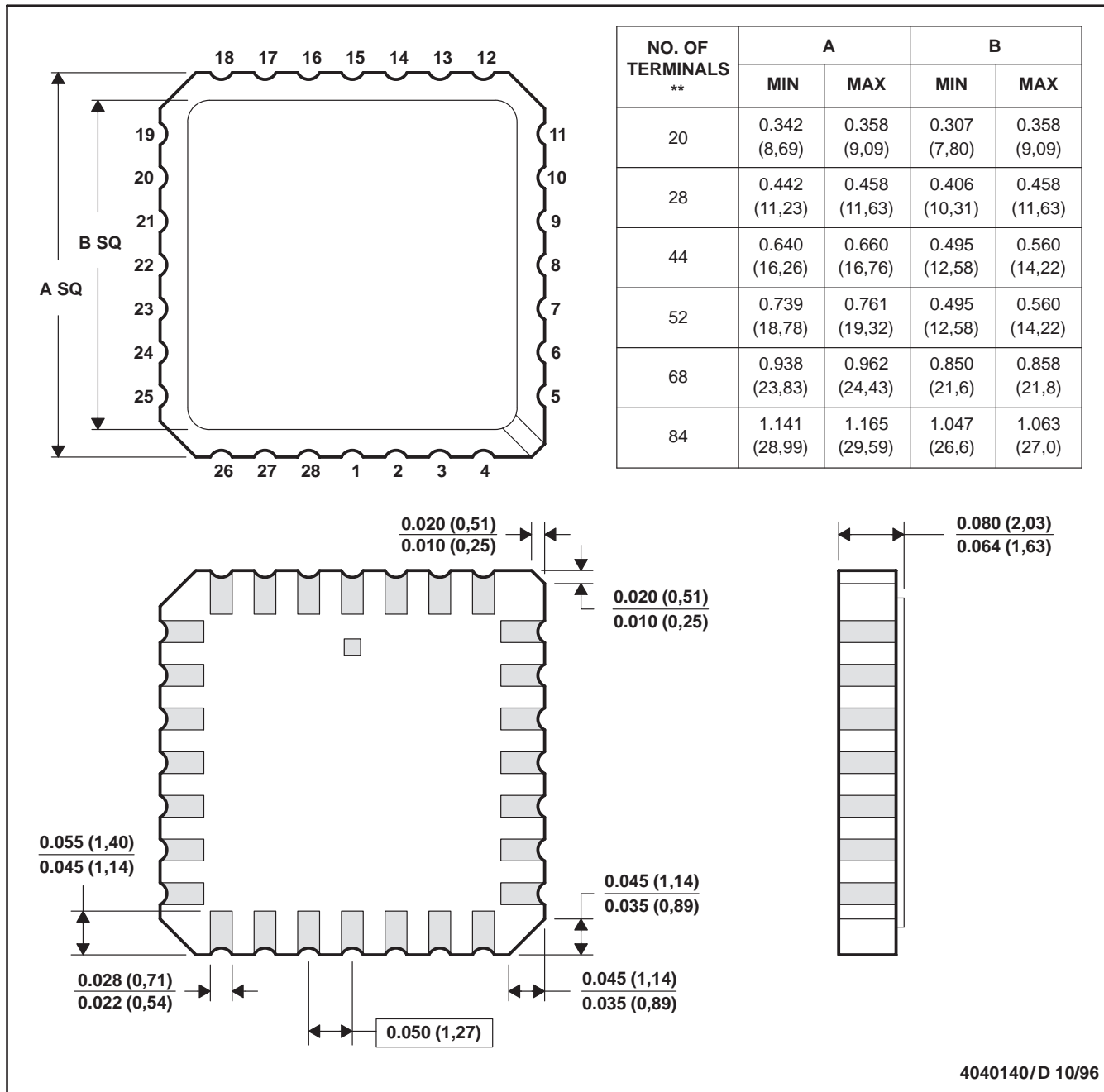


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

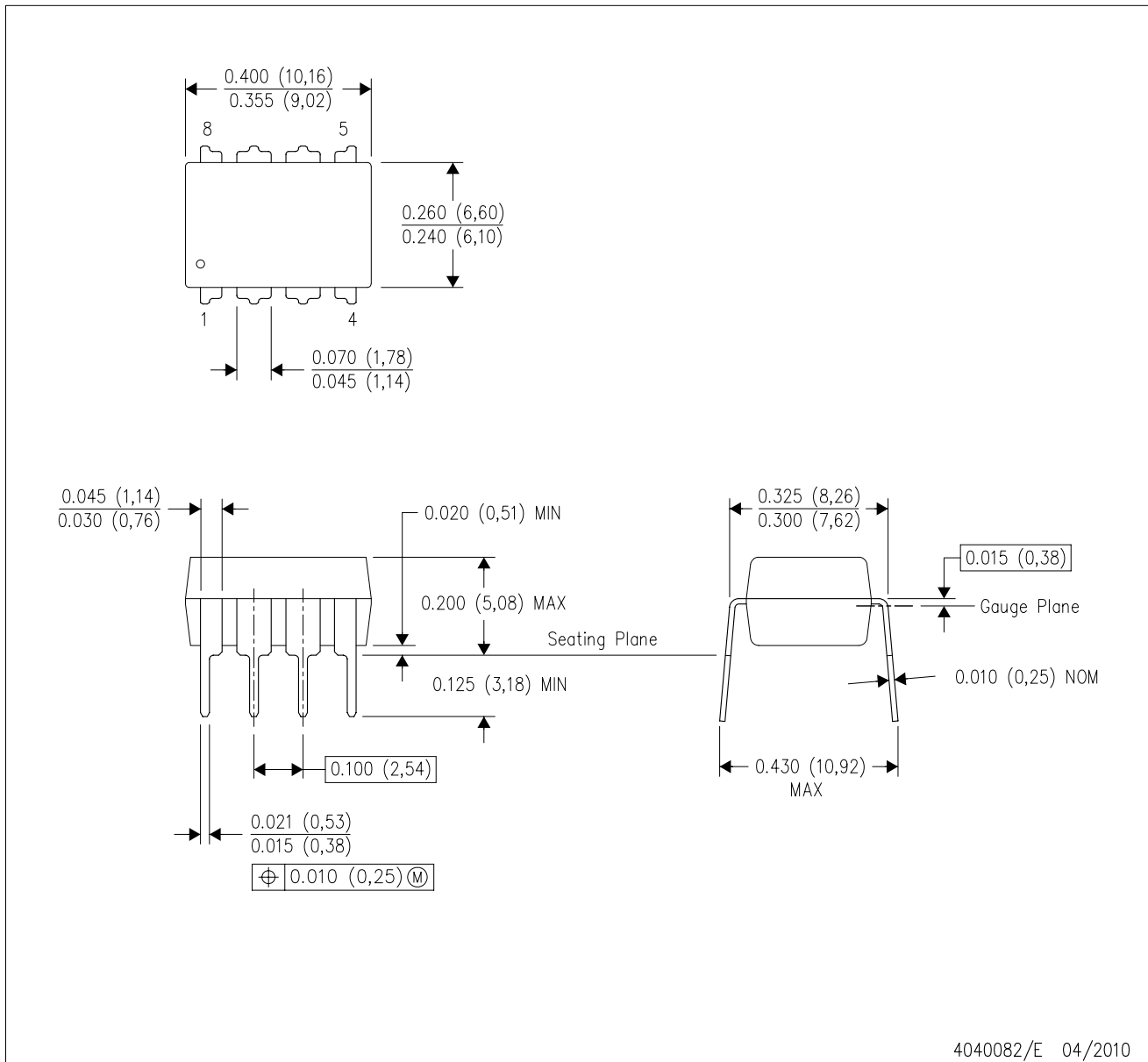


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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P (R-PDIP-T8)

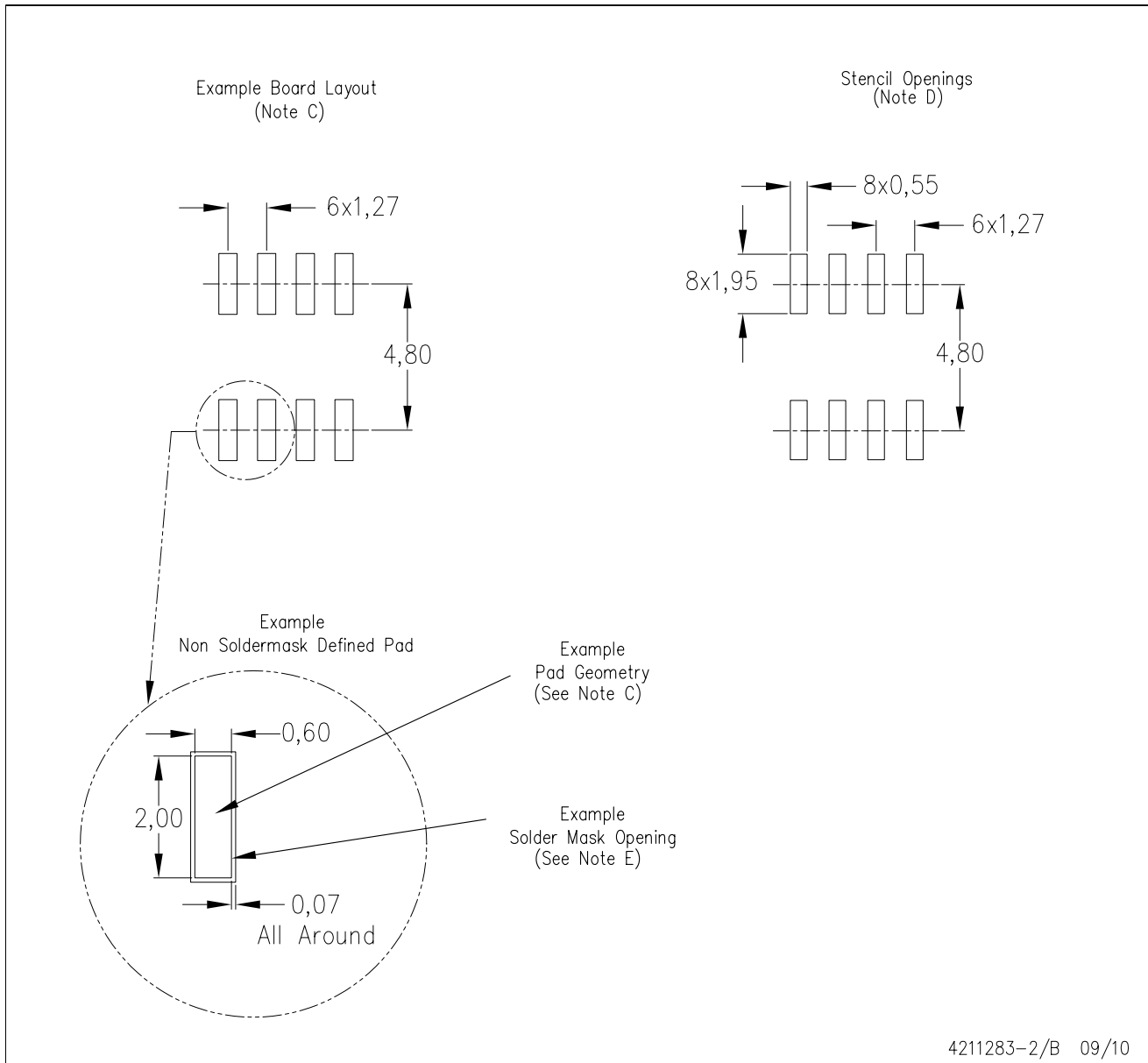
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

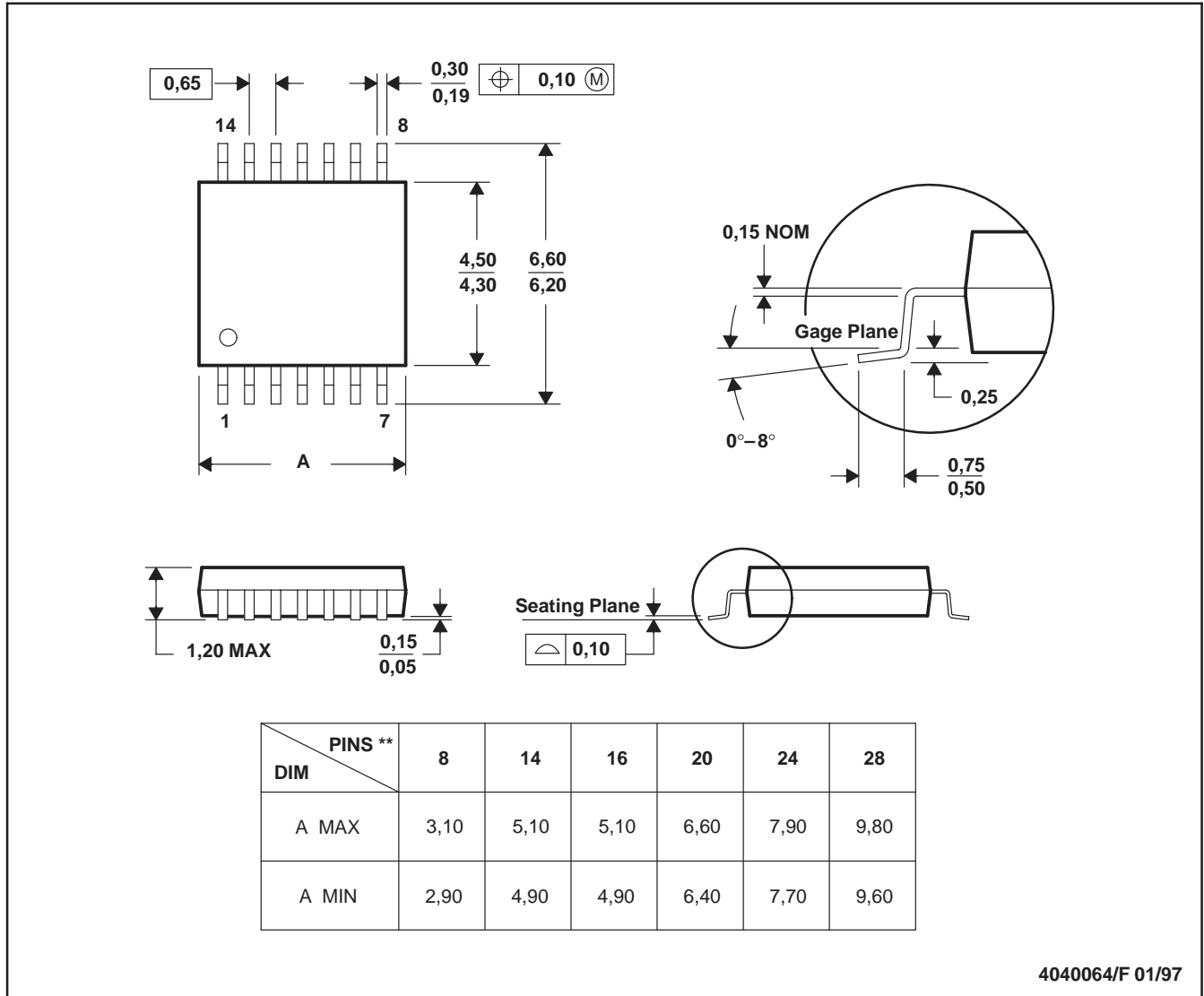


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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