

N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^e	Q_g (Typ.)
12	0.0038 at $V_{GS} = 4.5$ V	40	41 nC
	0.0047 at $V_{GS} = 2.5$ V	40	

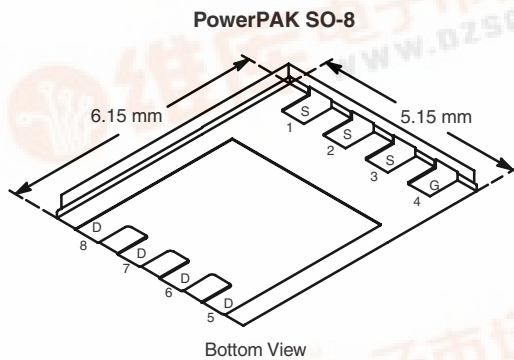
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- Low Thermal Resistance PowerPAK[®] Package with Small Size and Low 1.07 mm Profile
- 100 % R_g Tested



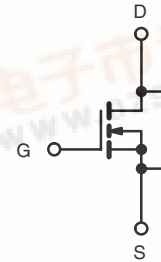
APPLICATIONS

- Secondary Synchronous Rectification
- Point-of-Load
- Load Switch



Bottom View

Ordering Information: SiR492DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	40 ^e	A
	$T_C = 70^\circ\text{C}$	35 ^e	
	$T_A = 25^\circ\text{C}$	27 ^{a, b}	
	$T_A = 70^\circ\text{C}$	21.6 ^{a, b}	
Pulsed Drain Current	I_{DM}	60	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	30	
	$T_A = 25^\circ\text{C}$	3.5 ^{a, b}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	36	W
	$T_C = 70^\circ\text{C}$	23	
	$T_A = 25^\circ\text{C}$	4.2 ^{a, b}	
	$T_A = 70^\circ\text{C}$	2.7 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 50 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t = 10$ s.c. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Package limited, pulse time ≤ 200 ms.

SiR492DP

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THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	25	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.9	3.5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 70 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		12		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 3.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 12$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 15$ A		0.0031	0.0038	Ω
		$V_{GS} = 2.5$ V, $I_D = 10$ A		0.0037	0.0047	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 5$ V, $I_D = 15$ A		110		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 6$ V, $V_{GS} = 0$ V, $f = 1$ MHz		3720		pF
Output Capacitance	C_{oss}			1290		
Reverse Transfer Capacitance	C_{rss}			840		
Total Gate Charge	Q_g	$V_{DS} = 6$ V, $V_{GS} = 8$ V, $I_D = 10$ A		73	110	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 6$ V, $V_{GS} = 4.5$ V, $I_D = 10$ A		41	62	
Gate-Drain Charge	Q_{gd}			4.5		
				8.5		
Gate Resistance	R_g	$f = 1$ MHz		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6$ V, $R_L = 1.2$ Ω $I_D \cong 5$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		27	41	ns
Rise Time	t_r			125	190	
Turn-Off Delay Time	$t_{d(off)}$			53	80	
Fall Time	t_f			12	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6$ V, $R_L = 1.2$ Ω $I_D \cong 5$ A, $V_{GEN} = 8$ V, $R_g = 1$ Ω		16	25	
Rise Time	t_r			55	85	
Turn-Off Delay Time	$t_{d(off)}$			53	80	
Fall Time	t_f			9	15	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			35	A
Pulse Diode Forward Current ^a	I_{SM}				60	
Body Diode Voltage	V_{SD}	$I_S = 3.2\text{ A}$		0.61	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		46	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			30	50	nC
Reverse Recovery Fall Time	t_a			20		ns
Reverse Recovery Rise Time	t_b			26		

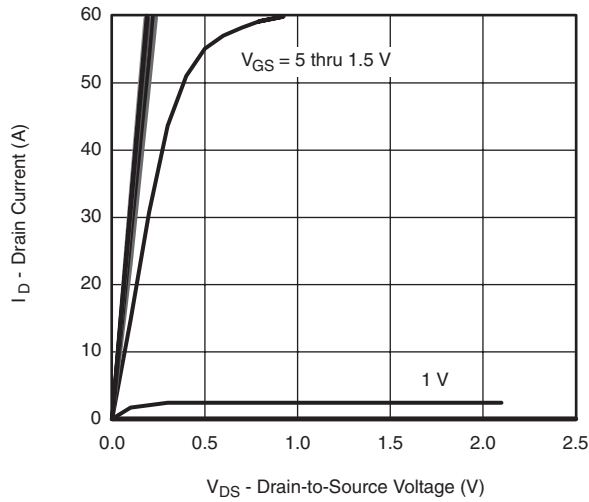
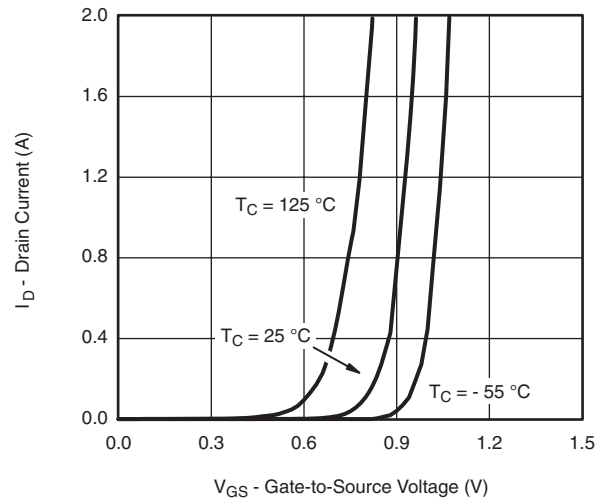
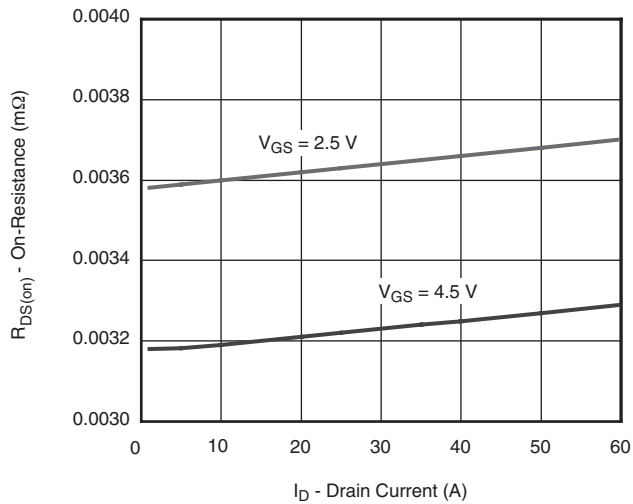
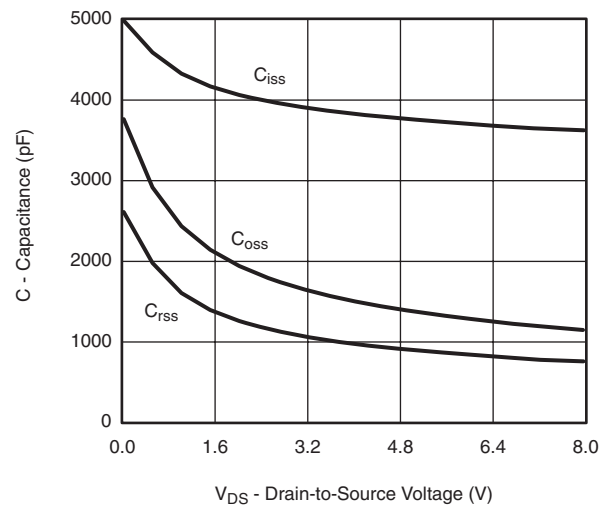
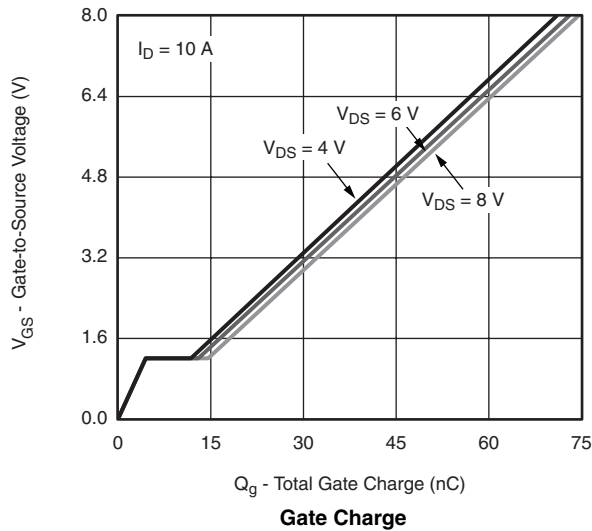
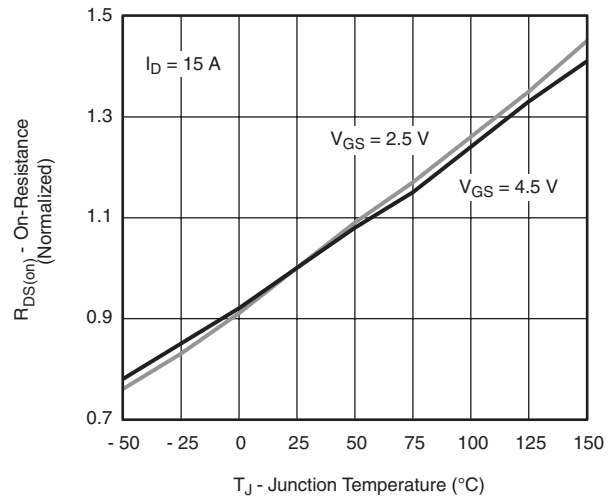
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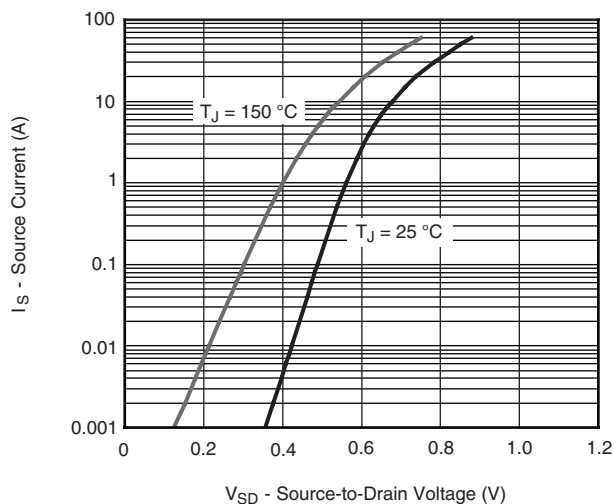
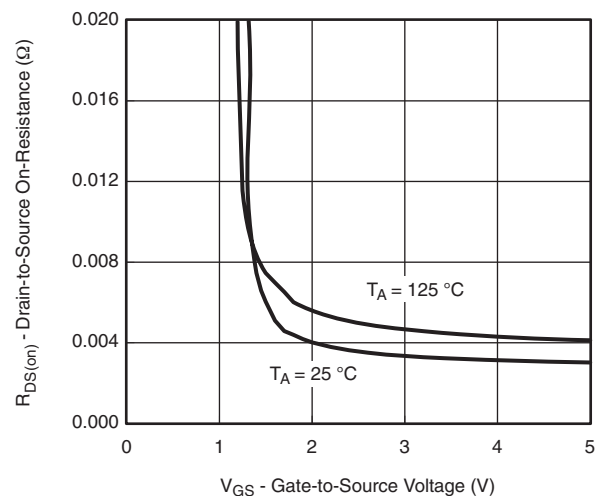
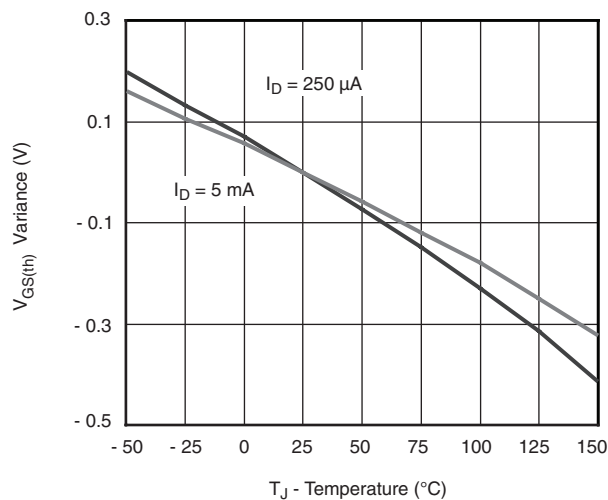
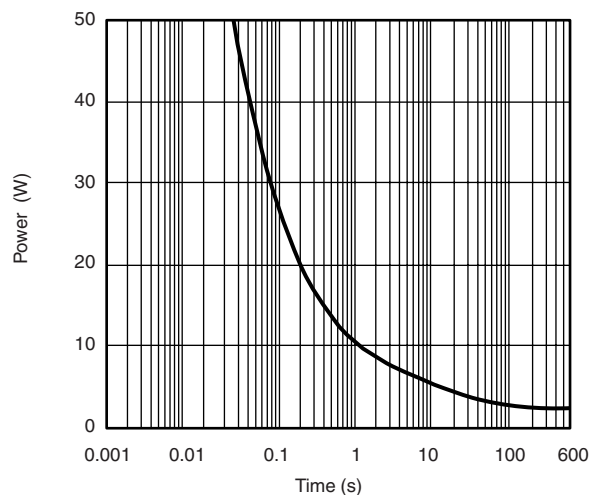
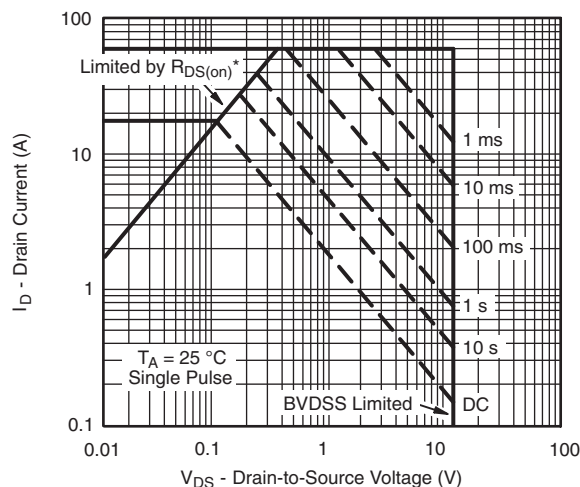
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiR492DP

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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

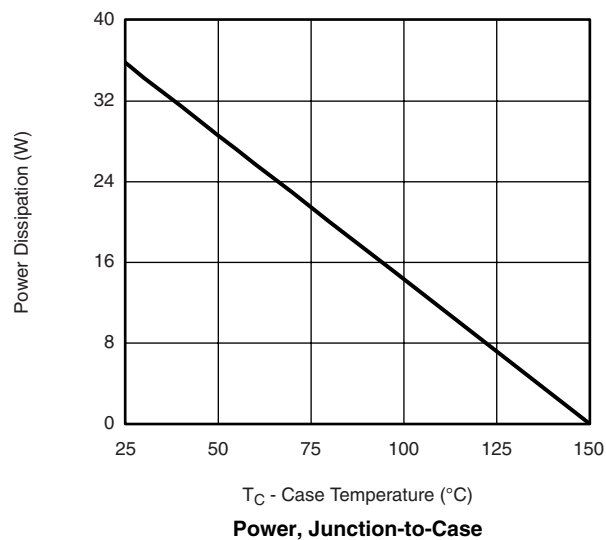
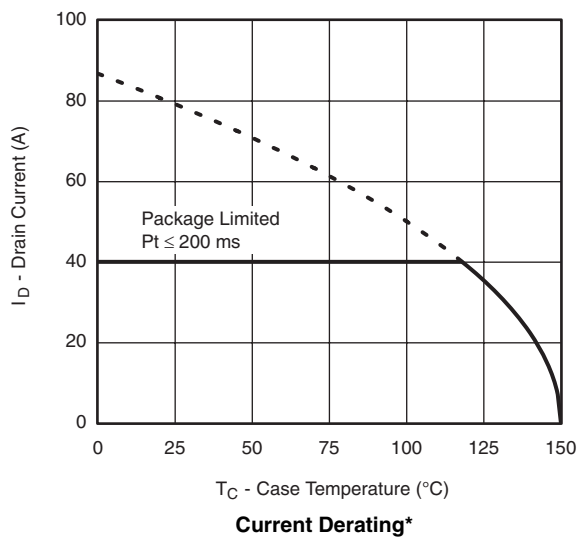
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

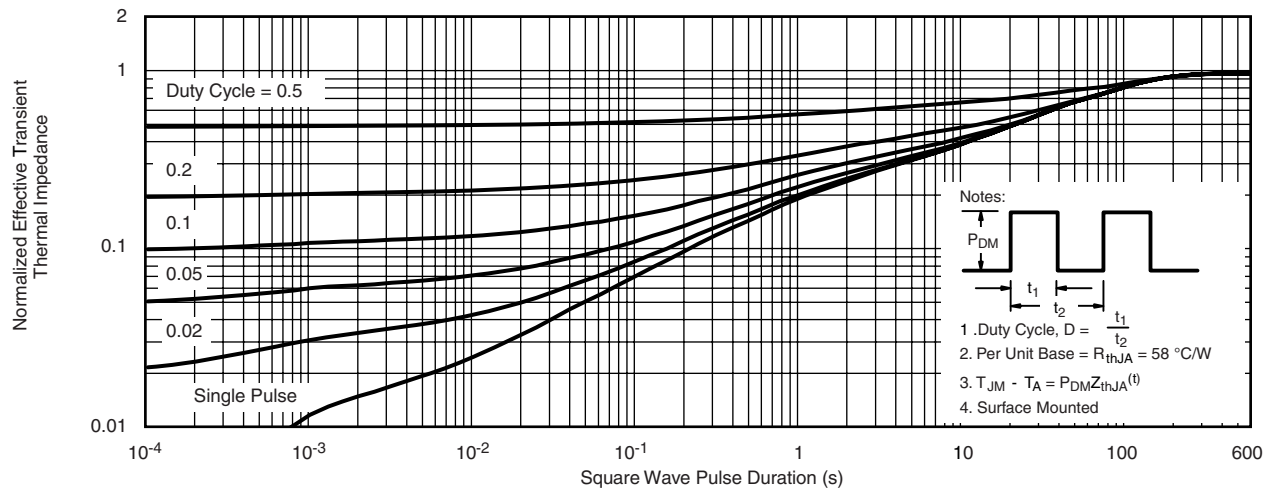


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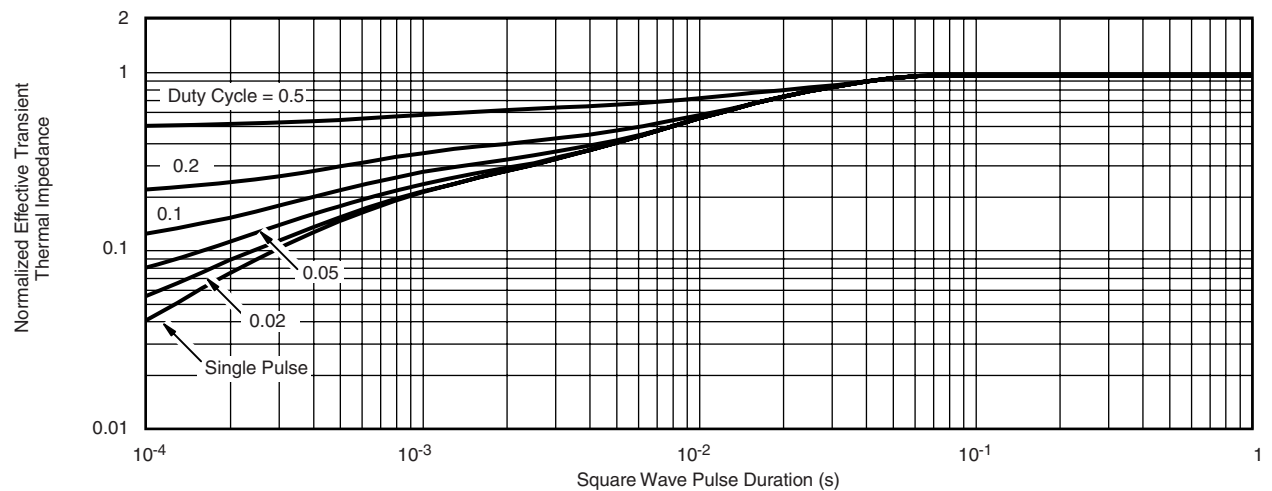
New Product

SiR492DP
Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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