

查询“74HC/HCT4353”供应商

FEATURES

- Wide analog input voltage range: ± 5 V
- Low "ON" resistance:
80 Ω (typ.) at $V_{CC} - V_{EE} = 4.5$ V
70 Ω (typ.) at $V_{CC} - V_{EE} = 6.0$ V
60 Ω (typ.) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation:
to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4353 are high-speed Si-gate CMOS devices.

They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4353 are triple 2-channel analog multiplexers/demultiplexers with two common enable inputs (E_1 and E_2) and a latch enable input (LE). Each multiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and select inputs (S_1 to S_3).

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PZH} /t _{PZL}	turn "ON" time E_1, E_2 or S_n to V_{os}	$C_L = 50$ pF $R_L = 1$ k Ω $V_{CC} = 5$ V	29	21	ns
t _{PHZ} /t _{PLZ}	turn "OFF" time E_1, E_2 or S_n to V_{os}		20	22	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	23	23	pF
C _S	max. switch capacitance independent (Y) common (Z)		5 8	5 8	pF

$V_{EE} = GND = 0$ V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} \text{ where:}$$

$$\begin{aligned} f_i &= \text{input frequency in MHz} & C_L &= \text{output load capacitance in pF} \\ f_o &= \text{output frequency in MHz} & C_S &= \text{max. switch capacitance in pF} \\ \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} &= \text{sum of outputs} & V_{CC} &= \text{supply voltage in V} \end{aligned}$$

2. For HC the condition is $V_I = GND$ to V_{CC} .

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

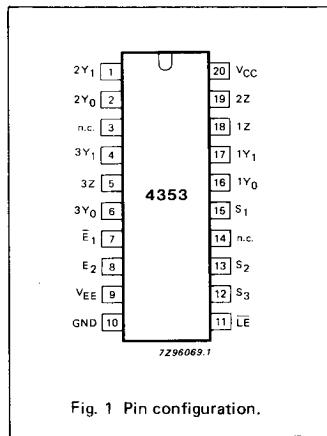


Fig. 1 Pin configuration.

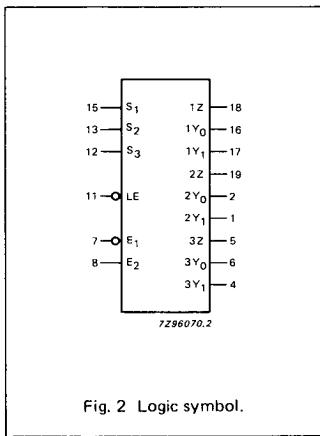


Fig. 2 Logic symbol.

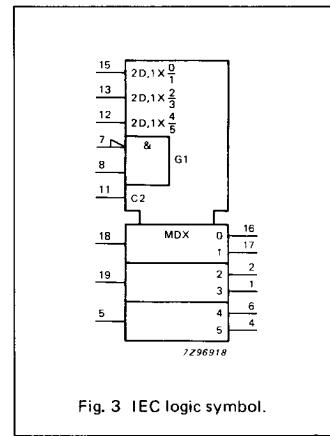


Fig. 3 IEC logic symbol.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	2Y ₀ , 2Y ₁	independent inputs/outputs
5	3Z	common input/output
6, 4	3Y ₀ , 3Y ₁	independent inputs/outputs
3, 14	n.c.	not connected
7	Ē ₁	enable input (active LOW)
8	E ₂	enable input (active HIGH)
9	V _{EE}	negative supply voltage
10	GND	ground (0 V)
11	LE	latch enable input (active LOW)
15, 13, 12	S ₁ to S ₃	select inputs
16, 17	1Y ₀ , 1Y ₁	independent inputs/outputs
18	1Z	common input/output
19	2Z	common input/output
20	V _{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				CHANNEL ON
Ē ₁	E ₂	LE	S _n	
H	X	X	X	none
X	L	X	X	none
L	H	H	L	nY ₀ – nZ
L	H	H	H	nY ₁ – nZ
L	H	L	X	*
X	X	↓	X	**

H = HIGH voltage level

* Last selected channel "ON".

L = LOW voltage level

** Selected channels latched.

X = don't care

↓ = HIGH-to-LOW LE transition

GENERAL DESCRIPTION

Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an independent input/output (nY₀ and nY₁) and the other side connected to a common input/output (nZ).

With Ē₁ LOW and E₂ HIGH, one of the two switches is selected (low impedance ON-state) by S₁ to S₃.

The data at the select inputs may be latched by using the active LOW latch enable input (LE). When LE is HIGH, the latch is transparent. When either of the two enable inputs, Ē₁ (active LOW) and E₂ (active HIGH), is inactive, all analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S₁ to S₃, LE, Ē₁ and E₂). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY₀ and nY₁, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} – V_{EE} may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

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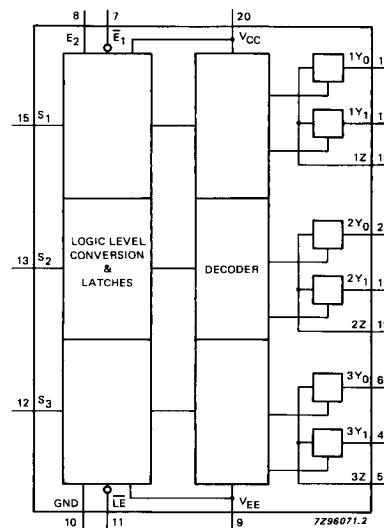


Fig. 4 Functional diagram.

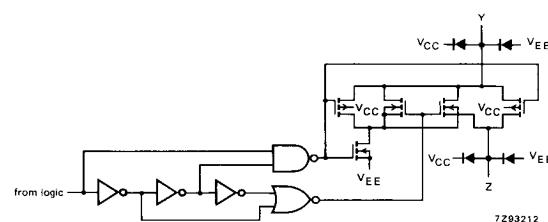


Fig. 5 Schematic diagram (one switch).

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_K$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V < V_S < $V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}$ $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC} - V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V $V_{CC} = 10.0$ V

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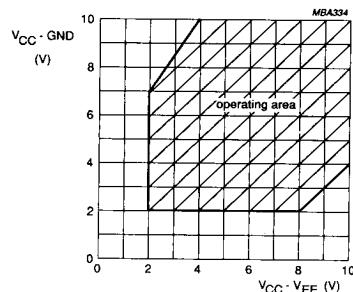


Fig. 6 Guaranteed operating area as a function of the supply voltages for 74HC4353.

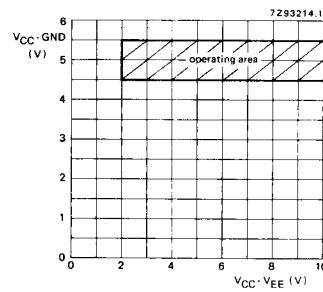


Fig. 7 Guaranteed operating area as a function of the supply voltages for 74HCT4353.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V
For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V ; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

SYMBOL	PARAMETER	T_{amb} ($^{\circ}\text{C}$)						UNIT	TEST CONDITIONS									
		74HC/HCT							V_{CC} V	V_{EE} V	I_S μA	V_{IS}	V_I					
		+25		-40 to +85		-40 to +125												
		min.	typ.	max.	min.	max.	min.	max.										
R_{ON}	ON resistance (peak)	—	100 90 70	180 160 130	—	225 200 165	—	270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC} to V_{EE}	V_{IH} or V_{IL}				
R_{ON}	ON resistance (rail)	150 80 70 60	— 140 120 105	— 175 150 130	— 210 180 160	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{EE}	V_{IH} or V_{IL}							
R_{ON}	ON resistance	150 90 80 65	— 160 140 120	— 200 175 150	— 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}							
ΔR_{ON}	maximum ΔR_{ON} resistance between any two channels	— 9 8 6	— 180 160 140 120	— 200 175 150	— 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 4.5	0 0 0 -4.5	— — — —	V_{CC} to V_{EE}	V_{IH} or V_{IL}							

Notes to DC characteristics

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig. 8.

查询"74HC4353D-T"供应商

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS							
		74HC							V _{CC} V	V _{EE} V	V _I	OTHER				
		+25		−40 to +85		−40 to +125										
		min.	typ.	max.	min.	max.	min.	max.								
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0						
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0						
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	0 0	V _{CC} or GND				
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 10)			
±I _S	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 10)			
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig. 11)			
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	6.0 10.0	0 0	V _{CC} or GND	V _{IS} = V _{EE} or V _{CC} ; V _{QS} = V _{CC} or V _{EE}			

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS					
		74HC							V _{CC} V	V _{EE} V	OTHER			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t_{PHL}/t_{PLH}	propagation delay V_{IS} to V_{OS}	14 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig. 18)		
t_{PZH}/t_{PZL}	turn "ON" time $E_1; E_2$ to V_{OS}	61 22 18 18	250 50 43 40		315 63 54 50		375 75 64 60		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PZH}/t_{PZL}	turn "ON" time $\bar{E}E$ to V_{OS}	55 20 16 17	200 40 34 40		250 50 43 50		300 60 51 60		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PZH}/t_{PZL}	turn "ON" time S_n to V_{OS}	61 22 18 17	225 45 38 40		280 56 48 50		340 68 58 60		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time $E_1; E_2$ to V_{OS}	66 24 19 19	250 50 43 40		315 63 54 50		375 75 64 60		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time S_n to V_{OS} ; $\bar{E}E$ to V_{OS}	55 20 16 19	200 40 34 40		250 50 43 50		300 60 51 60		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{SU}	set-up time S_n to $\bar{E}E$	60 12 10 18	17 6 5 8		75 15 13 23		90 18 15 27		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		
t_h	hold time S_n to $\bar{E}E$	5 5 5 5	−6 −2 −2 −3		5 5 5 5		5 5 5 5		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		
t_W	$\bar{E}E$ minimum pulse width HIGH	80 16 14 16	11 4 3 6		100 20 17 20		120 24 20 24		ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		

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DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS								
		74HCT							V _{CC} V	V _{EE} V	V _I	OTHER					
		+25		-40 to +85		-40 to +125											
		min.	typ.	max.	min.	max.	min.										
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5							
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5							
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	0	V _{CC} or GND					
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL} = V _{CC} - V _{EE} (see Fig. 10)					
±I _S	analog switch OFF-state current all channels			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL} = V _{CC} - V _{EE} (see Fig. 10)					
±I _S	analog switch ON-state current			0.1		1.0		1.0	μA	10.0	0	V _{IH} or V _{IL} = V _{CC} - V _{EE} (see Fig. 11)					
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V _{CC} or GND	V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE}				
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V _{CC} -2.1 V	other inputs at V _{CC} or GND				

Note to HCT types

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E ₁ , E ₂	0.50
S _n	0.50
LE	1.5

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS					
		74HCT							V _{CC} V	V _{EE} V	OTHER			
		+25		−40 to +85		−40 to +125								
		min.	typ.	max.	min.	max.	min.	max.						
t_{PHL}/t_{PLH}	propagation delay V_{IS} to V_{OS}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig. 18)		
t_{PZH}/t_{PZL}	turn "ON" time \bar{E}_1 to V_{OS}		26 22	55 45		69 56		83 68	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PZH}/t_{PZL}	turn "ON" time E_2 to V_{OS}		22 18	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PZH}/t_{PZL}	turn "ON" time $\bar{L}E$ to V_{OS}		21 17	45 40		56 50		68 60	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PZH}/t_{PZL}	turn "ON" time S_n to V_{OS}		25 19	50 45		63 56		75 68	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E}_1 to V_{OS}		23 19	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time E_2 to V_{OS}		27 23	50 40		63 50		75 60	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time $\bar{L}E$ to V_{OS}		19 19	40 40		50 50		60 60	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{PHZ}/t_{PLZ}	turn "OFF" time S_n to V_{OS}		22 22	45 45		56 56		68 68	ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 19)		
t_{SU}	set-up time S_n to $\bar{L}E$	12 15	7 9		15 19		18 22		ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		
t_h	hold time S_n to $\bar{L}E$	5 5	0 −2		5 5		5 5		ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		
t_W	$\bar{L}E$ minimum pulse width HIGH	16 16	3 5		20 20		24 24		ns	4.5 4.5	0 −4.5	$R_L = 1$ kΩ; $C_L = 50$ pF (see Fig. 20)		

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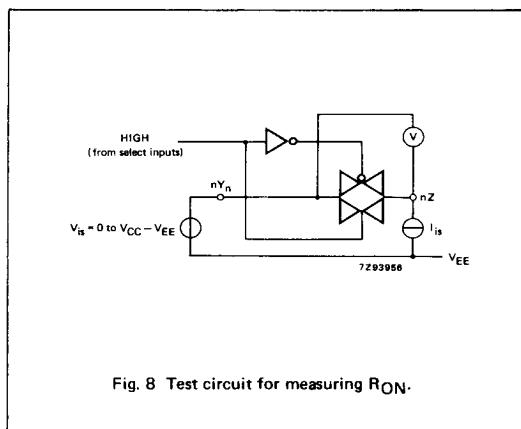


Fig. 8 Test circuit for measuring R_{ON} .

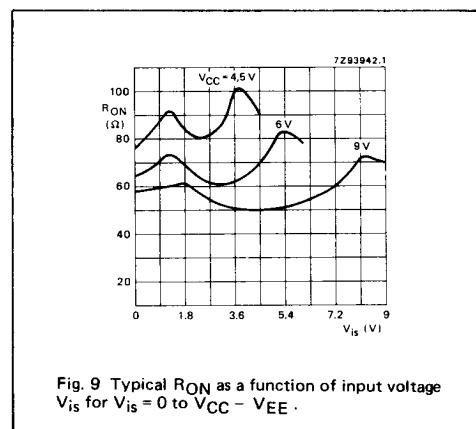


Fig. 9 Typical R_{ON} as a function of input voltage V_{IS} for $V_{IS} = 0$ to $V_{CC} - V_{EE}$.

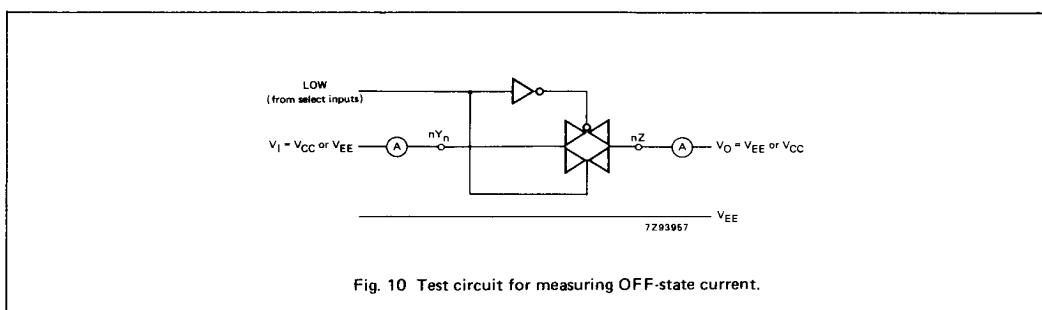


Fig. 10 Test circuit for measuring OFF-state current.

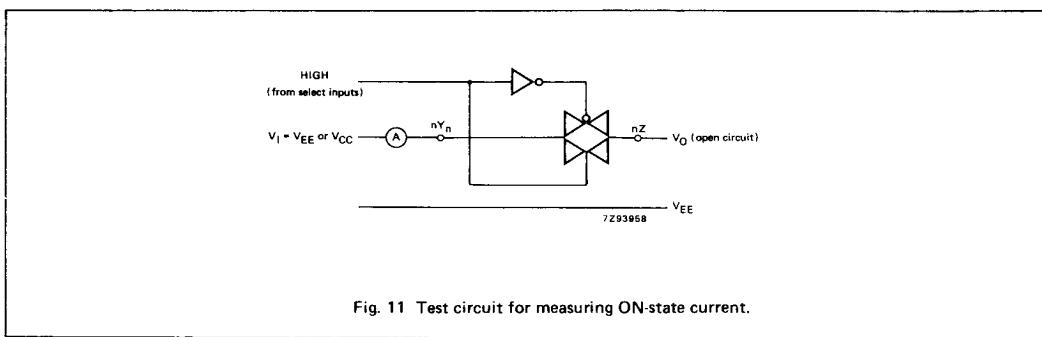


Fig. 11 Test circuit for measuring ON-state current.

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ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} V	V_{EE} V	$V_{IS(p-p)}$ V	CONDITIONS
	sine-wave distortion $f = 1$ kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10$ kΩ; $C_L = 50$ pF (see Fig. 14)
	sine-wave distortion $f = 10$ kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10$ kΩ; $C_L = 50$ pF (see Fig. 14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600$ Ω; $C_L = 50$ pF $f = 1$ MHz (see Figs 12 and 15)
	crosstalk between any two switches/ multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600$ Ω; $C_L = 50$ pF; $f = 1$ MHz (see Fig. 16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600$ Ω; $C_L = 50$ pF; $f = 1$ MHz (E_1, E_2 or S_n , square-wave between V_{CC} and GND, $t_r = t_f = 6$ ns) (see Fig. 17)
f_{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50$ Ω; $C_L = 10$ pF (see Figs 13 and 14)
C_S	maximum switch capacitance independent (Y) common (Z)	5 12	pF pF				

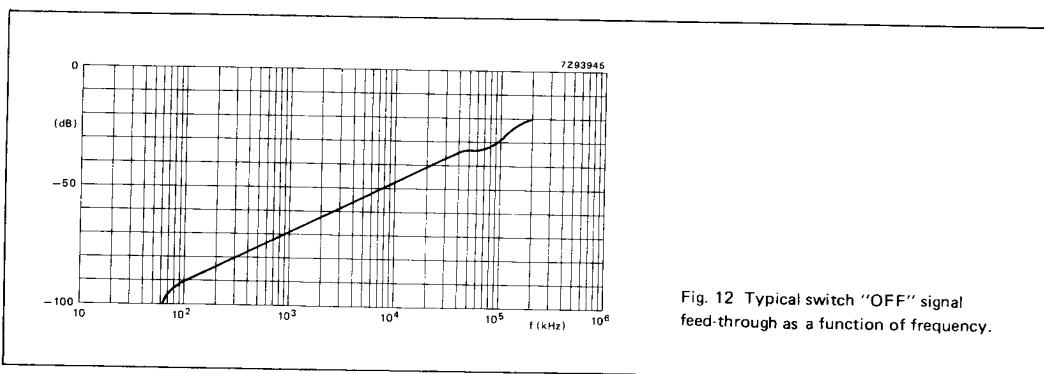
Notes to AC characteristics

General note

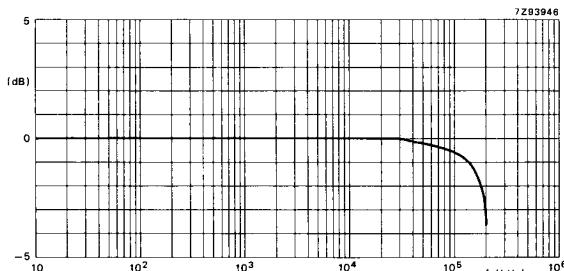
 V_{IS} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input. V_{OS} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{IS} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{IS} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).



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Note to Figs 12 and 13

Test conditions:

$V_{CC} = 4.5 \text{ V}$; GND = 0 V; $V_{EE} = -4.5 \text{ V}$;
 $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

Fig. 13 Typical frequency response.

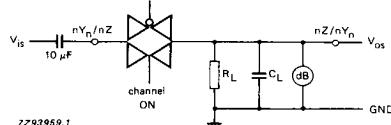


Fig. 14 Test circuit for measuring sine-wave distortion and minimum frequency response.

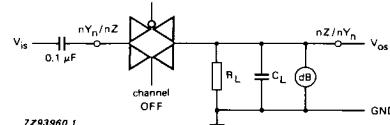


Fig. 15 Test circuit for measuring switch "OFF" signal feed-through.

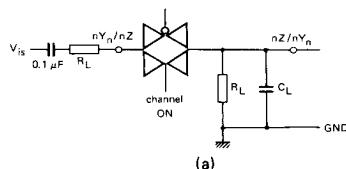
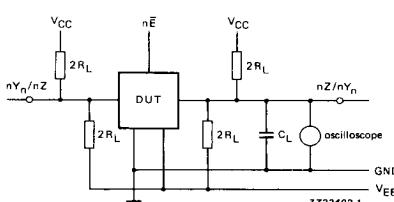
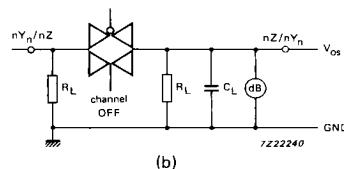
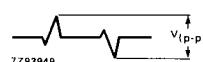
Fig. 16 Test circuits for measuring crosstalk between any two switches/multiplexers.
 (a) channel ON condition; (b) channel OFF condition.

Fig. 17 Test circuit for measuring crosstalk between control and any switch.

Note to Fig. 17

The crosstalk is defined as follows
 (oscilloscope output):

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AC WAVEFORMS

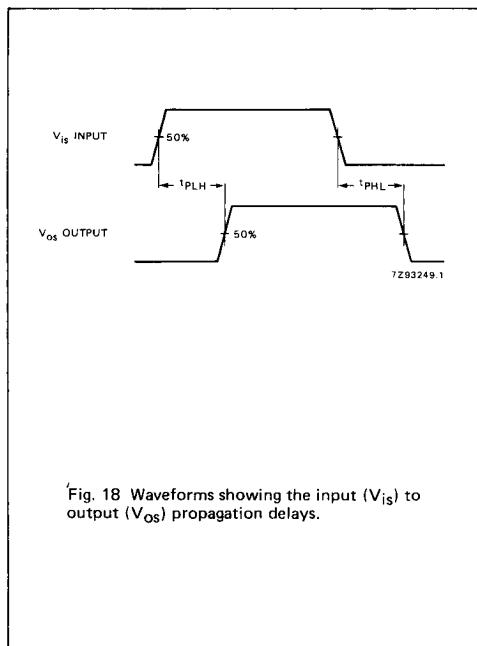


Fig. 18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

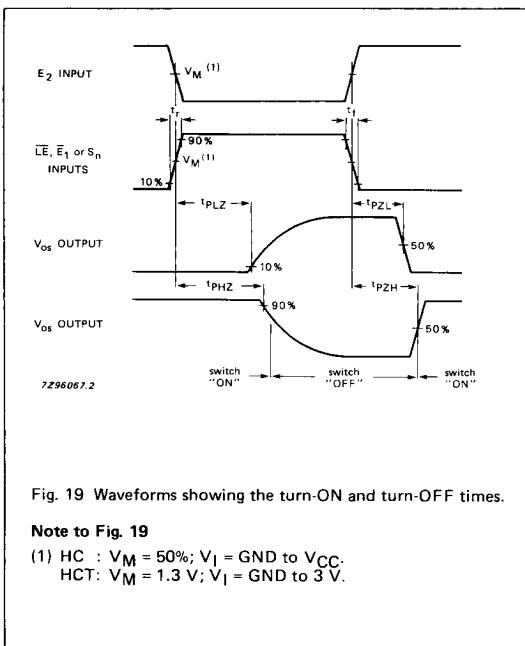


Fig. 19 Waveforms showing the turn-ON and turn-OFF times.

Note to Fig. 19

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

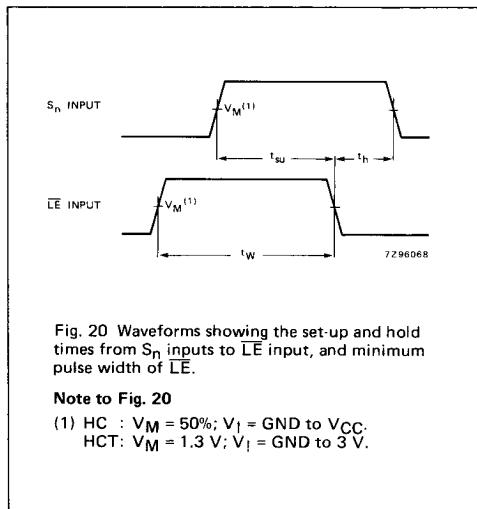


Fig. 20 Waveforms showing the set-up and hold times from S_n inputs to \overline{E} input, and minimum pulse width of \overline{E} .

Note to Fig. 20

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

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TEST CIRCUIT AND WAVEFORMS

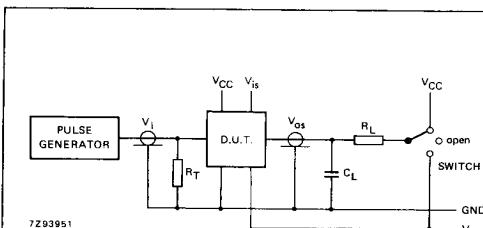


Fig. 21 Test circuit for measuring AC performance.

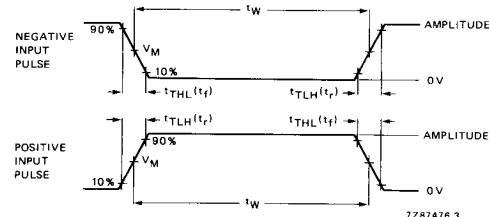


Fig. 22 Input pulse definitions.

Conditions

TEST	SWITCH	V_{IS}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	VM	$t_r; t_f$	
			$f_{max};$ PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Definitions for Figs 21 and 22:

C_L = load capacitance including jig and probe capacitance
(see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint on t_r, t_f with 50% duty factor.