



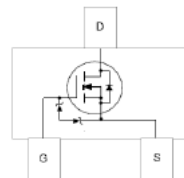
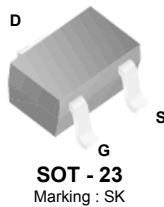
May 2010

BSS138K

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Pb Free/RoHS Compliant
- Green Compound
- ESD HBM=2000V as per JEDEC A114A ; ESD CDM = 2000V as per JEDEC C101C



Absolute Maximum Ratings * $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	50	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current	Continuous Pulsed	A
T_J	Operating Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

* These ratings are limiting values above which the serviceability of any semiconductor device maybe impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Total Device Dissipation Derating above $T_A = 25^\circ\text{C}$	350 2.8	mW mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient *	350	$^\circ\text{C}/\text{W}$

* Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\mu A$	50			V
$\frac{BV_{DSS}}{T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25°C		0.11		$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50V, V_{GS} = 0V$			0.1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 12V, V_{DS} = 0V$ $V_{GS} = \pm 10V, V_{DS} = 0V$ $V_{GS} = \pm 5V, V_{DS} = 0V$			± 1 ± 0.5 ± 0.05	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6		1.2	V
$\frac{V_{GS(th)}}{T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1mA$, Referenced to 25°C		-1.4		$mV/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 1.8V, I_D = 50mA$, $V_{GS} = 2.5V, I_D = 50mA$, $V_{GS} = 5V, I_D = 50mA$,			2.5 2.0 1.6	Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10V, V_{DS} = 5V$	0.2			A
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 200mA$	200			mS
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$		58		pF
C_{oss}	Output Capacitance			9.75		
C_{rss}	Reverse Transfer Capacitance			5.2		
R_G	Gate Resistance	$V_{DS} = 5V, V_{GS} = 10mV$		281		Ω
Switching Characteristics						
$t_{D(on)}$	Turn-On Delay Time	$V_{DD} = 30V, I_D = 0.29A$, $V_{GS} = 10V, R_{GEN} = 6\Omega$			5	ns
t_r	Turn-On Rise Time				5	
$t_{D(off)}$	Turn-Off Delay Time				60	
t_f	Turn-Off Fall Time				35	
Q_g	Total Gate Change	$V_{DS} = 25V, I_D = 0.2A$, $V_{GS} = 10V, I_G = 0.1mA$			2.4	nC
Q_{gs}	Gate-Source Change				0.5	
Q_{gd}	Gate-Drain Change				0.5	
Drain-Source Diode Characteristics and Maximum Ratings						
V_{sd}	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 115mA$			1.2	V

Typical Performance Characteristics

Figure 1. On-Region Characteristics

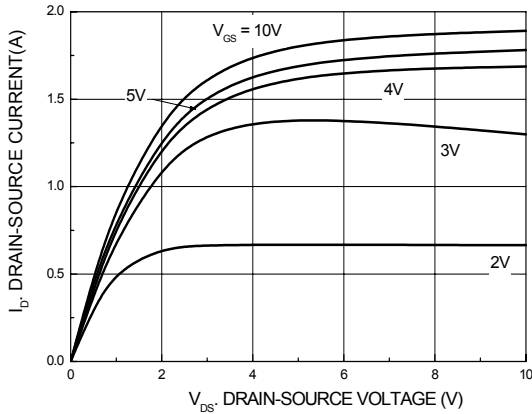


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

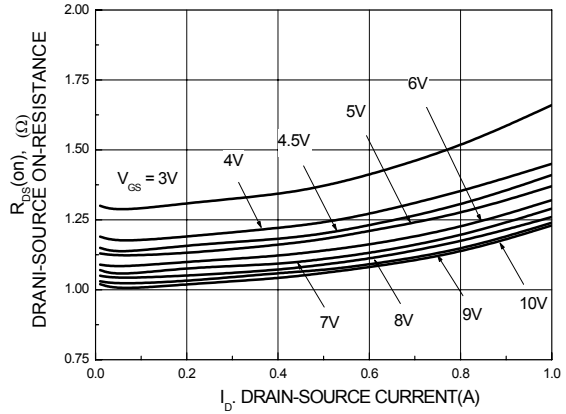


Figure 3. On-Resistance Variation with Temperature

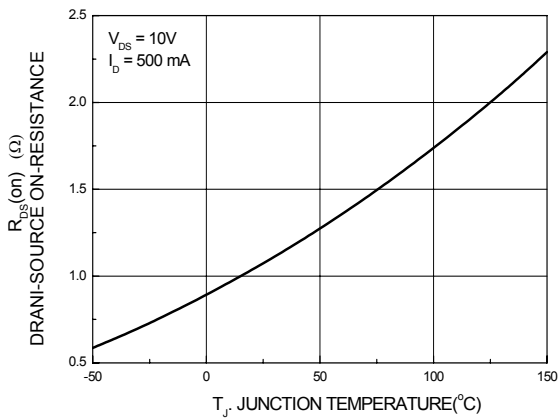


Figure 4. On-Resistance Variation with Gate-Source Voltage

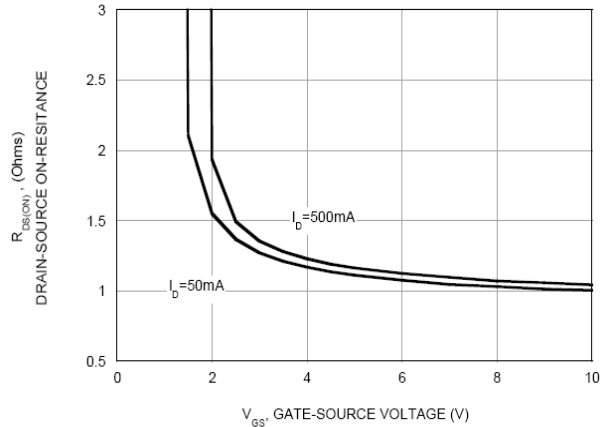


Figure 5. Transfer Characteristics

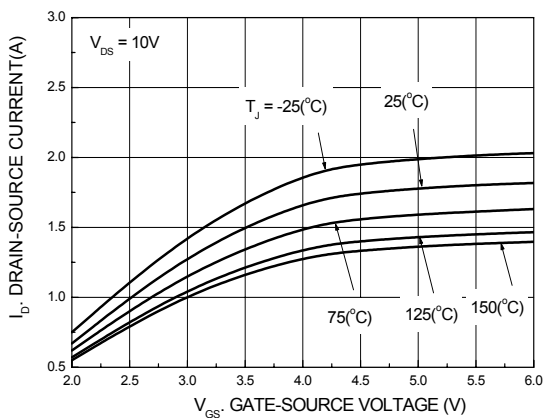
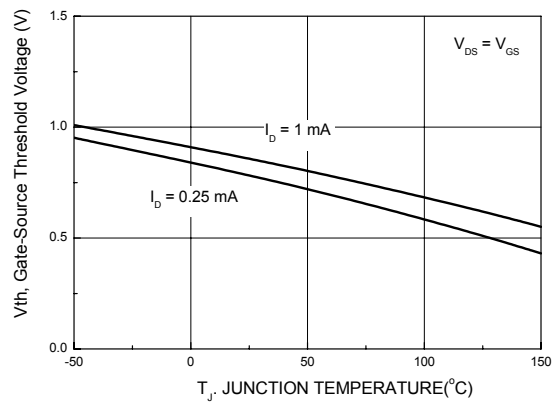
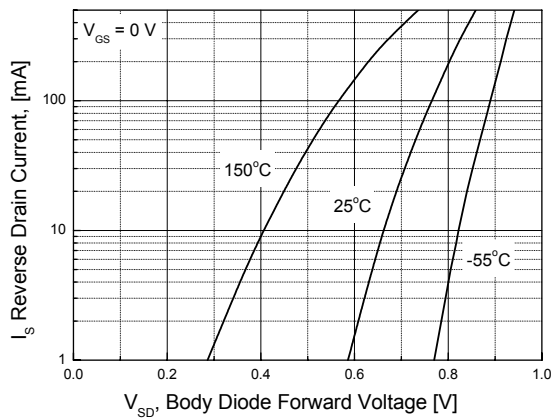


Figure 6. Gate Threshold Variation with Temperature



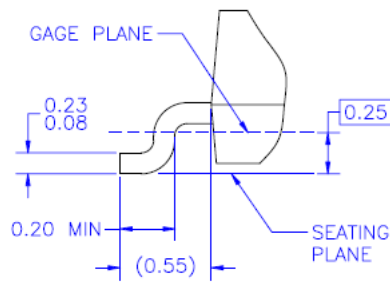
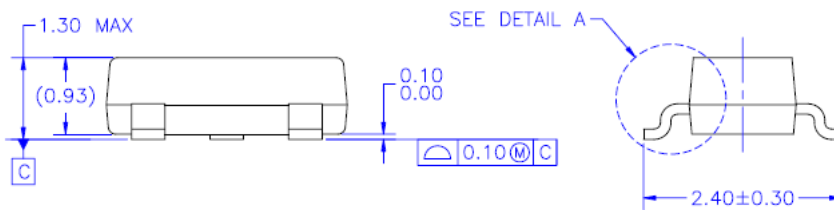
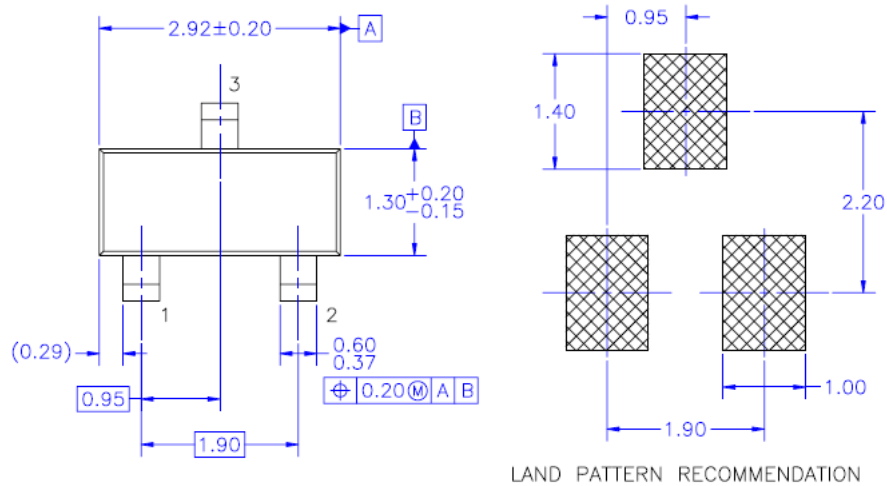
Typical Performance Characteristics (Continue)

Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature



Physical Dimensions

SOT - 23



DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
- E) DRAWING FILE NAME: MA03DREV9



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