REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Add vendor CAGE F8859. Add device class V criteria. Editorial changes throughout. jak	99-11-05	Monica L. Poelking

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS																
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Greg A. Pitz

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
D.A.DiCenzo

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

APPROVED BY
Robert P. Evans

MICROCIRCUIT, DIGITAL, HIGH SPEED CMOS, OCTAL TRANSPARENT D-TYPE LATCHES WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

DRAWING APPROVAL DATE
84-10-17

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
D	A	14933	84072

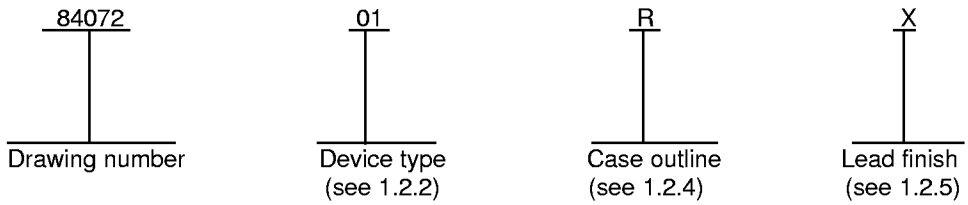
SHEET 1 OF 14

1. SCOPE

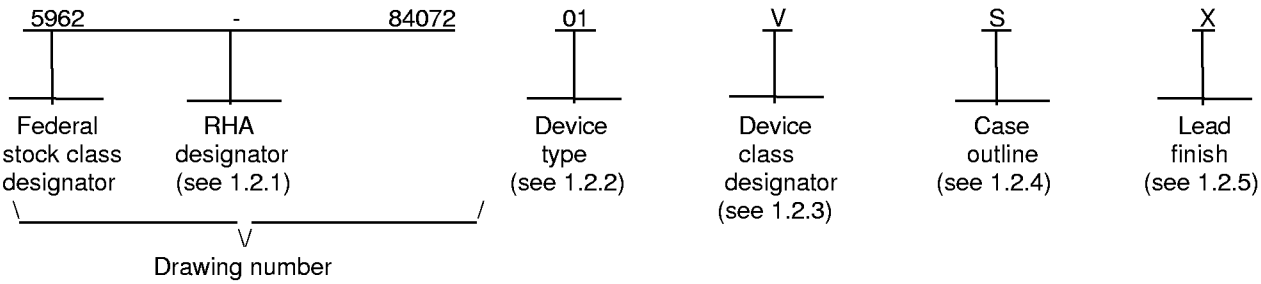
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC373	Octal transparent D-type latches

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current (I_{IK})	±20 mA
DC output diode current (I_{OK}) (per pin)	±35 mA
DC V_{CC} or GND current	±70 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D):	500 mW 4/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 5/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time t_r, t_f):	
VCC = 2.0 V	0 to 1,000 ns
VCC = 4.5 V	0 to 500 ns
VCC = 6.0 V	0 to 400 ns
Minimum setup time, data to enable (t_s):	
T_C = +25°C:	
V_{CC} = 2.0 V	100 ns
V_{CC} = 4.5 V	20 ns
V_{CC} = 6.0 V	17 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	26 ns
Minimum hold time, enable to data (t_h):	
T_C = +25°C:	
V_{CC} = 2.0 V	50 ns
V_{CC} = 4.5 V	10 ns
V_{CC} = 6.0 V	10 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	75 ns
V_{CC} = 4.5 V	15 ns
V_{CC} = 6.0 V	13 ns
Minimum reset clock pulse width (t_w):	
T_C = +25°C:	
V_{CC} = 2.0 V	100 ns
V_{CC} = 4.5 V	20 ns
V_{CC} = 6.0 V	17 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	26 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified VCC range and case temperature range of -55°C to +125°C.
4/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified in figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -6.0$ mA	$V_{CC} = 4.5$ V	1	3.98		
				2, 3	3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -7.8$ mA	$V_{CC} = 6.0$ V	1	5.48		
				2, 3	5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +6.0$ mA	$V_{CC} = 4.5$ V	1		0.26	
				2, 3		0.40	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = +7.8$ mA	$V_{CC} = 6.0$ V	1		0.26	
				2, 3		0.40	
High level input voltage	V_{IH} 2/		$V_{CC} = 2.0$ V	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		
Low level input voltage	V_{IL} 2/		$V_{CC} = 2.0$ V	1, 2, 3		0.3	V
			$V_{CC} = 4.5$ V			0.9	
			$V_{CC} = 6.0$ V			1.2	
Input capacitance	C_{IN}	$V_{IN} = 0.0$ V, $T_C = +25°C$, $V_{CC} = 2.0$ V to 6.0 V, See 4.4.1c		4		10.0	pF
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 6.0$ V $I_{OUT} = 0.0$ A		1		8.0	µA
				2, 3		160.0	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND		1		±100.0	nA
				2, 3		±1000.0	
Three-state output Leakage current	I_{OZ}	$V_{CC} = 6.0$ V, $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		1		±0.5	µA
				2, 3		±10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Power dissipation capacitance	C_{PD}	See 4.4.1c		4		100.0	pF
Functional tests		See 4.4.1b		7, 8			
Propagation delay time, data to output, Dn to Qn	t_{PHL1} t_{PLH1} 3/	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C and +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10, 11		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	
Propagation delay time, latch enable to any output, LE to Qn	t_{PHL2} t_{PLH2} 3/	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		T_C = -55°C and +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10, 11		265	ns
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	
Propagation delay time, output enable to any output, $\overline{OE}$ to Qn	t_{PZH} t_{PZL} 3/	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C and +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10, 11		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, output disable to any output, OE to Qn	t_{PHZ} t_{PLZ} 3/	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C and +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10, 11		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	
Transition time, output rise and fall	t_{THL} t_{TLH} 4/	T_C = +25°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		60	ns
			V_{CC} = 4.5 V			12	
			V_{CC} = 6.0 V			10	
		T_C = -55°C and +125°C C_L = 50 pF See figure 4	V_{CC} = 2.0 V	10, 11		90	ns
			V_{CC} = 4.5 V			18	
			V_{CC} = 6.0 V			15	

1/ For a power supply of 5 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage, so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 100 pF per latch, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.
2/ The V_{IH} and V_{IL} tests are not required because they are used as forcing functions for V_{OH} or V_{OL}.
3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limits in table I.
4/ Transition time (t_{TLH}, t_{THL}), if not tested, shall be guaranteed to the specified limits in table I.

Device type	01
Case Outline	R, S and 2
Terminal Number	Terminal Symbol
1	$\overline{OE}$
2	Q0
3	D0
4	D1
5	Q1
6	Q2
7	D2
8	D3
9	Q3
10	GND
11	LE
12	Q4
13	D4
14	D5
15	Q5
16	Q6
17	D6
18	D7
19	Q7
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs			Outputs
$\overline{OE}$	LE	Dn	Qn
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

H = High voltage level.
L = Low voltage level.
X = Irrelevant.
Z = High impedance
Q0 = The level of output before the steady-state input conditions were established

FIGURE 2. Truth table.

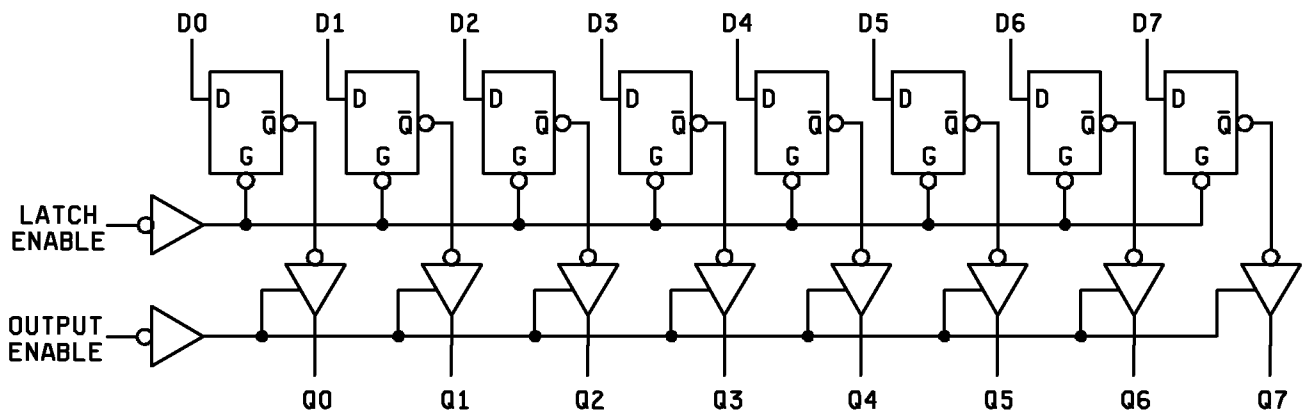
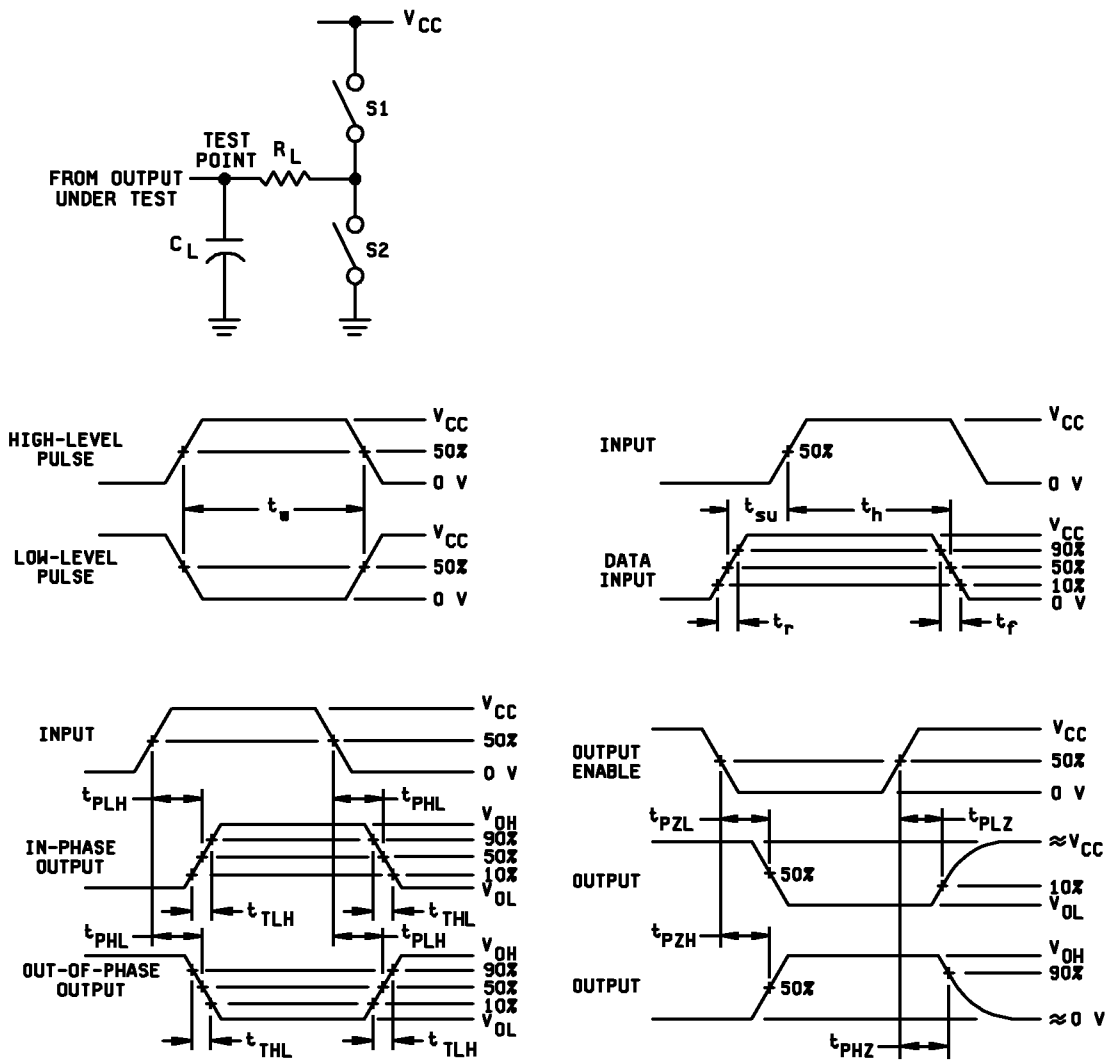


FIGURE 3. Logic diagram.



NOTES:

1. t_{PLH} and t_{PHL}: S1 and S2 = open
   t_{TLH} and t_{THL}: S1 and S2 = open
   t_{PZH} and t_{PLZ}: S1 = open and S2 = closed
   t_{PZL} and t_{PLZ}: S2 = closed and S2 = open
2. R_L = 1 kΩ.
3. C_L includes probe and test fixture capacitance.
4. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
5. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50Ω, t_r = 6.0 ns, t_f = 6.0 ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1, 2, 3, 7 1/	1/ 1, 2, 3, 7,	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 9, 10, 11 2/	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN
DATE: 99-11-05

Approved sources of supply for SMD 84072 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8407201RA	01295	CD54HC373F3A
	01295	SNJ54HC373J
8407201SA	01295	SNJ54HC373W
	F8859	54HC373K02Q
8407201SC	F8859	54HC373K01Q
84072012A	01295	SNJ54HC373FK
5962-8407201VSA	F8859	54HC373K02V
5962-8407201VSC	F8859	54HC373K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: 6412 Highway 75 South Sherman, TX 75090-0084
F8859	STMicroelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2-FRANCE