Dual, 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter

FEATURES

- ±1LSB INL
- 2.5V to 5.5V Supply Operation
- Fast Parallel Interface: 17ns Write Cycle
- Update Rate of 20.4MSPS
- 10MHz Multiplying Bandwidth
- ±15V Reference Input
- Extended Temperature Range: –40°C to +125°C
- 40-Lead QFN
- 12-Bit Monotonic
- 4-Quadrant Multiplication
- Power-On Reset with Brownout Detection
- Readback Function
- Industry-Standard Pin Configuration
- Pin-Compatible with the AD5405

APPLICATIONS

- Portable Battery-Powered Instruments
- Waveform Generators
- Analog Processing
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Calibration
- Programmable Filters and Oscillators
- Ultrasound

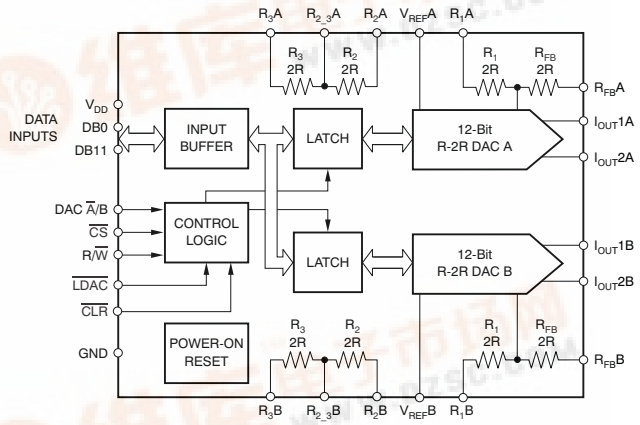
DESCRIPTION

The DAC7822 is a dual, CMOS, 12-bit, current output digital-to-analog converter (DAC). This device operates from a 2.5V to 5.5V power supply, making it suitable for battery-powered and many other applications.

The DAC7822 operates with a fast parallel interface. Data readback allows the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeroes and the DAC outputs are at zero scale.

The DAC7822 offers excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidth of 10MHz. The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external current-to-voltage precision amplifier. The DAC7822 also includes the resistors necessary for 4-quadrant multiplication and other configuration modes.

The DAC7822 is available in a 40-lead QFN package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7822	40-QFN	RTA	–40°C to +125°C	DAC7822	DAC7822IRTAT	250, Tape and Reel
					DAC7822IRTAR	2000, Tape and Reel

(1) For the most current specifications and package information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	DAC7822	UNIT
V_{DD} to GND	–0.3 to +7.0	V
Digital input voltage to GND	–0.3 to V_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to V_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature (T_J max)	+150	°C
ESD Rating, HBM	2000	V
ESD Rating, CDM	1000	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

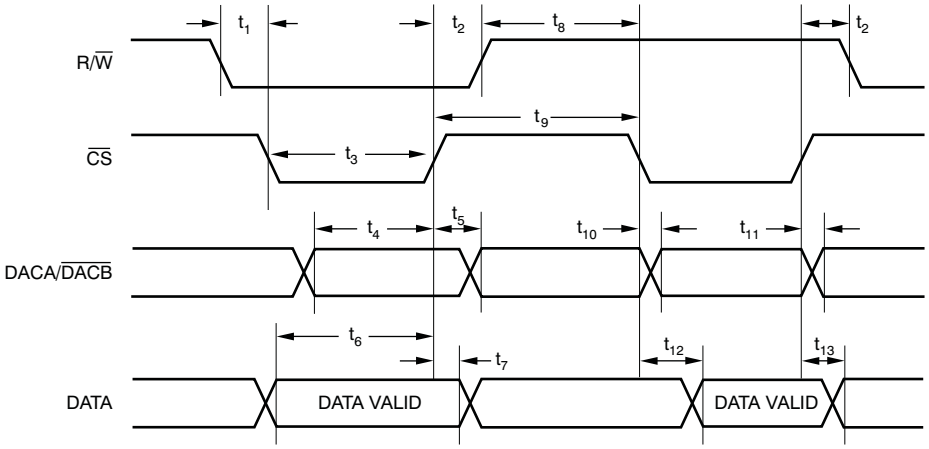
ELECTRICAL CHARACTERISTICS

V_{DD} = +2.5V to +5.5V; $I_{OUT}1$ = Virtual GND; $I_{OUT}2$ = 0V; V_{REF} = 10V; T_A = full operating temperature. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER		CONDITIONS	DAC7822 MIN	DAC7822 TYP	DAC7822 MAX	UNITS
STATIC PERFORMANCE						
Resolution			12			Bits
Relative accuracy					±1	LSB
Differential nonlinearity					±1	LSB
Output leakage current		Data = 000h, T_A = +25°C			±1	nA
Output leakage current		Data = 000h, T_A = T_{MAX}			±15	nA
Full-scale gain error		All ones loaded to DAC register		±10	±25	mV
Full-scale tempco(1)				±5		ppm/°C
Bipolar zero-code error		Circuit configuration as shown in Figure 41			±25	mV
Output capacitance		DAC latches leaded with all 1s		25	30	pF
REFERENCE INPUT						
V_{REF} range			–15		15	V
$V_{REF}A$, $V_{REF}B$, Input resistance			8	10	12	kΩ
R_1, R_{FB} resistance			17	20	25	kΩ
R_2, R_3 resistance			17	20	25	kΩ
$V_{REF}A$ to $V_{REF}B$ Input Mismatch				1.6	2.5	%
R_2 to R_3 Mismatch				0.06	0.18	%
LOGIC INPUTS AND OUTPUT(1)						
Input low voltage	V_{IL}	V_{DD} = +2.5V			0.6	V
		V_{DD} = +5V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.5V	2.1			V
		V_{DD} = +5V	2.4			V
Input leakage current	I_{IL}				1	µA
Input capacitance	C_{IL}				10	pF
POWER REQUIREMENTS						
V_{DD}			2.5		5.5	V
I_{DD} (normal operation)		Logic inputs = 0V			5	µA
V_{DD} = +4.5V to +5.5V		V_{IH} = V_{DD} and V_{IL} = GND		0.8	5	µA
V_{DD} = +2.5V to +3.6V		V_{IH} = V_{DD} and V_{IL} = GND		0.4	2.5	µA
AC CHARACTERISTICS(1)						
Output voltage settling time					0.2	µs
Reference multiplying BW		V_{REF} = $7V_{PP}$, Data = FFFh		10		MHz
DAC glitch impulse		V_{REF} = 0V to 10V, Data = 7FFh to 800h to 7FFh		10		nV-s
Feedthrough error V_{OUT}/V_{REF}		Data = 000h, V_{REF} = 100kHz		–70		dB
Digital feedthrough				2		nV-s
Total harmonic distortion				–105		dB
Output spot noise voltage				25		nV/√Hz

(1) Specified by design and characterization; not production tested.

TIMING INFORMATION



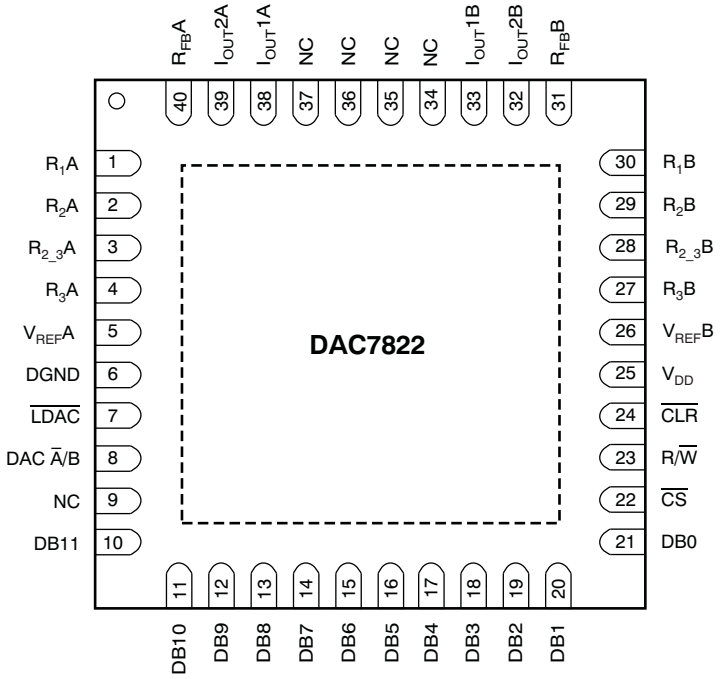
TIMING REQUIREMENTS: 2.5 V to 5.5 V

At $t_r = t_f$ = 1ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; V_{DD} = 2.5V to 5.5V, V_{REF} = 10V, $I_{OUT}2$ = 0V. All specifications –40°C to +125°C, unless otherwise noted.

PARAMETER(1)	TEST CONDITIONS	DAC7822			UNIT
		MIN	TYP	MAX	
t_1	R/$\overline{W}$ to $\overline{CS}$ setup time	0			ns
t_2	R/$\overline{W}$ to $\overline{CS}$ hold time	0			ns
t_3	$\overline{CS}$ low time (write cycle)	10			ns
t_4	Address setup time	10			ns
t_5	Address hold time	0			ns
t_6	Data setup time	6			ns
t_7	Data hold time	0			ns
t_8	R/$\overline{W}$ high to $\overline{CS}$ low	5			ns
t_9	$\overline{CS}$ minimum high time	7			ns
t_{10}	Address setup time (Read Cycle)	0			ns
t_{11}	Address hold time (Read Cycle)	0			ns
t_{12}	Data access time		5	35	ns
t_{13}	Bus relinquish time		5	10	ns

(1) Ensured by design; not production tested.

DEVICE INFORMATION



TERMINAL FUNCTIONS

PIN NO.	PIN NAME	DESCRIPTION
1-4	R_1A, R_2A, $R_{2\_3}A$, R_3A	DAC A 4-Quadrant Resistors. Allows a number of configuration modes, including bipolar operation with minimum of external components.
5, 26	$V_{REF}A$, $V_{REF}B$	DAC Reference Voltage Input Terminals.
6	DGND	Digital Ground Pin.
7	$\overline{LDAC}$	Load DAC Input. Allows asynchronous or synchronous updates to the DAC output. The DAC is asynchronously updated when this signal goes low. Alternatively, if this line is held permanently low, an automatic or synchronous update mode is selected whereby the DAC is updated on the rising edge of $\overline{CS}$.
8	DAC $\overline{A}$/B	Selects DAC A or B. Low selects DAC A, and high selects DAC B.
9, 34-37	NC	Not internally connected.
10-21	DB11 to DB0	Parallel Data Bits 11 through 0.
22	$\overline{CS}$	Chip Select Input; active low. Used in conjuction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Edge sensitive; when pulled high, the DAC data is latched.
23	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, used in conjunction with $\overline{CS}$ to read back contents of DAC register.
24	$\overline{CLR}$	Active Low Control Input. Clears DAC output and input and DAC registers.
25	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5V to 5.5V.
27-30	R_3B, $R_{2\_3}B$, R_2B, R_1B	DAC B 4-Quadrant Resistors. Allow a number of configuration modes, including bipolar operation with a minimum of external components.
31, 40	$R_{FB}B$, $R_{FB}A$	External Amplifier Output.
32	$I_{OUT}2B$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.
33	$I_{OUT}1B$	DAC B Current Output.
38	$I_{OUT}1A$	DAC A Current Output.
39	$I_{OUT}2A$	DAC A Analog Ground. This pin typically should be tied to the analog ground of the system, but can be biased to achieve single-supply operation.

TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

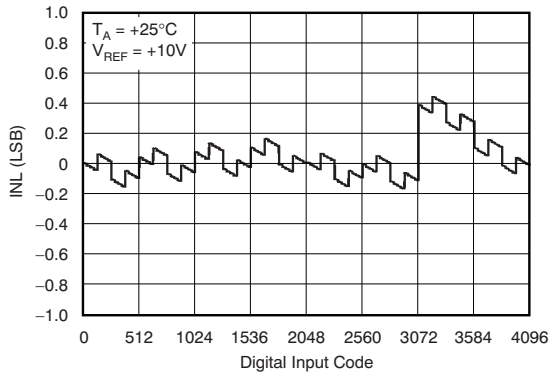


Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

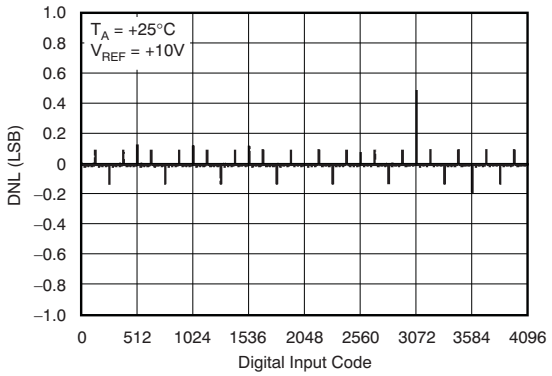


Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

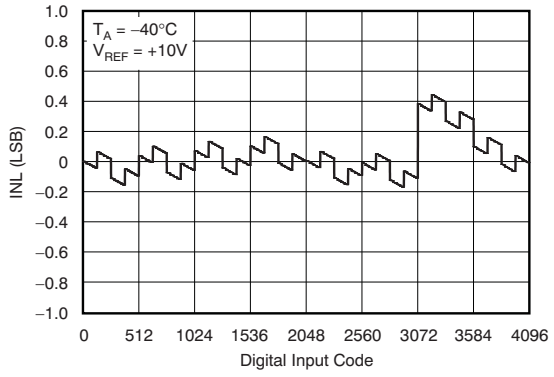


Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

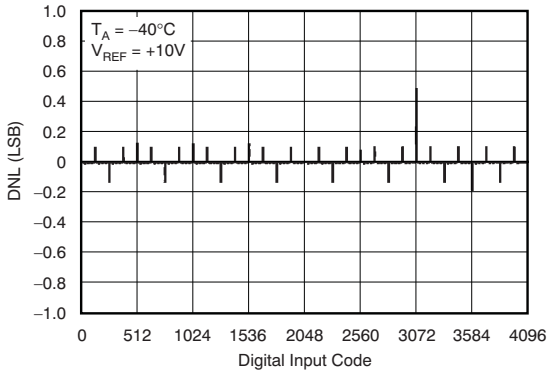


Figure 4.

LINEARITY ERROR vs DIGITAL INPUT CODE

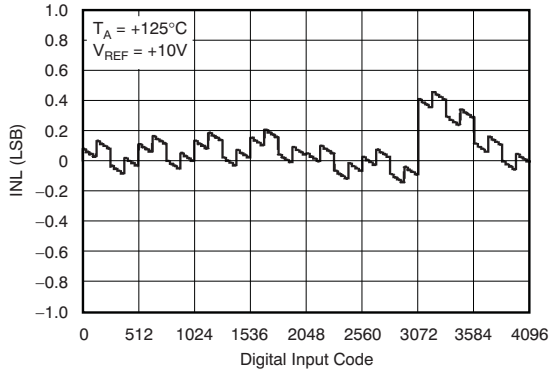


Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

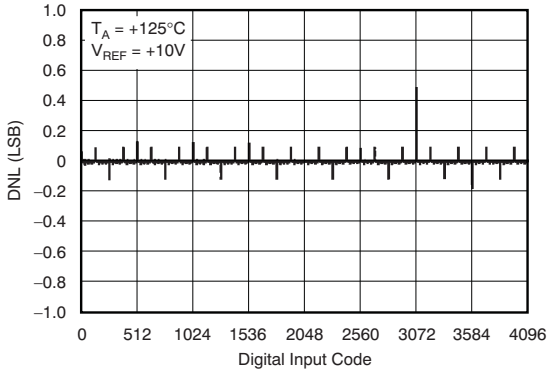


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

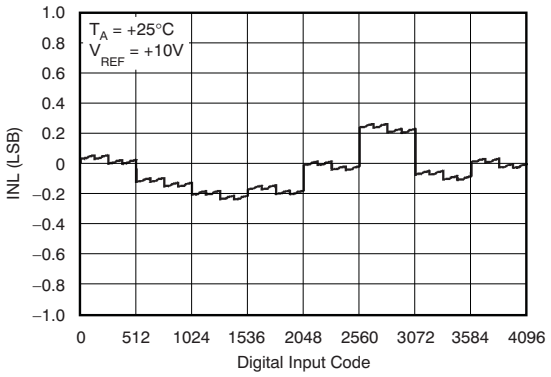


Figure 7.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

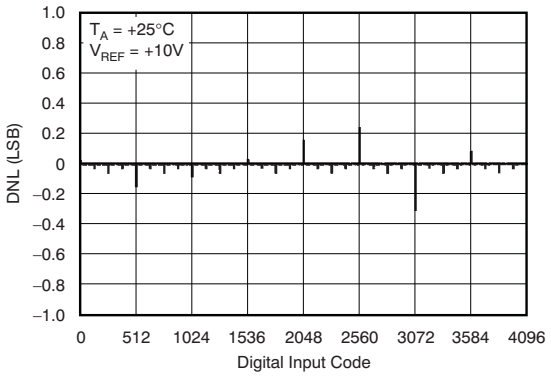


Figure 8.

LINEARITY ERROR vs DIGITAL INPUT CODE

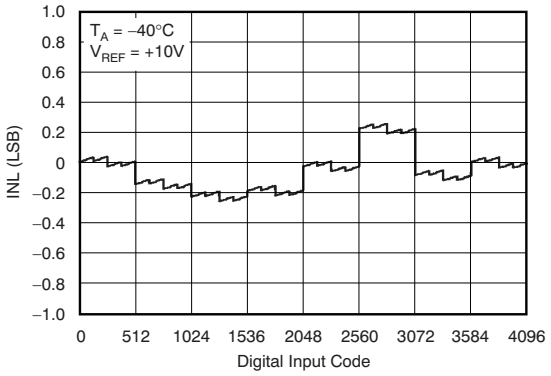


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

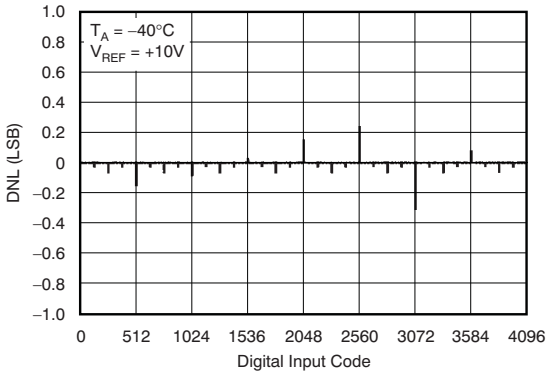


Figure 10.

LINEARITY ERROR vs DIGITAL INPUT CODE

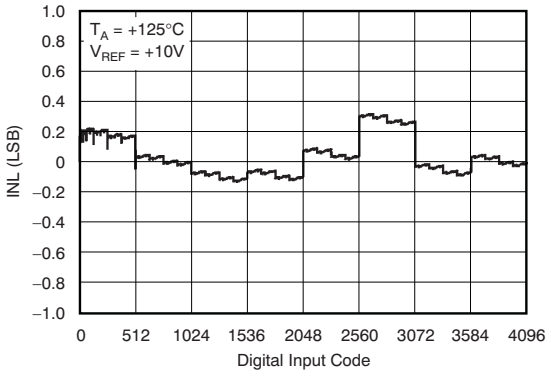


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

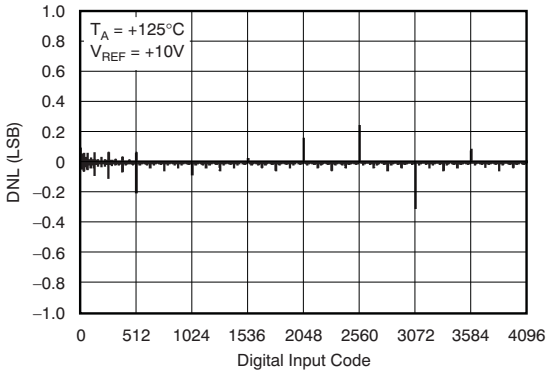


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, +V_{DD} = +5V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

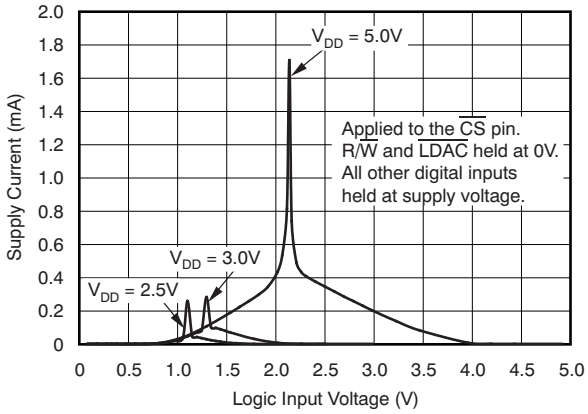


Figure 13.

REFERENCE MULTIPLYING BANDWIDTH

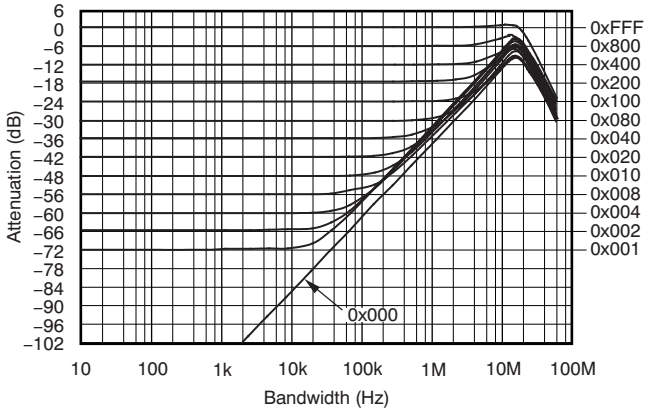


Figure 14.

MIDSCALE DAC GLITCH

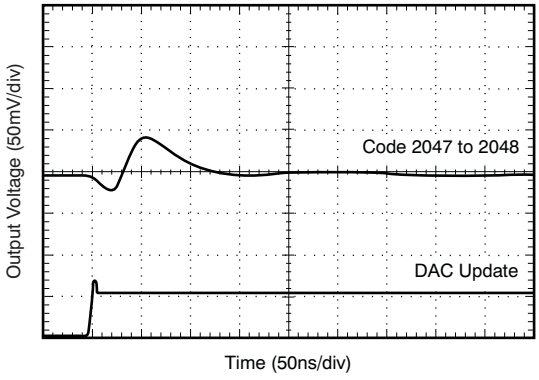


Figure 15.

MIDSCALE DAC GLITCH

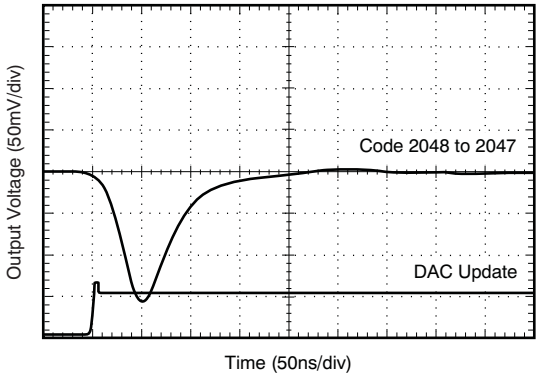


Figure 16.

DAC SETTLING TIME

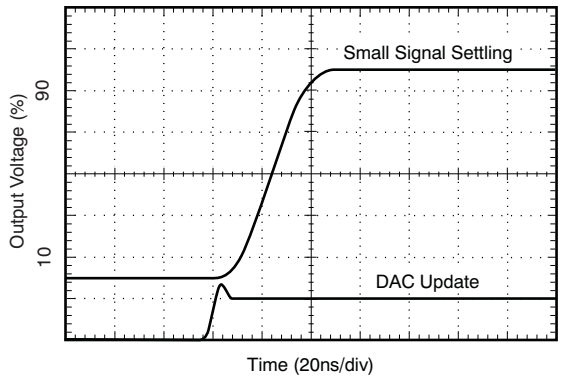


Figure 17.

GAIN ERROR vs TEMPERATURE

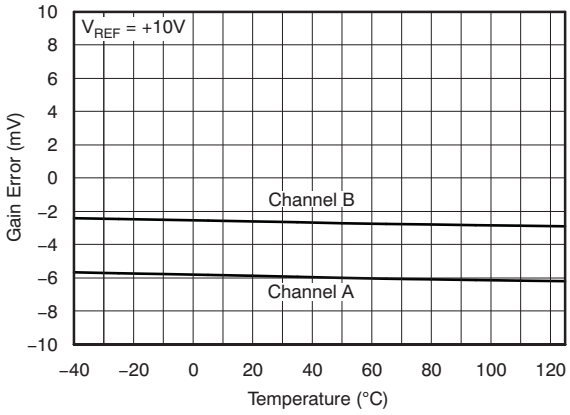


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE

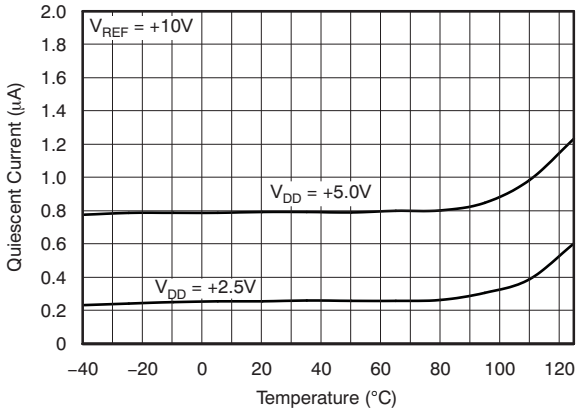


Figure 19.

OUTPUT LEAKAGE vs TEMPERATURE

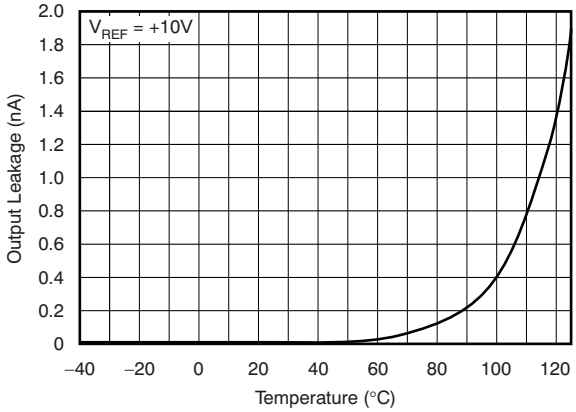


Figure 20.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V

At T_A = +25°C, +V_{DD} = +2.5V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

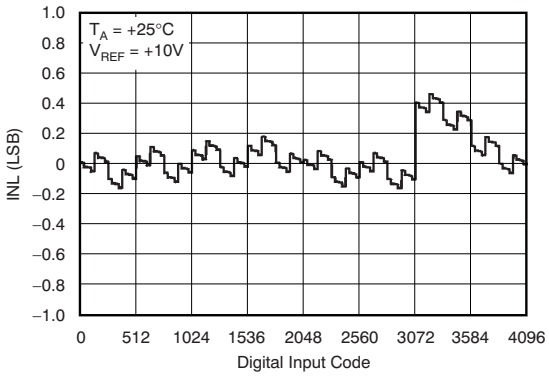


Figure 21.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

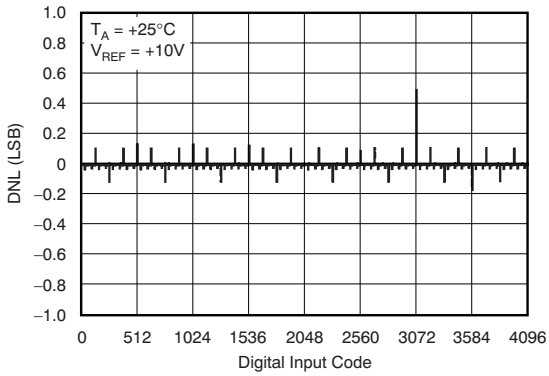


Figure 22.

LINEARITY ERROR vs DIGITAL INPUT CODE

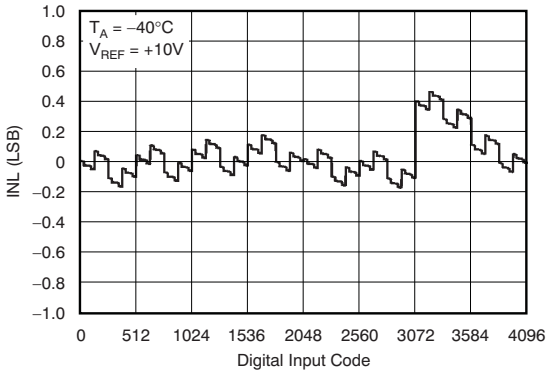


Figure 23.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

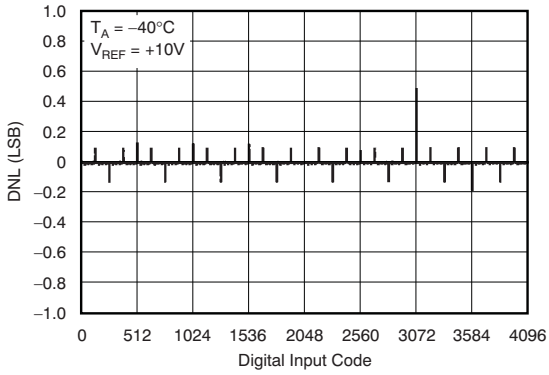


Figure 24.

LINEARITY ERROR vs DIGITAL INPUT CODE

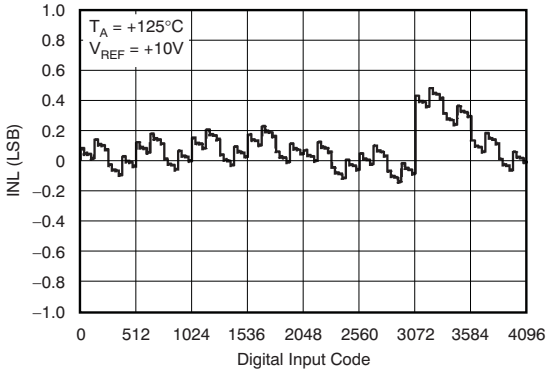


Figure 25.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

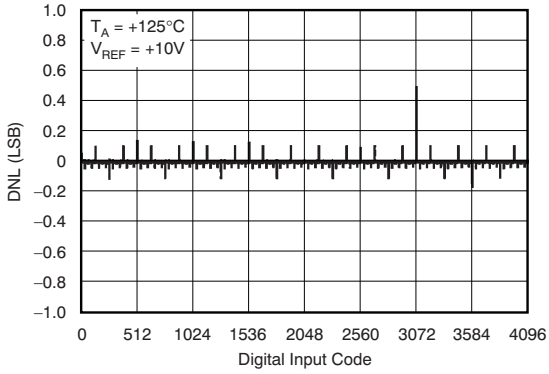


Figure 26.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At T_A = +25°C, +V_{DD} = +2.5V, unless otherwise noted.

Channel B

LINEARITY ERROR
vs DIGITAL INPUT CODE

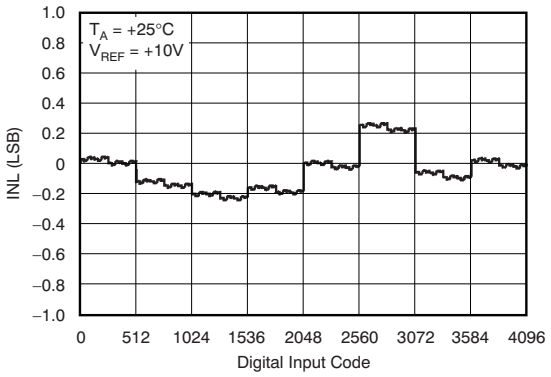


Figure 27.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

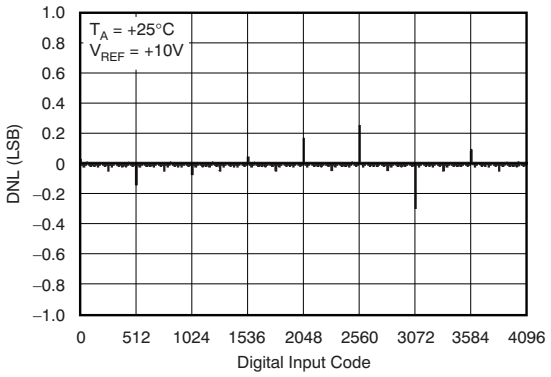


Figure 28.

LINEARITY ERROR
vs DIGITAL INPUT CODE

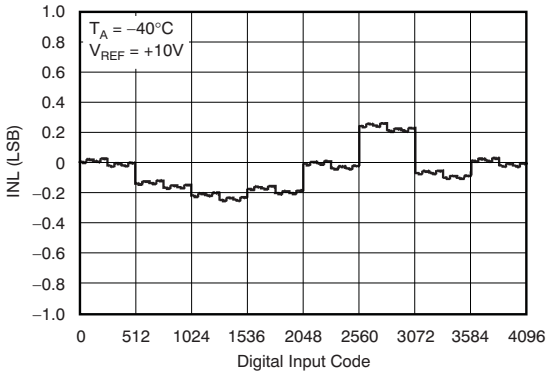


Figure 29.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

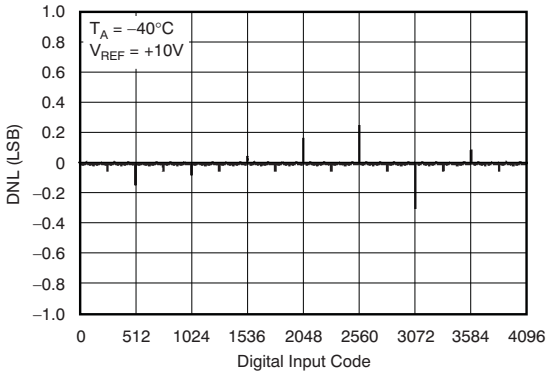


Figure 30.

LINEARITY ERROR
vs DIGITAL INPUT CODE

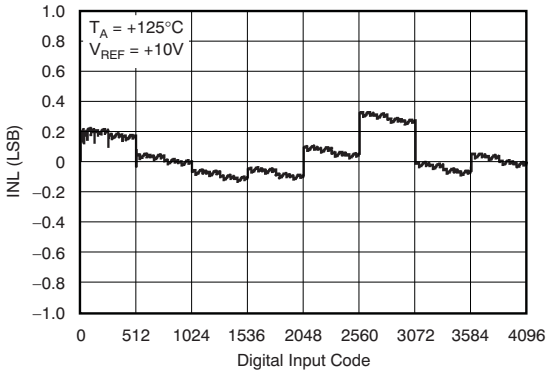


Figure 31.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

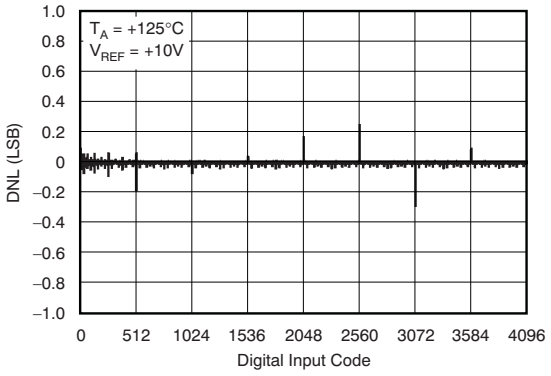


Figure 32.

TYPICAL CHARACTERISTICS: V_{DD} = +2.5V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.5V, unless otherwise noted.

MIDSCALE DAC GLITCH

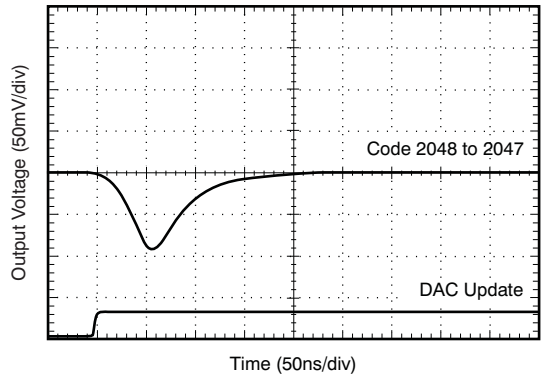


Figure 33.

MIDSCALE DAC GLITCH

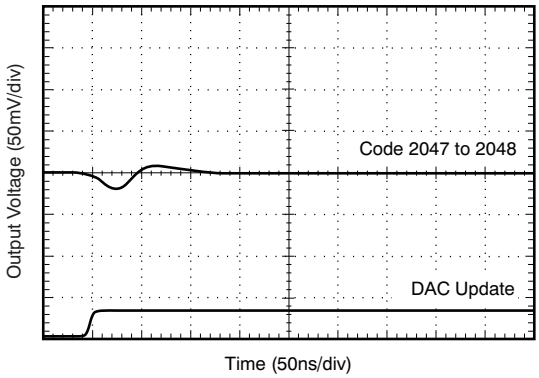


Figure 34.

GAIN ERROR vs TEMPERATURE

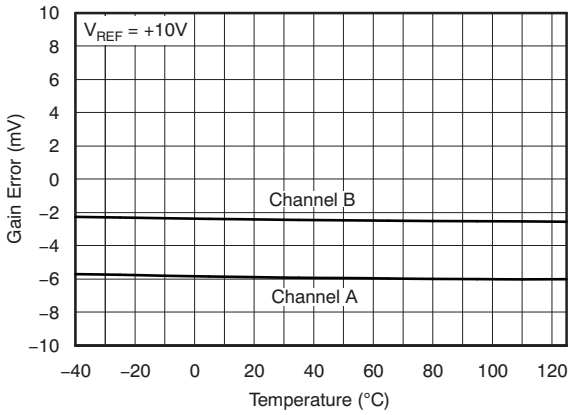


Figure 35.

OUTPUT LEAKAGE vs TEMPERATURE

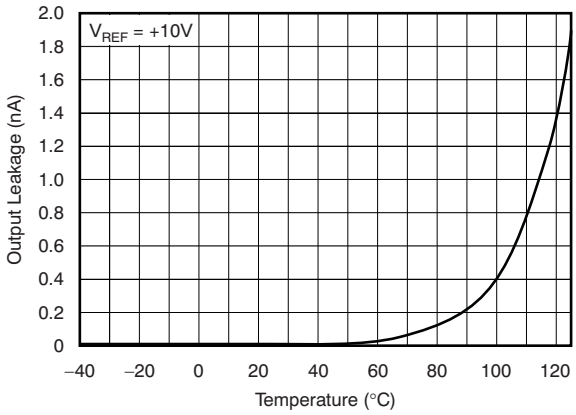


Figure 36.

THEORY OF OPERATION

The DAC7822 is a dual channel, current output, 12-bit, digital-to-analog converter (DAC). The architecture, illustrated in Figure 37, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to $I_{OUT}1$ or the $I_{OUT}2$ terminal. The $I_{OUT}1$ terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code-independent load impedance to the external reference of 10kΩ ±20%. The external reference voltage can vary over a range of –15V to +15V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC7822 R_{FB} resistor, output voltage ranges of $–V_{REF}$ to V_{REF} can be generated.

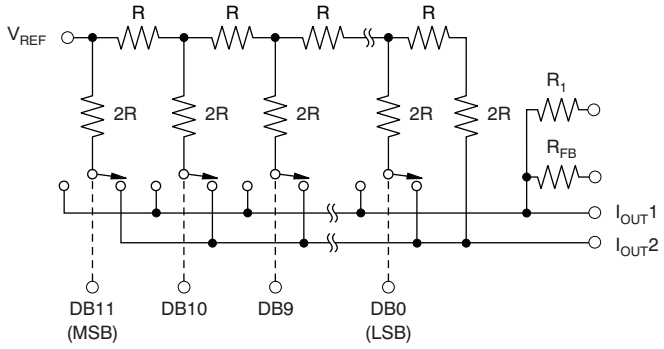


Figure 37. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC7822 R_{FB} and R_1 resistors, the DAC output voltage is given by Equation 1:

$$V_{OUT} = - V_{REF} \times \frac{CODE}{4096} \quad (1)$$

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the $I_{OUT}1$ terminal changes versus code, the external I/V converter noise gain also changes. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC $I_{OUT}1$ terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC7822 as a result of offset modulation versus DAC code.

For best linearity performance of the DAC7822, a low input offset voltage op amp (such as the OPA277) is recommended (see Figure 38). This circuit allows V_{REF} swinging from –10V to +10V.

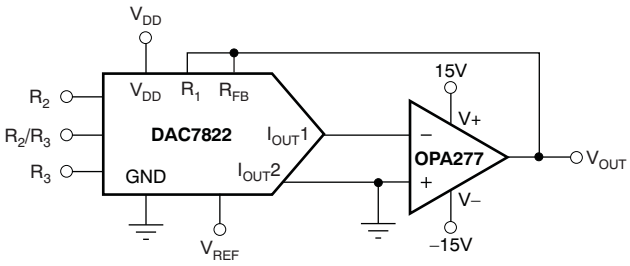


Figure 38. Voltage Output Configuration

APPLICATION INFORMATION

Stability Circuit

For a current-to-voltage design (see Figure 39), the DAC7822 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct printed circuit board (PCB) layout design. For each code change, there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C_1 (1pF to 5pF typ) can be added to the design, as shown in Figure 39.

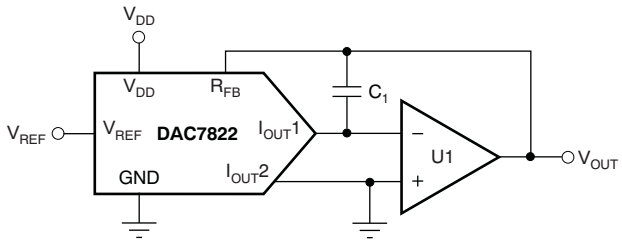


Figure 39. Gain Peaking Prevention Circuit with Compensation Capacitor

Positive Voltage Output Circuit

As Figure 40 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC7822. This design is suggested instead of using an inverting amp to invert the output as a result of resistor tolerance errors. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a –2.5V input to the DAC7822 with an op amp.

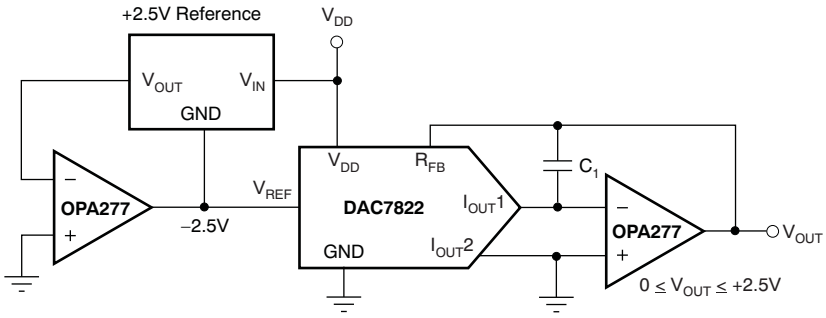


Figure 40. Positive Voltage Output Circuit

Bipolar Output Section

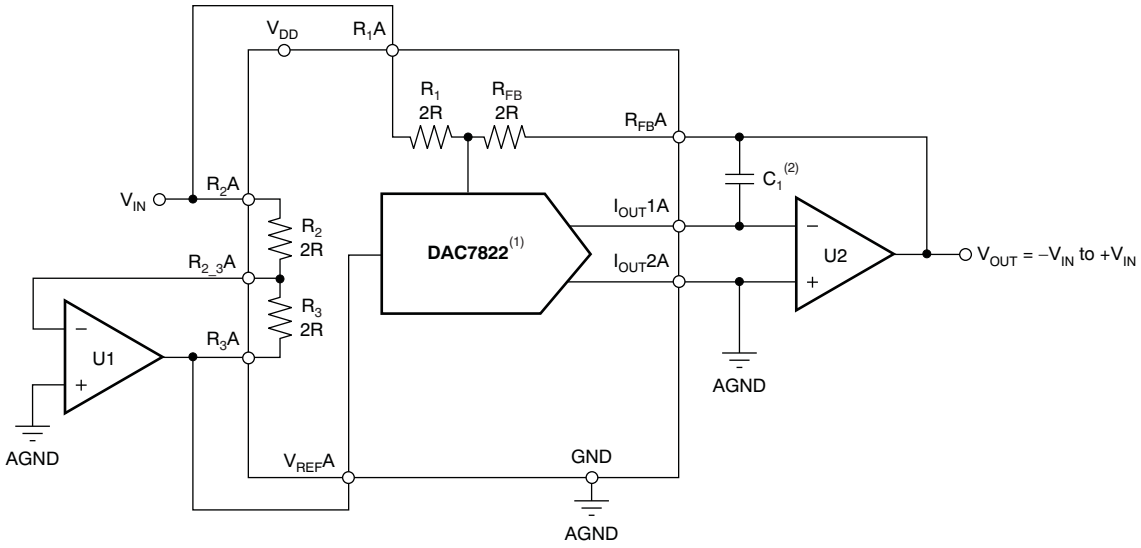
The DAC7822, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 41, external op amp U2 is added as a summing amp and has a gain of 2X that widens the output span to 5V. A 4-quadrant multiplying circuit is implemented by using a 2.5V offset of the reference voltage to bias U2. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full-scale produces output voltages of V_{OUT} = –2.5V to V_{OUT} = +2.5V.

$$V_{OUT} = \left(\frac{D}{0.5 \times 2^N} - 1 \right) \times V_{REF} \quad (2)$$

APPLICATION INFORMATION (continued)

External resistance mismatching is the significant error in Figure 41.



NOTES: (1) Similar configuration for DAC B.
(2) C_1 phase compensation (1pF to 5pF) may be required if U2 is a high-speed amplifier.

Figure 41. Bipolar Output Circuit

Parallel Interface

Data is loaded to the DAC7822 as a 12-bit parallel word. The bi-directional bus is controlled with $\overline{CS}$ and R/$\overline{W}$, allowing data to be written to or read from the DAC register. To write to the device, $\overline{CS}$ and R/$\overline{W}$ are brought low, and data available on the data lines fills the input register. The rising edge of $\overline{CS}$ latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent; therefore, a write sequence must consist of a falling and rising edge on $\overline{CS}$ in order to ensure that data is loaded to the DAC register and its analog equivalent is reflected on the DAC output.

To read data stored in the device, R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Data is loaded from the DAC register back to the input register and out onto the data line, where it can be read back to the controller.

Cross-Reference

The DAC7822 has an industry-standard pinout. Table 1 provides the cross-reference information.

Table 1. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC7822	±1	±1	–40°C to +125°C	40-Lead QFN	QFN-40	AD5405

PACKAGING INFORMATION

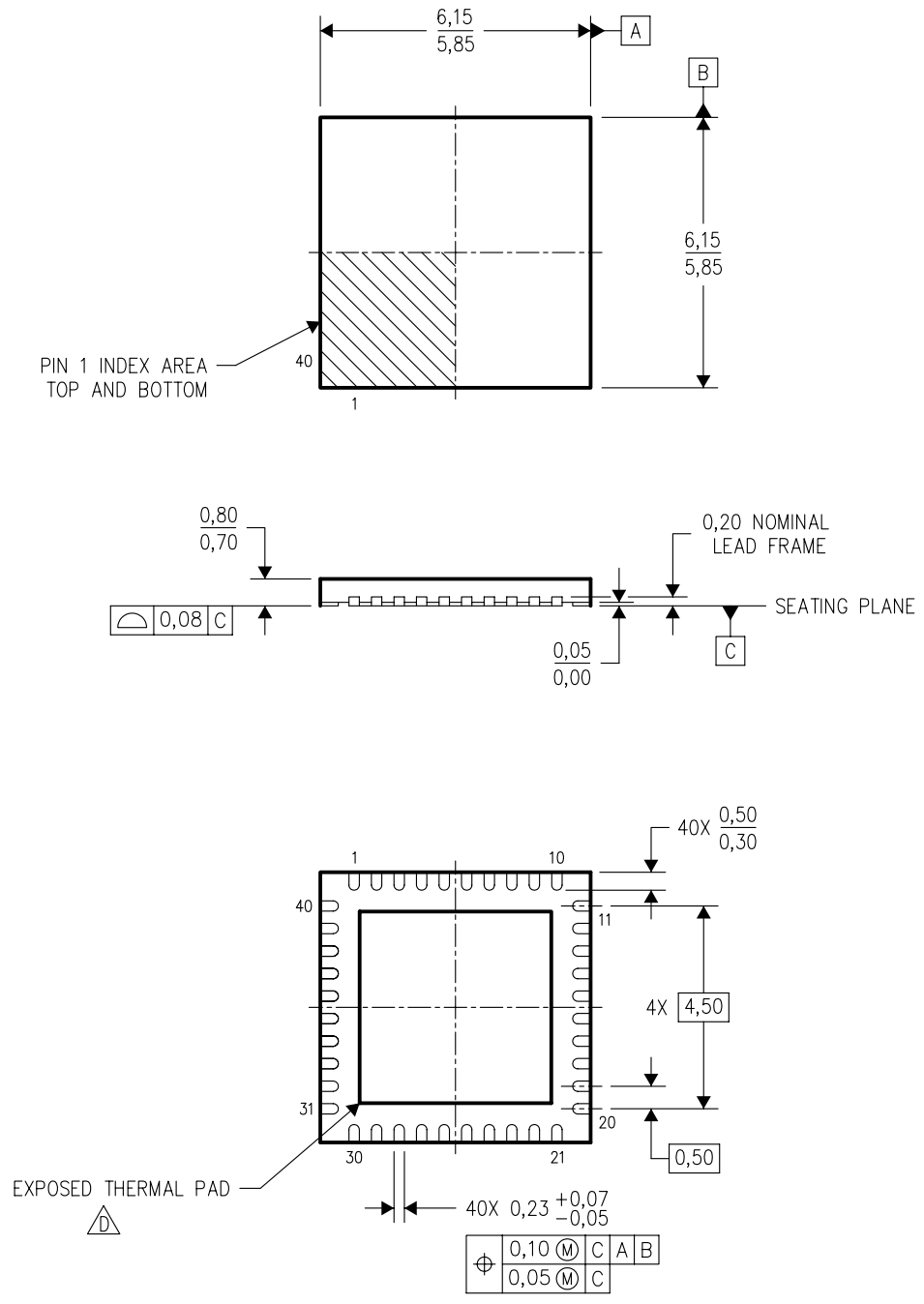
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7822IRTAR	ACTIVE	QFN	RTA	40	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7822IRTARG4	ACTIVE	QFN	RTA	40	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7822IRTAT	ACTIVE	QFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DAC7822IRTATG4	ACTIVE	QFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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