

# Small Signal MOSFET

## 60 V, 310 mA, Single, N-Channel, SOT-23

### Features

- Low  $R_{DS(on)}$
- Small Footprint Surface Mount Package
- Trench Technology
- This is a Pb-Free Device

### Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	60	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (Note 1) Steady State	$I_D$	$T_A = 25^\circ\text{C}$ 260	mA
		$T_A = 85^\circ\text{C}$ 190	
$t < 5$ s		$T_A = 25^\circ\text{C}$ 310	
		$T_A = 85^\circ\text{C}$ 220	
Power Dissipation (Note 1) Steady State $t < 5$ s	$P_D$	300 420	mW
Pulsed Drain Current ( $t_p = 10$ $\mu\text{s}$ )	$I_{DM}$	1.2	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	$-55$ to $+150$	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	300	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)



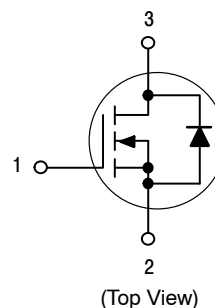
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<http://onsemi.com>

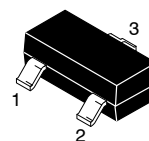
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX (Note 1)
60 V	$3.0 \Omega$ @ 4.5 V	310 mA
	$2.5 \Omega$ @ 10 V	

### Simplified Schematic

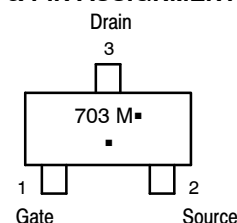
N-Channel



### MARKING DIAGRAM & PIN ASSIGNMENT



**SOT-23  
CASE 318  
STYLE 21**



703 = Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
2N7002ET1G	SOT-23 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# 2N7002E

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			75		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C		1	μA
			T <sub>J</sub> = 125°C		500	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			4.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 240 mA		0.86	2.5	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 mA		1.1	3.0	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 200 mA		80		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		26.7	40	pF
Output Capacitance	C <sub>OSS</sub>			4.6		
Reverse Transfer Capacitance	C <sub>RSS</sub>			2.9		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V; I <sub>D</sub> = 240 mA		0.81		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.31		
Gate-to-Source Charge	Q <sub>GS</sub>			0.48		
Gate-to-Drain Charge	Q <sub>GD</sub>			0.08		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = V (Note 3)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 30 V, I <sub>D</sub> = 200 mA, R <sub>G</sub> = 10 Ω		1.7		ns
Rise Time	t <sub>r</sub>			1.2		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			4.8		
Fall Time	t <sub>f</sub>			3.6		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 200 mA	T <sub>J</sub> = 25°C		0.79	1.2	V
			T <sub>J</sub> = 85°C		0.7		

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
- Switching characteristics are independent of operating junction temperatures

[查询"2N7002E-D"供应商](#)

## TYPICAL CHARACTERISTICS

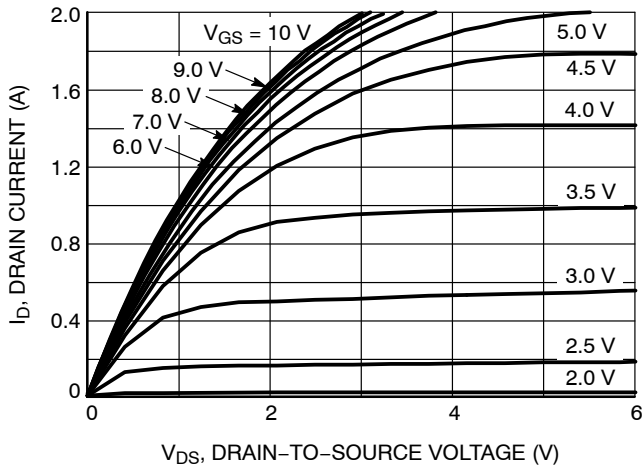


Figure 1. On-Region Characteristics

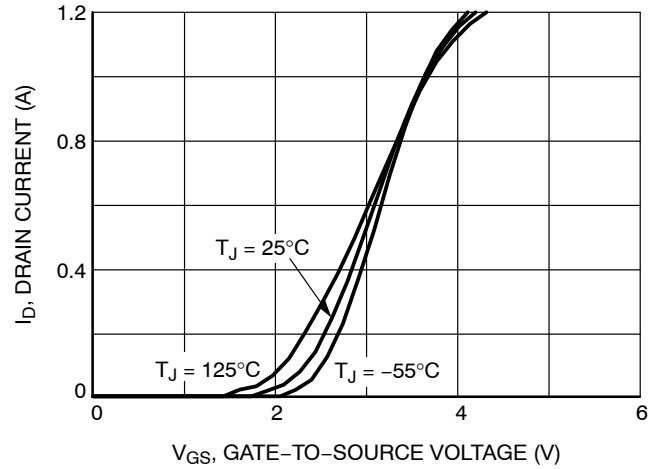


Figure 2. Transfer Characteristics

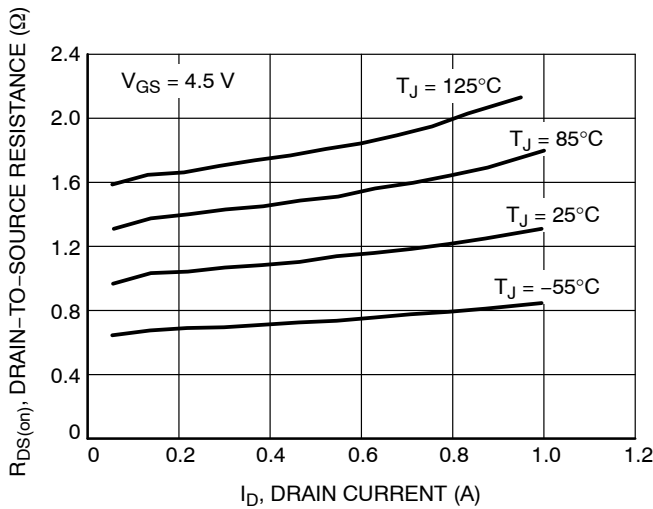


Figure 3. On-Resistance vs. Drain Current and Temperature

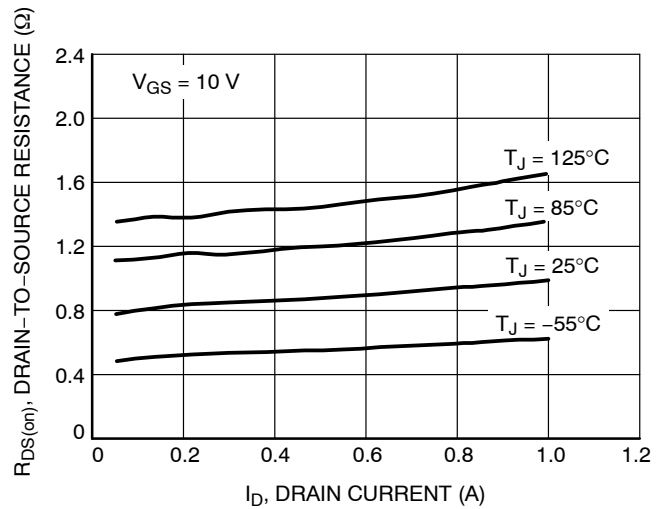


Figure 4. On-Resistance vs. Drain Current and Temperature

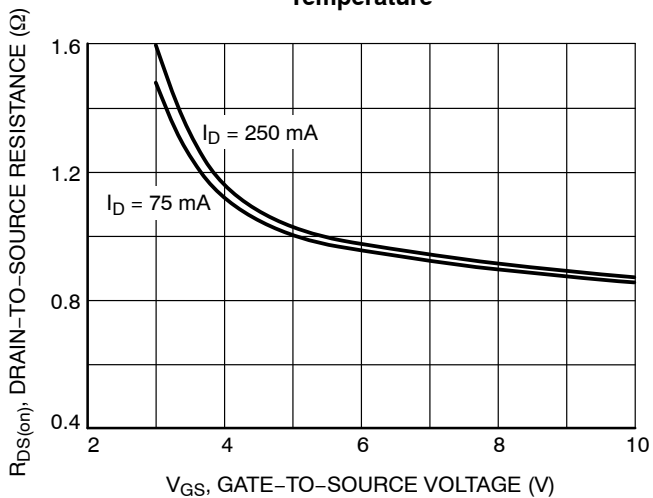


Figure 5. On-Resistance vs. Gate-to-Source Voltage

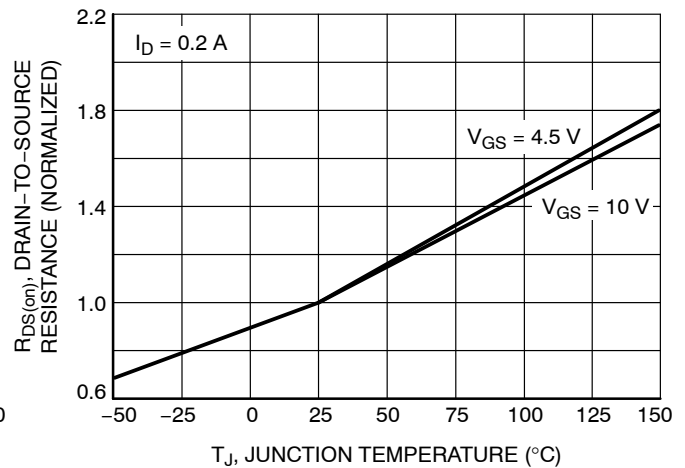


Figure 6. On-Resistance Variation with Temperature

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## TYPICAL CHARACTERISTICS

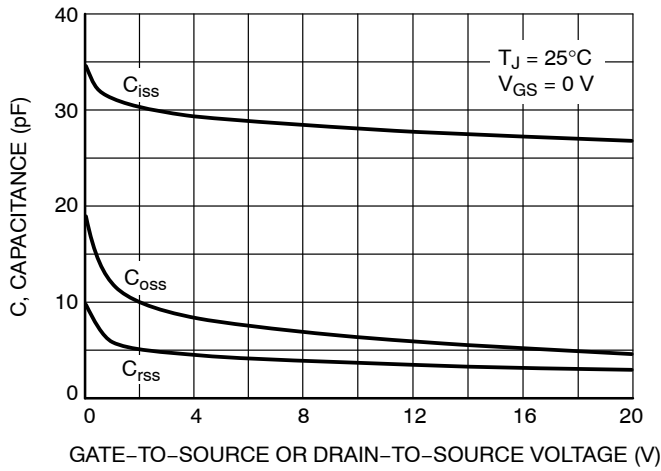


Figure 7. Capacitance Variation

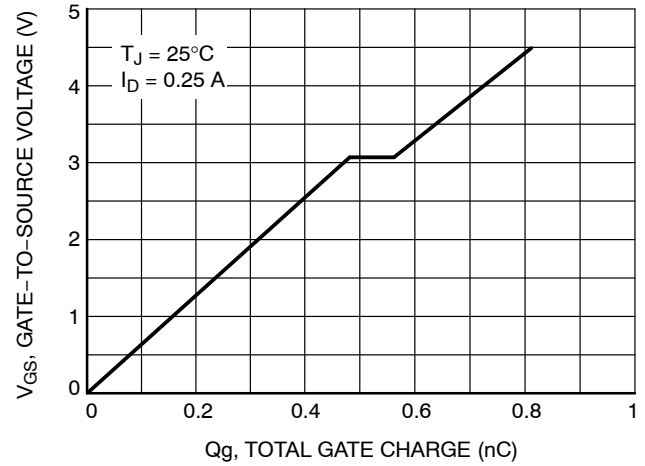


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

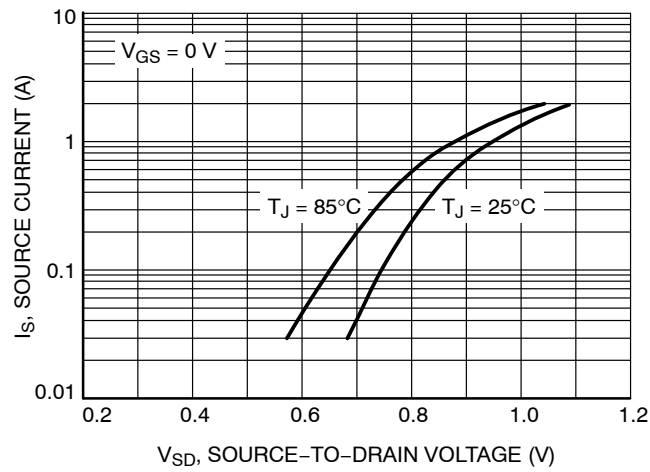


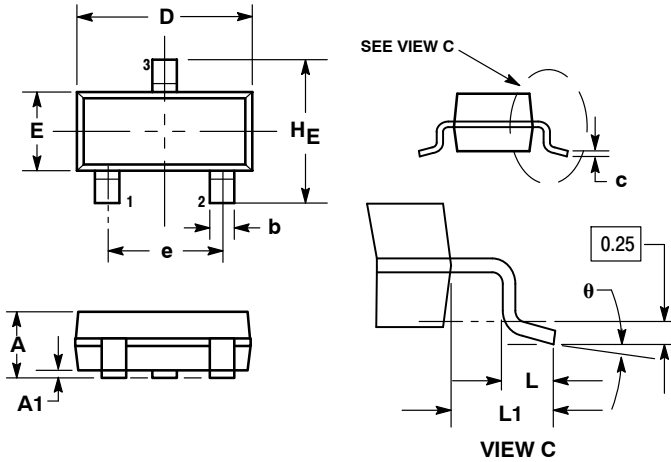
Figure 9. Diode Forward Voltage vs. Current

# 2N7002E

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## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AP

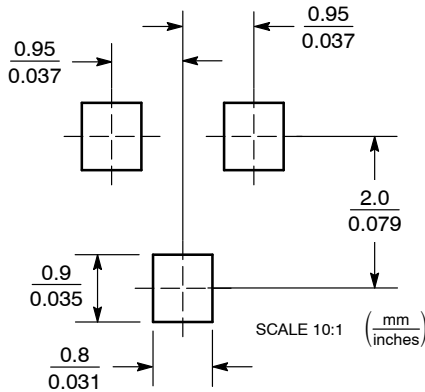


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

## SOLDERING FOOTPRINT



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