REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 25 MARCH 1988

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, BIPOLAR, BIDIRECTIONAL I/O PORT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-87576

SHEET 1 OF 16

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E365

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87576	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8X371	8-bit latched bidirectional I/O port

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-11 (24-lead, 1.250" x .410" x .225") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage	+7.0 V dc maximum
Input voltage	+5.5 V dc maximum
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	.825 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.8 V dc

1/ Must withstand the added P_D due to short circuit tests; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Supply voltage	V_{CC}		1,2,3	4.5	5.5	V
High level input voltage	V_{IH}		1,2,3	2.0		V
Low level input voltage	V_{IL}		1,2,3		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_I = -10 mA	1,2,3		-1.5	V
High level input current 1/	I_{IH}	V_{CC} = 5.5 V V_{IH} = 2.7 V	1,2,3		100	µA
Low level input current 1/	I_{IL}	V_{CC} = 5.5 V V_{IL} < 0.5 V	1,2,3		-550	µA
Low level output voltage $\overline{IV}$ bus ($\overline{IV0}$-$\overline{IV7}$) user bus (UD4-UD7)	V_{OL}	V_{CC} = 4.5 V I_{OL} = 16 mA	1,2,3		0.55	V
		V_{CC} = 4.5 V I_{OL} = 24 mA	1,2,3		0.55	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -3.2 mA	1,2,3	2.4		V
Short circuit output current 2/ $\overline{IV}$ bus ($\overline{IV0}$-$\overline{IV7}$)	I_{OS}	V_{CC} = 5.5 V	1,2,3	-20		mA
UD bus (UD0-UD7)		V_{CC} = 5.5 V	1,2,3	-10		mA
Supply current	I_{CC}	V_{CC} = 5.5 V $\overline{ME}$ = $\overline{UOC}$ = V_{CC}	1,2,3		150	mA
Function test		See 4.3.1c 3/	7,8			
Pulse widths:						
Clock high ↑ MCLK to ↓ MCLK	t_{W1}	3/	9,10,11	30		ns
User input control ↓ $\overline{UIC}$ to ↑$\overline{UIC}$	t_{W2}	MCLK = High 3/	9,10,11	35		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delays:						
UD propagation delay UD to $\overline{IV}$	t_{PD1}	MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UIC}$ = Low 3/	9,10,11		45	ns
UD clock delay ↑ MCLK to $\overline{IV}$	t_{PD2}	UD = Stable; $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UIC}$ = Low 3/			55	ns
UD input delay ↓ $\overline{UIC}$ to $\overline{IV}$	t_{PD3}	UD = Stable; MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = Low 3/			55	ns
$\overline{IV}$ data propagation delay $\overline{IV}$ to UD	t_{PD4}	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low 3/			45	ns
$\overline{IV}$ data clock delay ↑ MCLK to UD	t_{PD5}	WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable 3/ $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low			55	ns
Output enable timing:						
UD output enable ↓ UOC to UD	t_{OE1}	$\overline{UIC}$ = High 3/			45	ns
UD input recovery ↑ $\overline{UIC}$ to UD	t_{OE2}	$\overline{UOC}$ = Low 3/			45	ns
$\overline{IV}$ data master enable ↓ $\overline{ME}$ to $\overline{IV}$	t_{OE3}	WC = $\overline{RC}$ = Low 3/			45	ns
$\overline{IV}$ data read enable ↓ $\overline{RC}$ to $\overline{IV}$	t_{OE4}	WC = $\overline{ME}$ = Low 3/			45	ns
$\overline{IV}$ data write recovery ↓ WC to $\overline{IV}$	t_{OE5}	$\overline{RC}$ = $\overline{ME}$ = Low 3/			45	ns
Output disable timing:						
UD output disable ↑ $\overline{UOC}$ to UD	t_{OD1}	$\overline{UIC}$ = High 3/			40	ns
UD input override ↓ $\overline{UIC}$ to UD	t_{OD2}	$\overline{UOC}$ = Low 3/			45	ns
$\overline{IV}$ data master disable ↑ $\overline{ME}$ to $\overline{IV}$	t_{OD3}	WC = $\overline{RC}$ = Low 3/ 4/			40	ns
$\overline{IV}$ data read disable ↑ $\overline{RC}$ to $\overline{IV}$	t_{OD4}	WC = $\overline{ME}$ = Low 3/ 4/			40	ns
$\overline{IV}$ data write override ↑ WC to $\overline{IV}$	t_{OD5}	$\overline{RC}$ = $\overline{ME}$ = Low 3/ 4/			40	ns

See footnotes at end of table.

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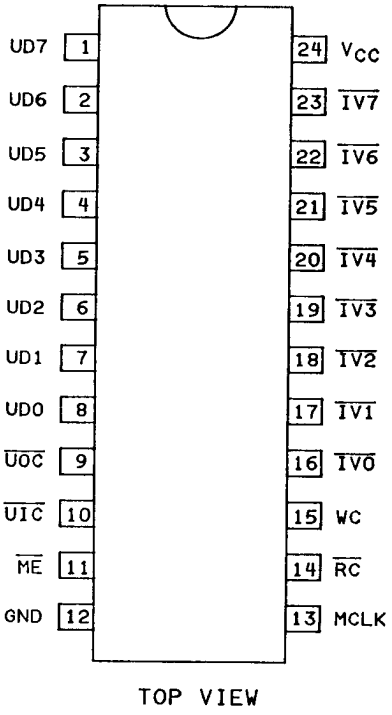
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Setup time:						
UD clock setup time UD to ↓ MCLK	t_{S1}	$\overline{UIC}$ = Low 3/	9,10,11	15		ns
UD setup time UD to ↑ UIC	t_{S2}	MCLK = High 3/		25		ns
User input control setup time ↓ UIC to ↓ MCLK	t_{S3}	3/		25		ns
$\overline{IV}$ data setup time $\overline{IV}$ to ↓ MCLK	t_{S4}	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low 3/		15		ns
$\overline{IV}$ master enable setup time ↓ $\overline{ME}$ to ↓ MCLK	t_{S5}	5/ WC = $\overline{UIC}$ = High 3/		20		ns
$\overline{IV}$ write control setup time ↑ WC to ↓ MCLK	t_{S6}	$\overline{ME}$ = Low; $\overline{UIC}$ = High 3/		40		ns
Hold times:						
UD clock hold time ↓ MCLK to UD	t_{H1}	$\overline{UIC}$ = Low 3/		20		ns
UD control hold time ↑ $\overline{UIC}$ to UD	t_{H2}	MCLK = High 3/		10		ns
User input control hold time ↓ MCLK to ↑ $\overline{UIC}$	t_{H3}	3/		0		ns
$\overline{IV}$ data hold time ↓ MCLK to $\overline{IV}$	t_{H4}	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low 3/	9 10,11	5 20		ns ns
$\overline{IV}$ master enable hold time ↓ MCLK to ↑ $\overline{ME}$	t_{H5}	5/ $\overline{WE}$ = $\overline{UIC}$ = High 3/	9,10,11	0		ns
$\overline{IV}$ write control hold time ↓ MCLK to ↓ WC	t_{H6}	$\overline{ME}$ = Low; $\overline{UIC}$ = High 3/		0		ns

1/ The input current includes the three-state leakage current of the output driver on the data lines.
2/ Only one output may be shorted at a time.
3/ Test loading circuit and timing diagrams see figures 4 and 5.
4/ These parameters are measured with a capacitive loading of 50 pf and represent the output driver turn-off time.
5/ If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.



TOP VIEW

Pin. no.	Identifier	Function
1-8	UD7-UD0	Three-state bidirectional user data (UD) bus. UD0 corresponds to IV0.
9	UOC	User output control-active low input to enable data output to UD0-UD7.
10	UIC	User input control-active low input to enable data input from UD0-UD7.
11	ME	Master enable-active low input to enable the IV bus for data input or data output, UD-bus operations are unaffected.
12	GND	Ground
13	MCLK	Master clock-active high input (from microcontroller) used to strobe data into data latches from the IV and UD buses.
14	RC	Read control-active low input to enable data output to IV0-IV7.
15	WC	Write command-active high input (from microcontroller) to enable the writing of data into the data latches from the IV bus (provided UIC is not low).
16-23	IV0-IV7	Interface vector (input/output bus)-three-state bidirectional, microcontroller data bus, IV0 corresponds to UD0.
24	Vcc	+5 V power supply.

FIGURE 1. Terminal connections.

Functional operation

UD bus control

The user data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. Data input to the UD bus is synchronous with MCLK, that is, with $\overline{UIC}$ low, information is written into the data latches only when MCLK is high. Output drivers on the UD bus are enabled when $\overline{UOC}$ is low and $\overline{UIC}$ is high.

Input/output control of UD Bus

$\overline{UIC}$	$\overline{UOC}$	MCLK	function of UD bus
H	L	X	output
L	X	H	input data
L	X	L	inactive
H	H	X	inactive

X = don't care

Bus logic level

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note. A logic "1" in microcontroller software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted). The device wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

Input/output control of $\overline{IV}$ bus

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{UIC}$	function of $\overline{IV}$ bus
L	L	L	X	X	output data
L	X	H	H	H	input data
L	H	L	X	X	inactive
L	X	H	X	L	inactive
L	X	H	L	H	inactive
H	X	X	X	X	inactive

$\overline{IV}$ bus control

Input/output control of the $\overline{IV}$ bus is shown above. This bus is controlled by $\overline{RC}$, WC, $\overline{ME}$, and MCLK. The $\overline{IV}$ bus is enabled for output (microcontroller read operation) when $\overline{ME}$, $\overline{RC}$, and WC are all low. Data is written into the data latches from the $\overline{IV}$ bus when $\overline{ME}$ is low and both WC and MCLK are high. To avoid data-input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently. The microcontroller left bank ($\overline{LB}$) and right bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus acting as a ninth address bit. If more than one I/O port are to be connected to the same bank ($\overline{LB}$ or $\overline{RB}$) of the microcontroller, selection of each device must be accomplished with external control logic to avoid bus conflicts.

FIGURE 2. Truth tables.

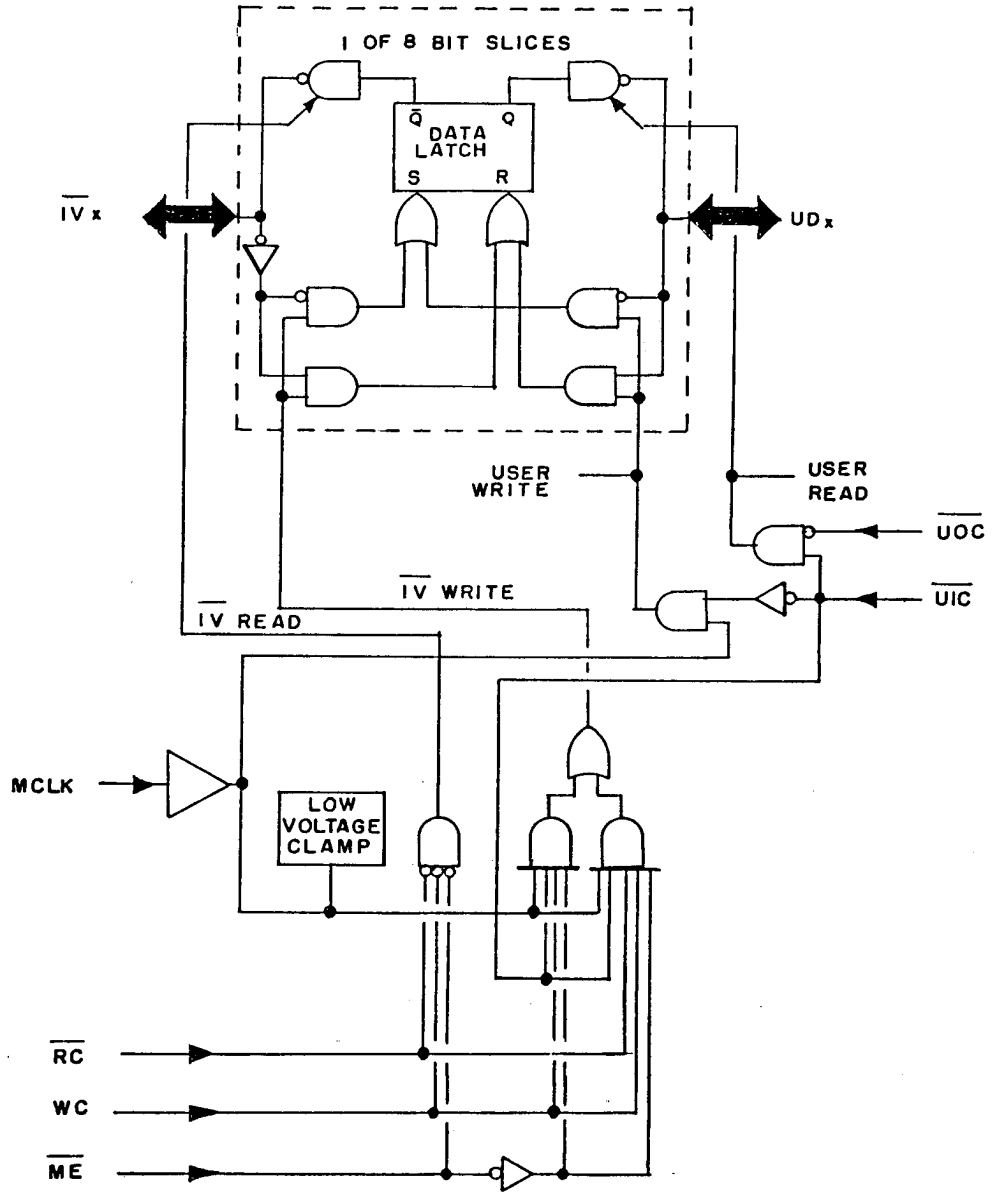
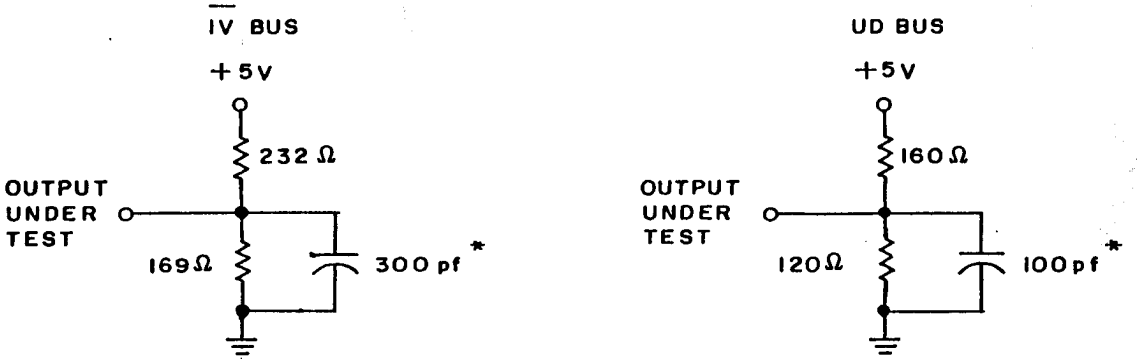
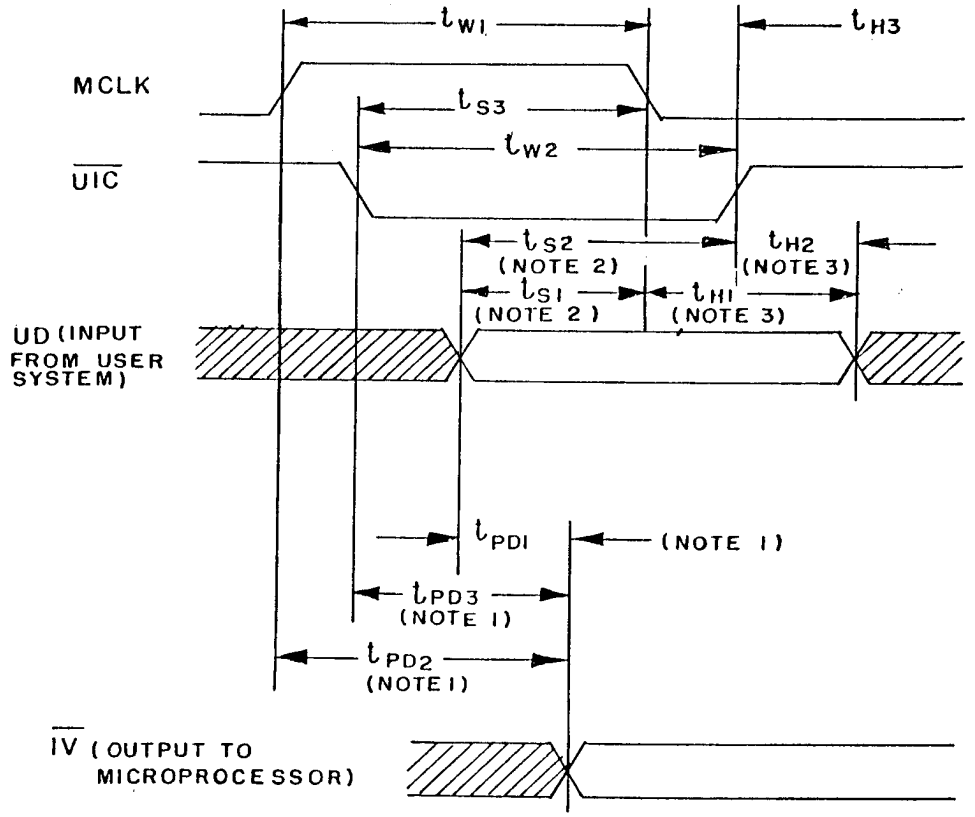


FIGURE 3. Logic diagram.



* Total equivalent load = fixed capacitance and test circuit capacitance.

FIGURE 4. Test loading circuits.

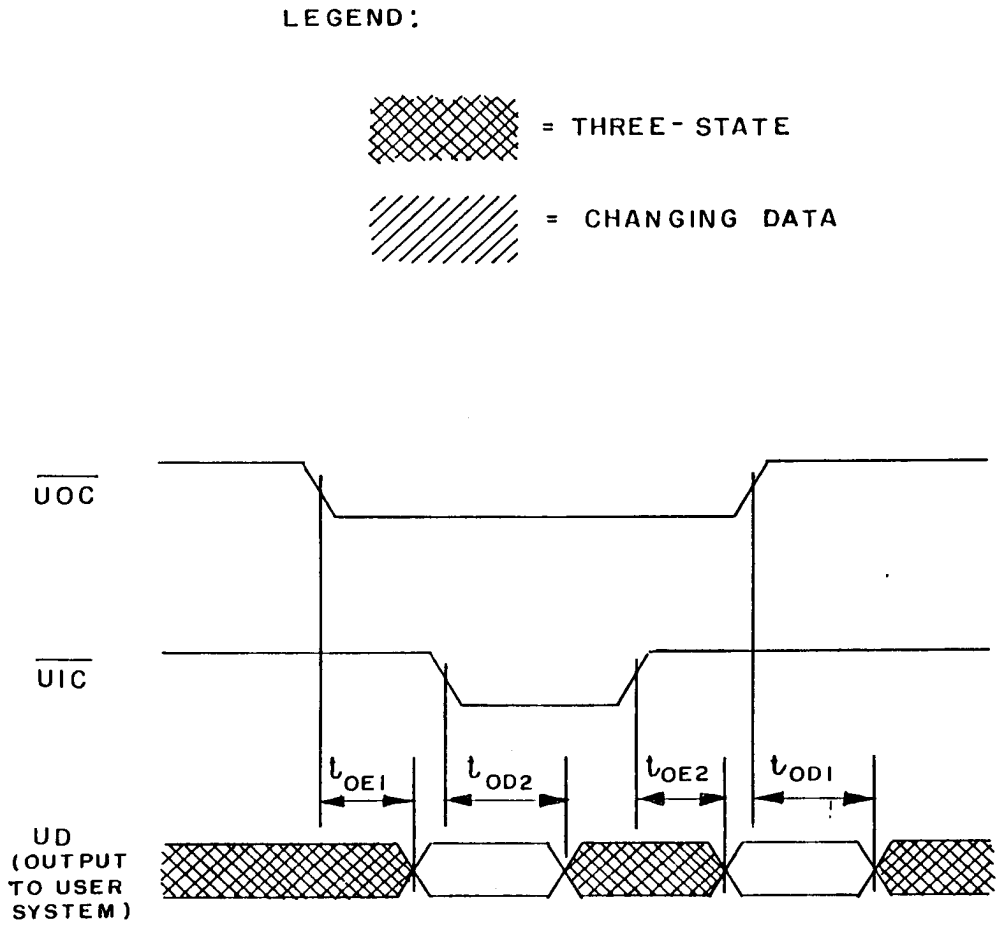


STATIC CONDITIONS:
SC = WC = $\overline{ME}$ = Low; $\overline{UOC}$ = High

a. User data input timing

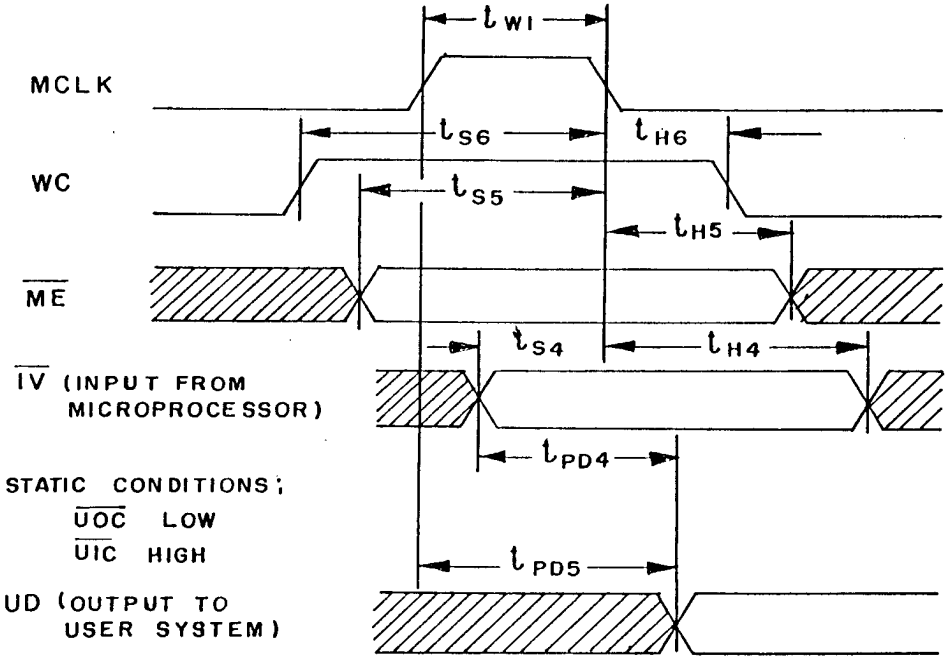
NOTES:
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from t_{PD1}, t_{PD2}, t_{PD3}.
2. The UD input must satisfy the setup-time requirements for both t_{S1} and t_{S2}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1} and t_{H2}.

FIGURE 5. Timing diagrams.

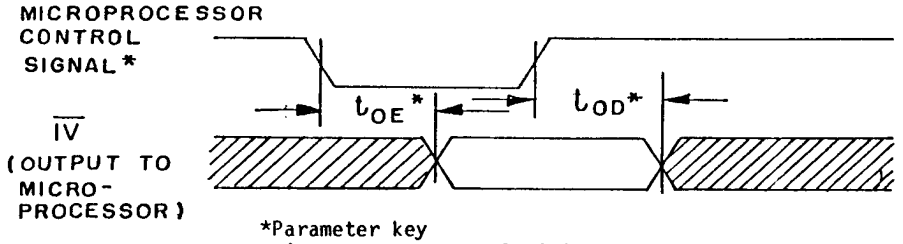


b. User data output timing

FIGURE 5. Timing diagrams - Continued.



c. Microcontroller write cycle timing



*Parameter key

microprocessor control signal	AC timing parameters		Static conditions
$\overline{ME}$	t_{OE3}	t_{OD3}	SC = WC = Low
$\overline{RC}$	t_{OE4}	t_{OD4}	SC = $\overline{ME}$ = Low
SC	t_{OE5}	t_{OD5}	$\overline{RC}$ = $\overline{ME}$ = Low

d. Microcontroller select cycle timing

FIGURE 5. Timing diagrams - Continued.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests sufficient to verify the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,7,8,9, 10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8757601XX	18324	8X371/BXA	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834

011929