Freescale Semiconductor
Technical Data

Document Number: MRF5P21045N
Rev. 0, 4/2007

RoHS

RF Power Field-Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

MRF5P21045NR1

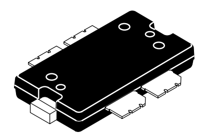
2110-2170 MHz, 10 W AVG., 28 V
2 x W-CDMA, DUAL PATH
LATERAL N-CHANNEL
RF POWER MOSFET

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. Dual path topology suitable for Doherty, quadrature, single-ended and push-pull applications.

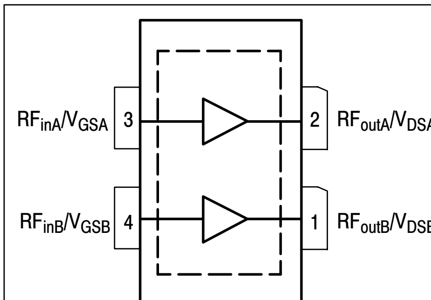
- Typical 2-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 500 mA, P_{out} = 10 Watts Avg., Full Frequency Band, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 14.5 dB
  Drain Efficiency — 25.5%
  IM3 @ 10 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
  ACPR @ 5 MHz Offset — -39 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 45 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1486-03, STYLE 1
TO-270 WB-4



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 45 W CW Case Temperature 77°C, 10 W CW	$R_{\theta JC}$	 1.35 1.48	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

freescale™ semiconductor

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

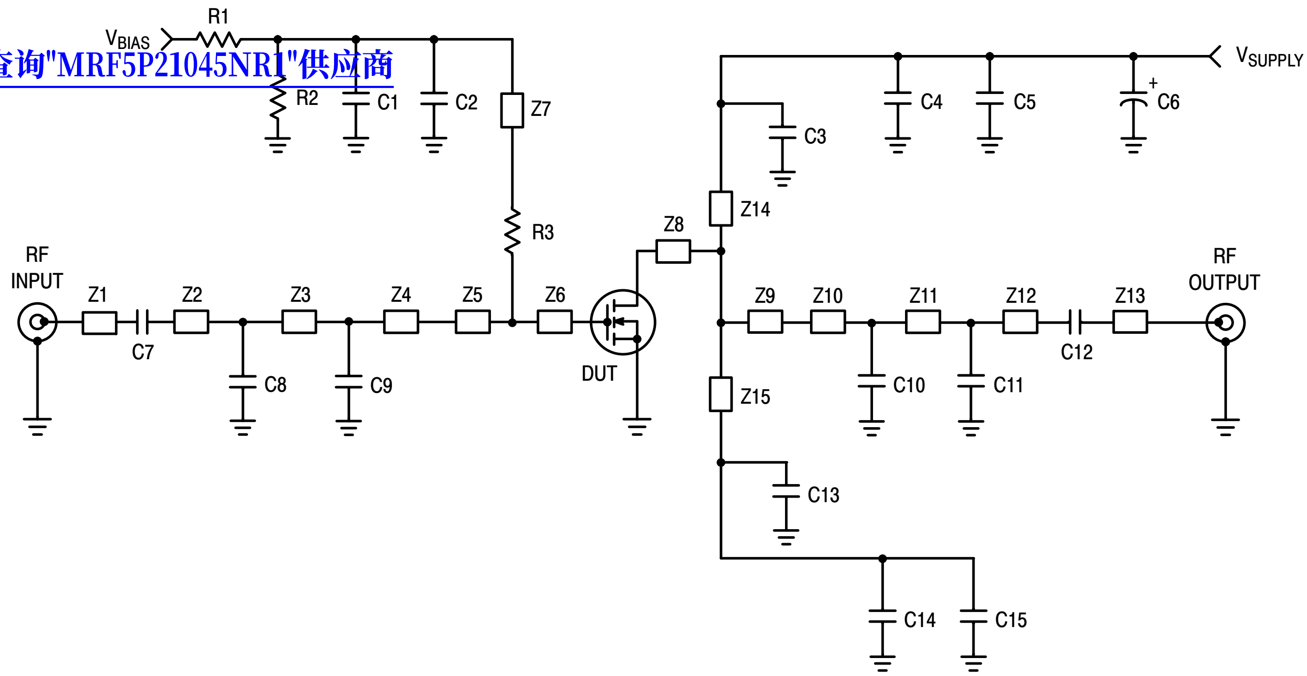
Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 120 μAdc)	$V_{GS(th)}$	2	—	3.5	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	—	3.8	—	Vdc
Fixture Gate Quiescent Voltage (2) (V_{DD} = 28 Vdc, I_D = 500 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6	7.6	10	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.2 Adc)	$V_{DS(on)}$	0.2	0.3	0.35	Vdc
Dynamic Characteristics (1,3)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.9	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	124	—	pF
Input Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	247	—	pF

Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg., f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz, 2-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 measured in 3.84 MHz Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	13.5	14.5	16.5	dB
Drain Efficiency	η_D	23.5	25.5	—	%
Intermodulation Distortion	IM3	—	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	—	-39	-37	dBc
Input Return Loss	IRL	—	-12	-8	dB

1. Measurement made with device in single-ended configuration. (See Figure 4, Possible Circuit Topologies)
2. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
3. Part internally matched both on input and output.



Z1, Z13	0.250″ x 0.080″ Microstrip	Z9	0.385″ x 1.000″ Microstrip
Z2	1.012″ x 0.080″ Microstrip	Z10	0.179″ x 0.080″ Microstrip
Z3	0.165″ x 0.080″ Microstrip	Z11	0.527″ x 0.080″ Microstrip
Z4	0.378″ x 0.080″ Microstrip	Z12	0.789″ x 0.080″ Microstrip
Z5	0.365″ x 1.000″ Microstrip	Z14, Z15	0.270″ x 0.080″ Microstrip
Z6, Z8	0.115″ x 1.000″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z7	0.510″ x 0.080″ Microstrip		

Figure 2. MRF5P21045NR1 Test Circuit Schematic — Single-Ended Configuration

Table 6. MRF5P21045NR1 Test Circuit Component Designations and Values — Single-Ended Configuration

Part	Description	Part Number	Manufacturer
C1	220 nF Chip Capacitor	18125C224KAT4A	AVX
C2, C3, C7, C12, C13	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4, C5, C14, C15	6.8 μF Chip Capacitors	C4532X5R1H685MT	TDK
C6	220 μF, 63 V Electrolytic Capacitor, Radial	EMVY630ATR221MKE0S	Nippon Chemi-Con
C8, C10	1 pF Chip Capacitors	ATC100B1R0BT500XT	ATC
C9	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C11	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061001FKTA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKTA	Vishay

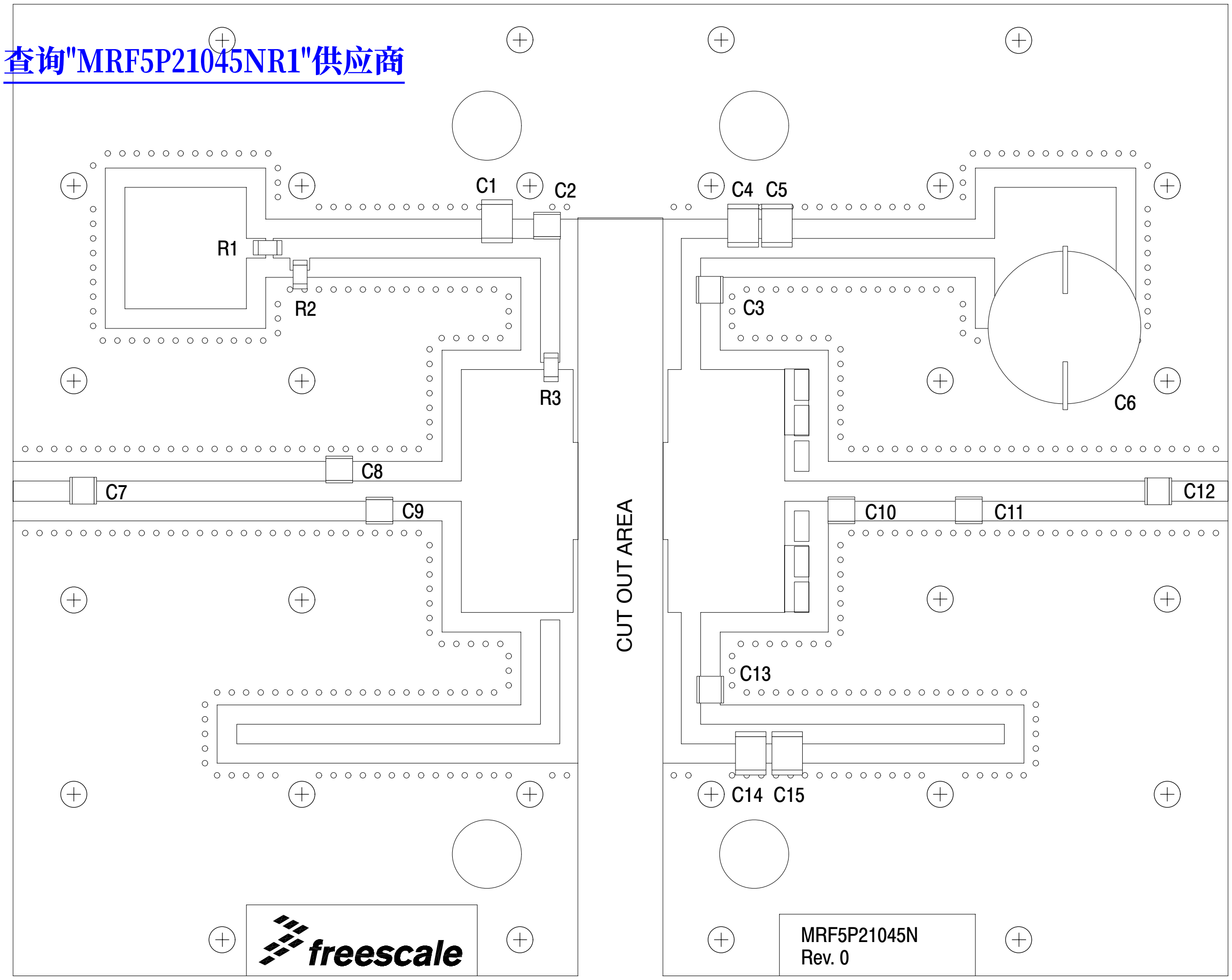


Figure 3. MRF5P21045NR1 Test Circuit Component Layout — Single-Ended Configuration

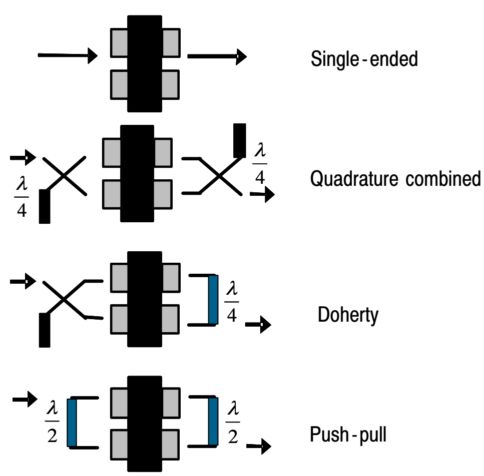


Figure 4. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

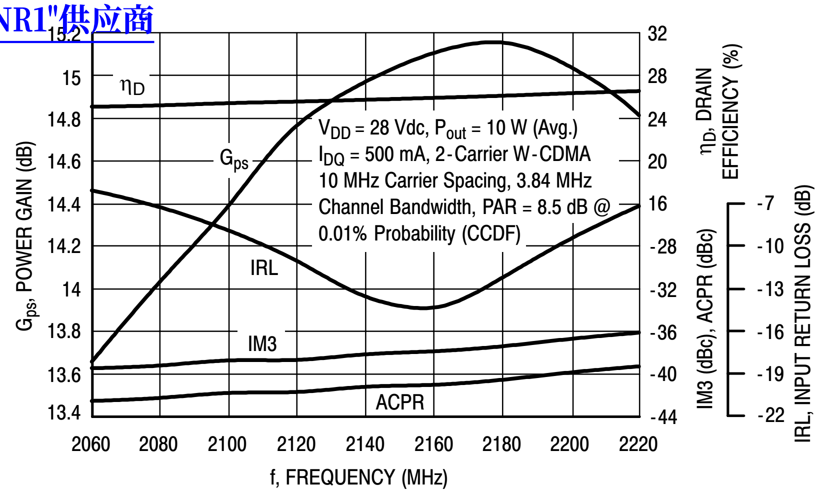


Figure 5. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 10 Watts Avg.

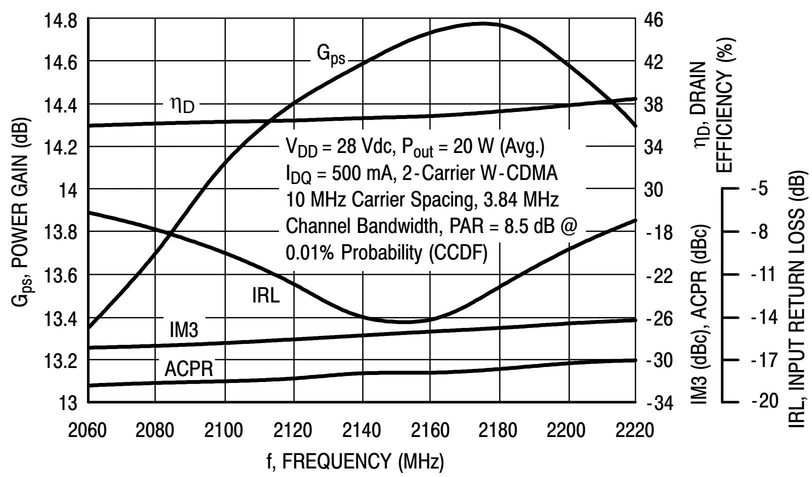


Figure 6. 2-Carrier W-CDMA Broadband Performance @ P_{out} = 20 Watts Avg.

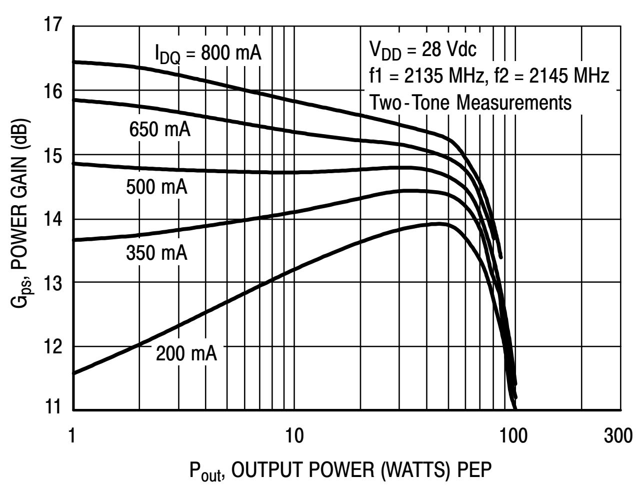


Figure 7. Two-Tone Power Gain versus Output Power

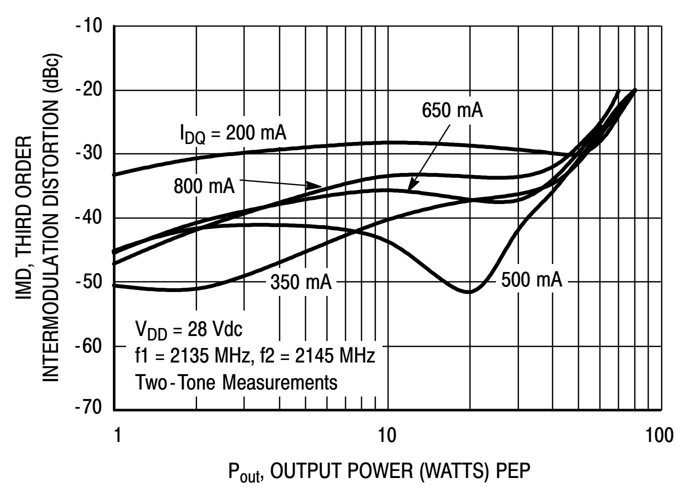


Figure 8. Third Order Intermodulation Distortion versus Output Power

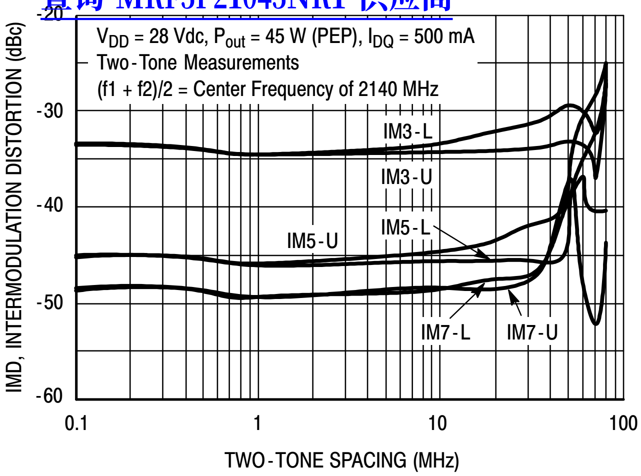


Figure 9. Intermodulation Distortion Products versus Tone Spacing

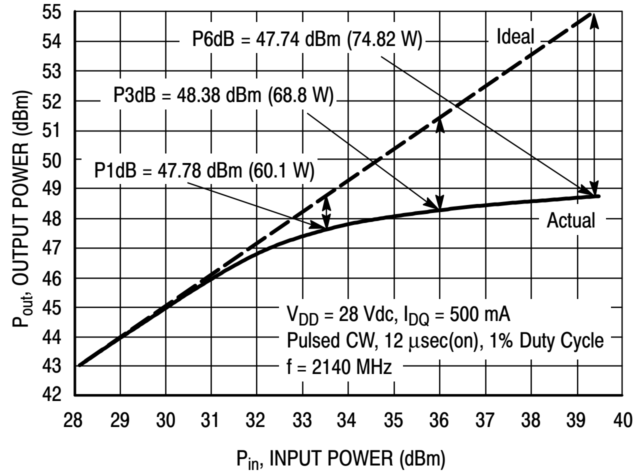


Figure 10. Pulsed CW Output Power versus Input Power

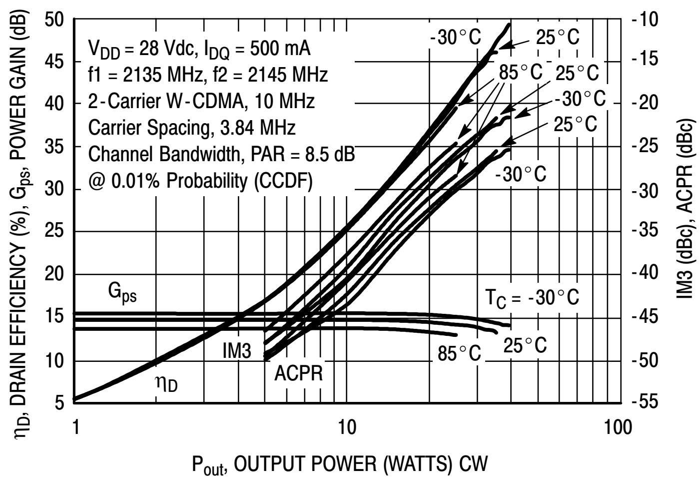


Figure 11. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

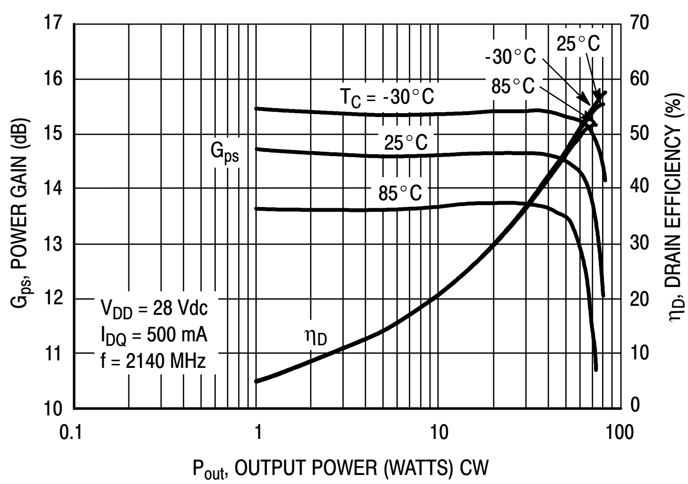


Figure 12. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

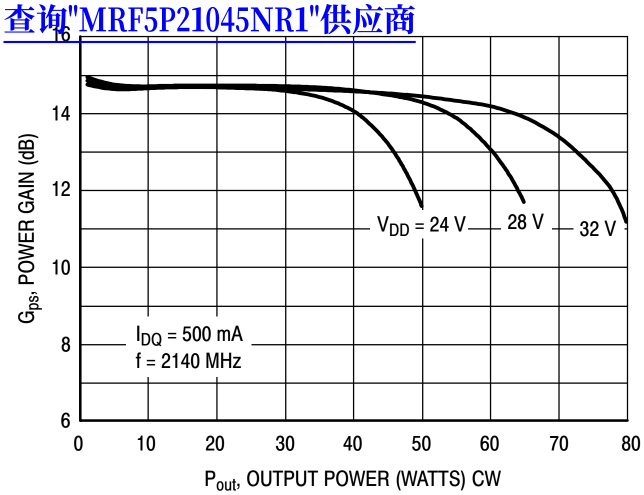
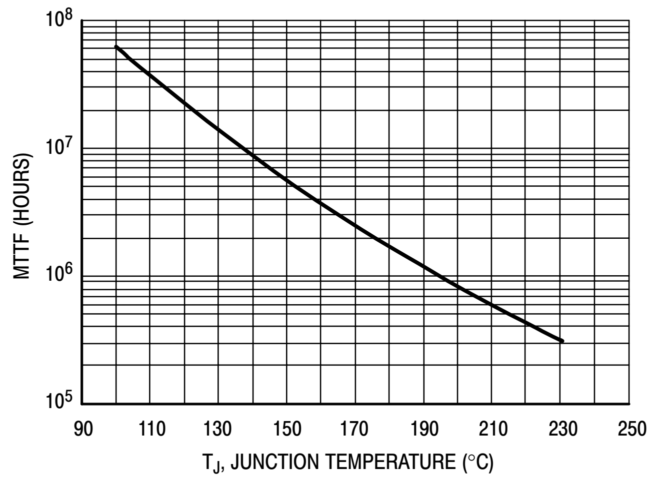


Figure 13. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 10 W Avg., and η_D = 25.5%.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/ Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 14. MTTF versus Junction Temperature

W-CDMA TEST SIGNAL

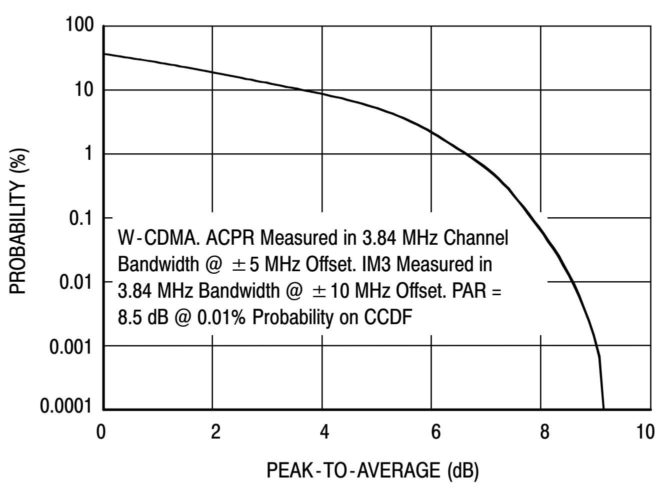


Figure 15. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal

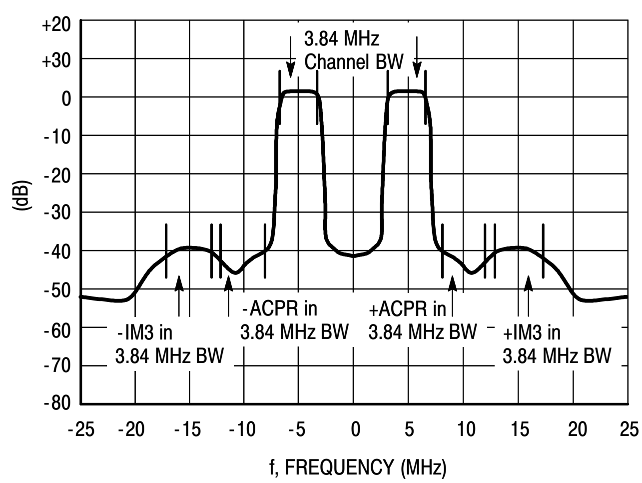
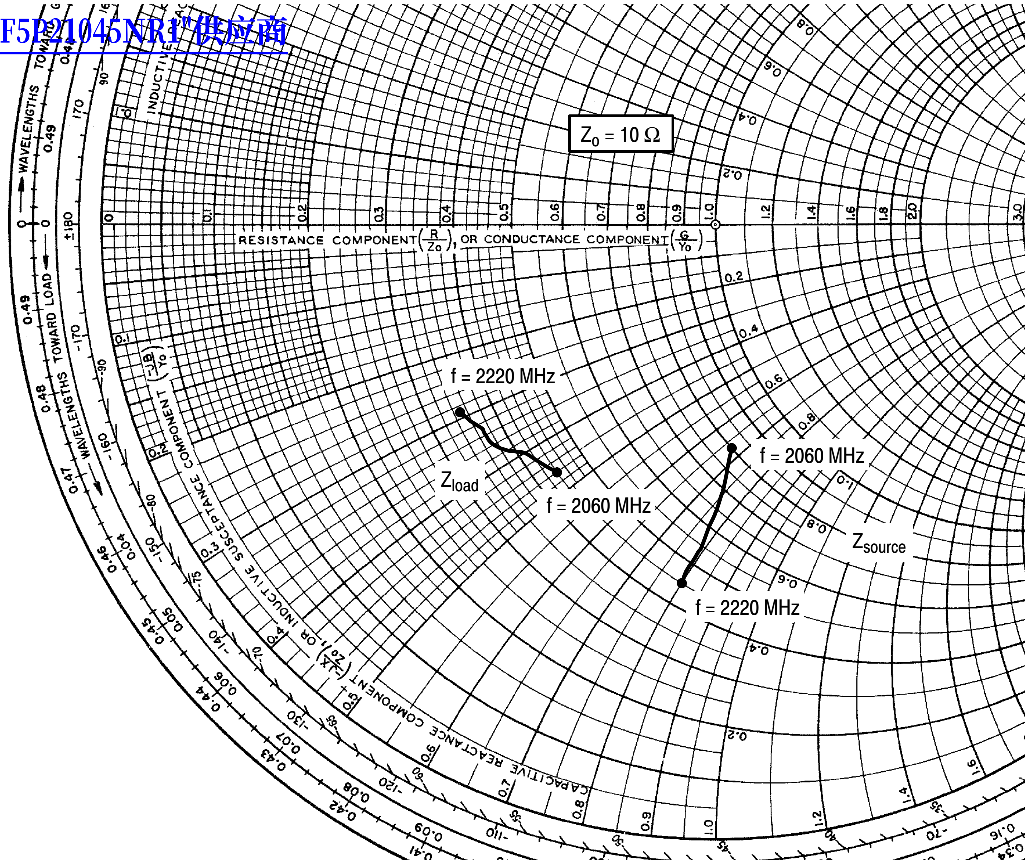


Figure 16. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	8.01 - j6.68	4.38 - j4.62
2080	7.66 - j6.94	4.27 - j4.43
2100	7.26 - j7.20	4.12 - j4.04
2120	6.76 - j7.45	3.98 - j3.90
2140	6.28 - j7.71	3.81 - j3.69
2160	5.82 - j7.78	3.73 - j3.50
2180	5.37 - j7.85	3.65 - j3.30
2200	4.92 - j7.85	3.57 - j3.11
2220	4.46 - j7.97	3.49 - j2.92

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

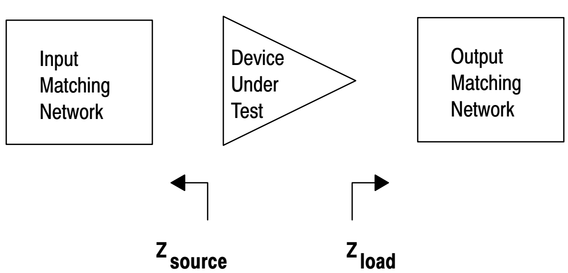
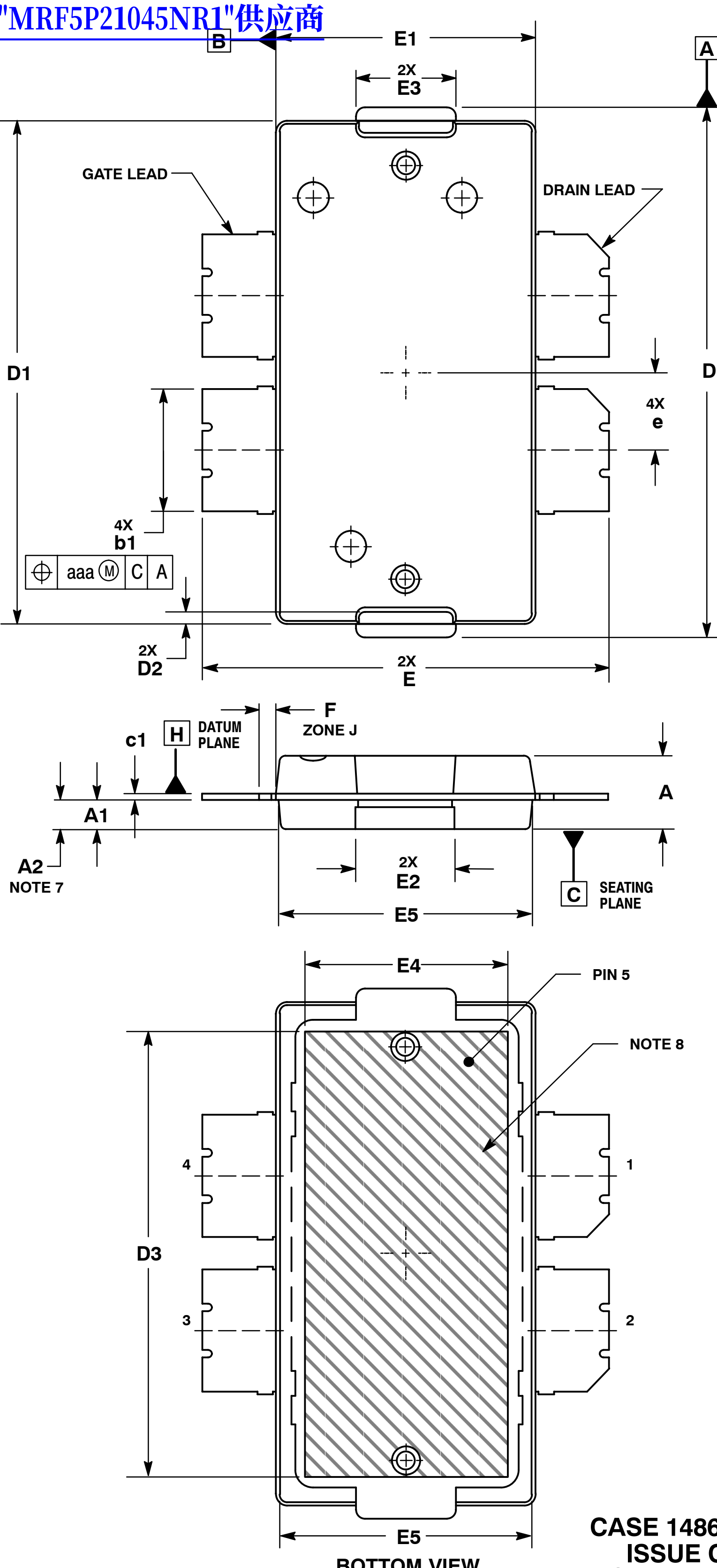


Figure 17. Series Equivalent Source and Load Impedance — Single-Ended Configuration

PACKAGE DIMENSIONS



CASE 1486-03
ISSUE C
TO-270 WB-4
PLASTIC

NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	April 2007	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com