

## Microprocessor Supervisory Circuit

### FEATURES

- *Guaranteed* Reset Assertion at  $V_{CC} = 1V$
- 8-Pin SOIC Plastic Package
- 2.0mA Maximum Supply Current
- 4.62V/4.37V Precision Voltage Monitor
- Power OK/Reset Time Delay: 600ms
- Minimum External Component Count
- Superior Upgrade for DS1232

### APPLICATIONS

- Critical  $\mu P$  Power Monitoring
- Intelligent Instruments
- Computers and Controllers
- Automotive Systems

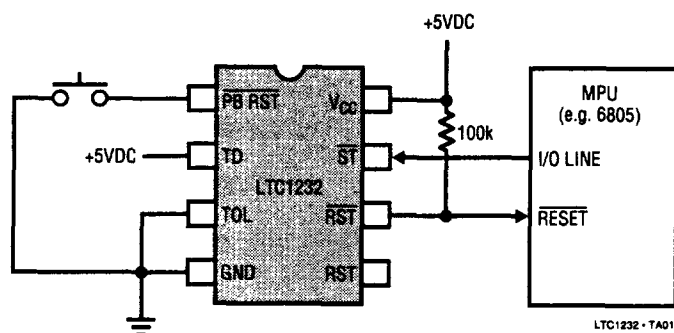
### DESCRIPTION

The LTC1232 provides power supply monitoring, watchdog timing and external reset for microprocessor systems. A precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the reset outputs are forced to active states. The  $\overline{RST}$  output is guaranteed to remain logic low even with  $V_{CC}$  as low as 1V.

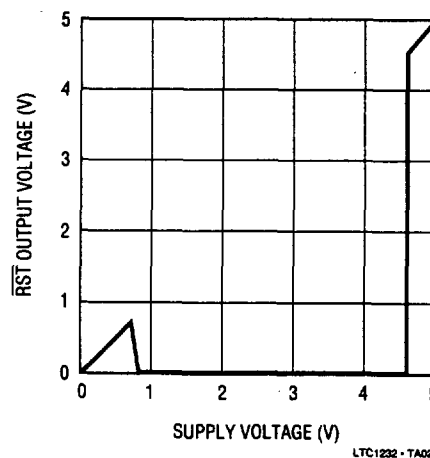
The LTC1232 has an internal watchdog timer which forces the reset outputs to active states when the Strobe input is not forced low prior to a preset time-out period. The watchdog timing can be set to operate on time-out periods of typically 150ms, 600ms or 1.2 seconds.

The LTC1232 performs push-button reset control. The LTC1232 debounces the push-button input and guarantees an active reset pulse width of 250ms minimum.

### TYPICAL APPLICATION



$\overline{RST}$  Output Voltage vs Supply Voltage



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### ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

**Terminal Voltage**

V<sub>CC</sub> ..... -0.3V to 7.0V

ST and RST ..... -0.3V to 7.0V

All Other Inputs and Outputs ..... -0.3V to V<sub>CC</sub> + 0.3V

Power Dissipation ..... 500mW

**Operating Temperature Range**

LTC1232C ..... 0°C to 70°C

LTC1232I ..... -40°C to 85°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

### PACKAGE/ORDER INFORMATION

<p>TOP VIEW N8 PACKAGE 8-LEAD PLASTIC DIP LTC1232 - PO01</p>	ORDER PART NUMBER
	LTC1232CN8 LTC1232IN8
<p>TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SOIC LTC1232 - PO02</p>	LTC1232CS8 LTC1232IS8
	S8 PART MARKING
	1232 1232I

### PRODUCT SELECTION GUIDE

	Pins	Reset	Watchdog Timer	Battery Backup	Power Fail Warning	RAM Write Protect	Push-Button Reset	Conditional Battery Backup
LTC1232	8	X	X				X	
LTC690	8	X	X	X	X			
LTC691	16	X	X	X	X	X		
LTC694	8	X	X	X	X			
LTC695	16	X	X	X	X	X		
LTC699	8	X	X					
LTC1235	16	X	X	X	X	X	X	X

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## RECOMMENDED OPERATING CONDITIONS $V_{CC}$ = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage	●	4.5	5.0	5.5	V
$V_{IH}$	$\overline{ST}$ and $\overline{PB}$ RST Input High Level	●	2.0		$V_{CC} + 0.3$	V
$V_{IL}$	$\overline{ST}$ and $\overline{PB}$ RST Input Low Level	●	-0.3		0.8	V

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{IL}$	Input Leakage	(Note 3) ●	-1.0		1.0	$\mu A$
$I_{OH}$	Output Current at 2.4V	(Note 5) ●	-1.0	-13.0		mA
$I_{OL}$	Output Current at 0.4V	(Note 5) ●	2.0	6.0		mA
$I_{CC}$	Supply Current	(Note 4) ●		0.5	2.0	mA
$V_{CCTP}$	$V_{CC}$ Trip Point	TOL = GND ●	4.50	4.62	4.74	V
$V_{CCTP}$	$V_{CC}$ Trip Point	TOL = $V_{CC}$ ●	4.25	4.37	4.49	V
$V_{HYS}$	$V_{CC}$ Trip Point Hysteresis			40		mV
$V_{RST}$	RST Output Voltage at $V_{CC} = 1V$	$I_{SINK} = 10\mu A$		4	200	mV

## AC CHARACTERISTICS $V_{CC}$ = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PB}$	$\overline{PB}$ RST = $V_{IL}$	●	40			ms
$t_{RST}$	RESET Active Time	●	250	610	1000	ms
$t_{ST}$	$\overline{ST}$ Pulse Width	●	20			ns
$t_{RPD}$	$V_{CC}$ Detect to RST and $\overline{RST}$	●			100	ns
$t_F$	$V_{CC}$ Slew Rate 4.75V-4.25V	●	300			$\mu s$
$t_{RPU}$	$V_{CC}$ Detect to RST and $\overline{RST}$ (Reset Active Time)	$t_R = 5\mu s$ ●	250	610	1000	ms
$t_R$	$V_{CC}$ Slew Rate 4.25V-4.75V	●	0			ns
$t_{TD}$	$\overline{ST}$ Pin Detect to RST and $\overline{RST}$ (Watchdog Time-Out Period)	TD = GND ● TD = Floating ● TD = $V_{CC}$ ●	60 250 500	150 610 1200	250 1000 2000	ms ms ms
$C_{IN}$	Input Capacitance			5		pF
$C_{OUT}$	Output Capacitance			5		pF

The ● indicates specifications which apply over the full operating temperature.

**Note 1:** Absolute maximum ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** The  $\overline{PB}$  RST pin is internally pulled up to  $V_{CC}$  with an internal impedance of 10k typical. The TD pin has internal bias current.

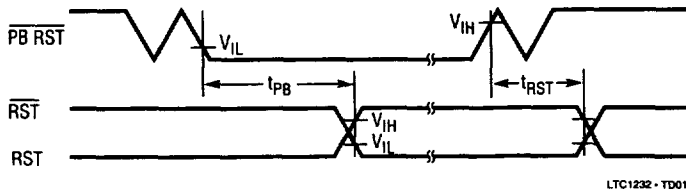
**Note 4:** Measured with outputs open.

**Note 5:** The RST pin is an open drain output.

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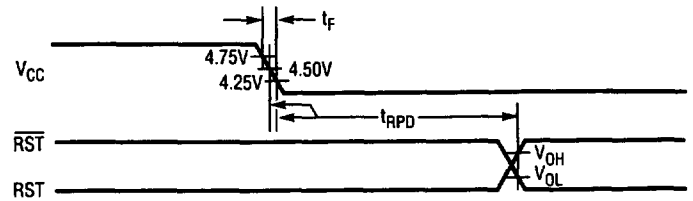
**TIMING DIAGRAMS**

**Push-Button Reset**



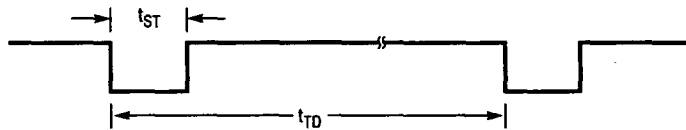
LTC1232 - TD01

**Power Down**



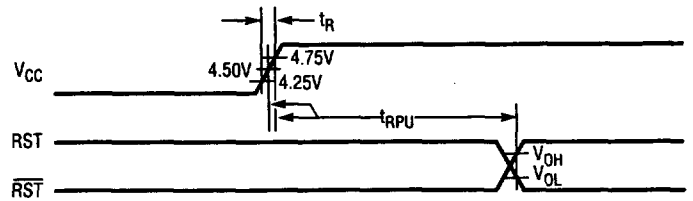
LTC1232 - TD03

**Strobe Input**



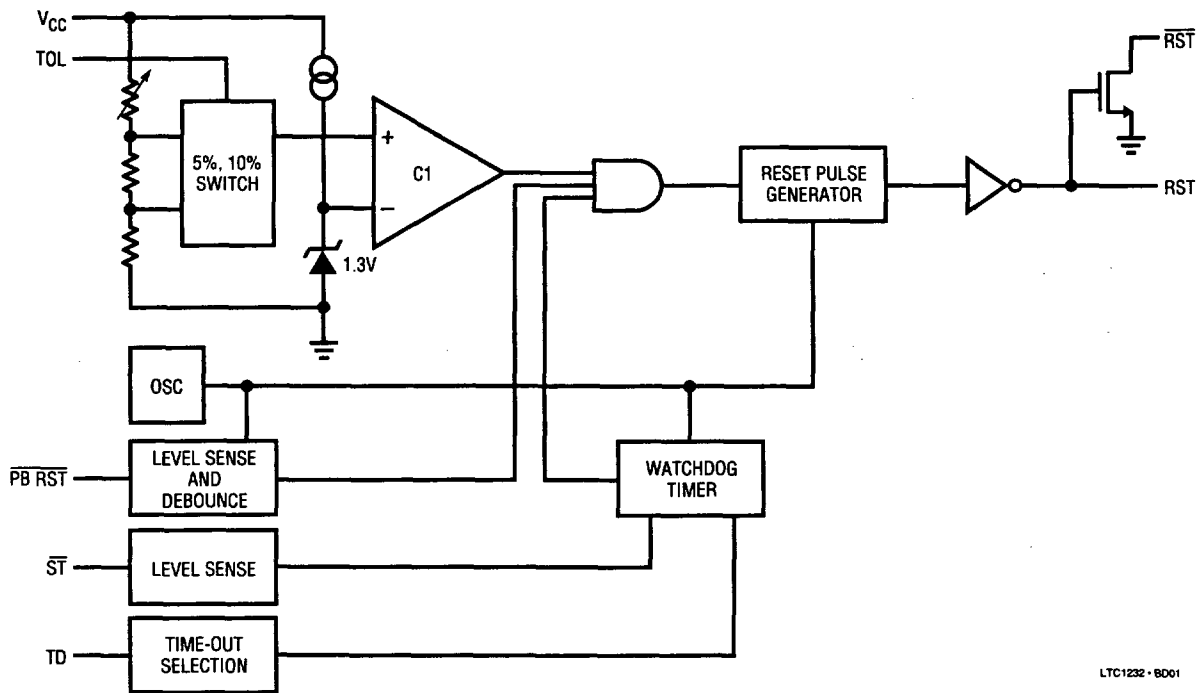
LTC1232 - TD02

**Power Up**



LTC1232 - TD04

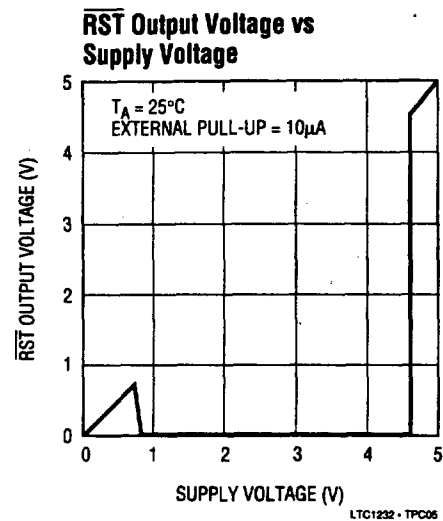
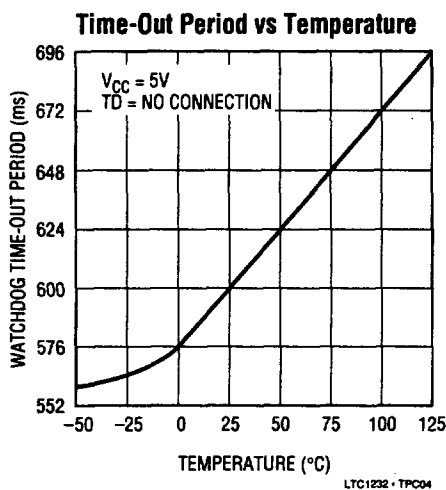
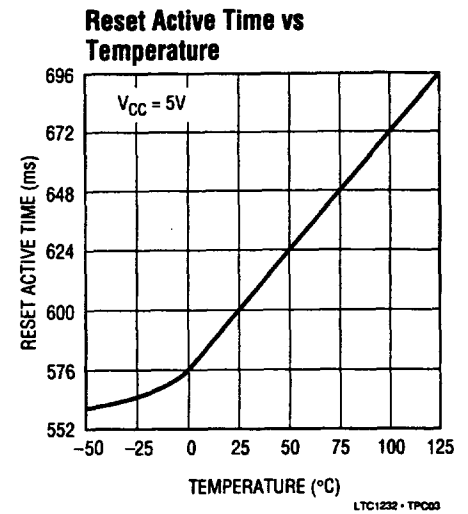
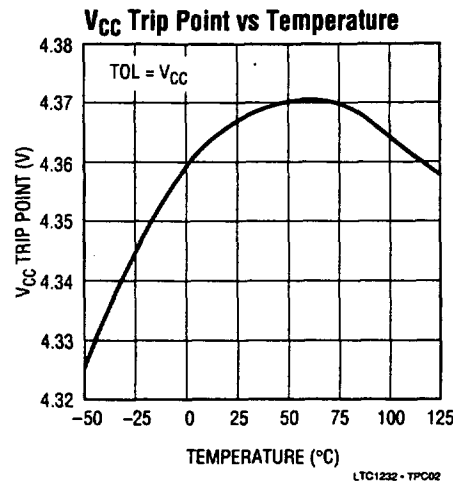
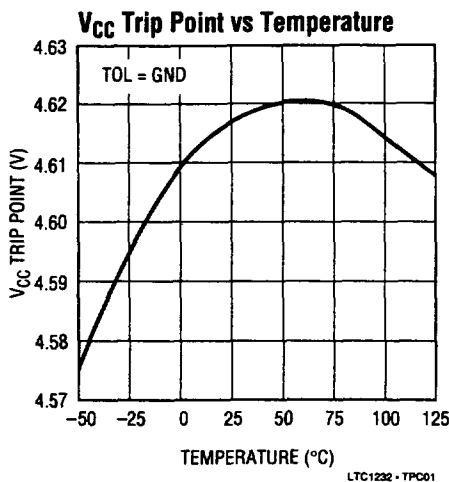
**BLOCK DIAGRAM**



LTC1232 - BD01

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## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**V<sub>CC</sub>**: +5V supply input. The V<sub>CC</sub> pin should be bypassed with a 0.1μF capacitor.

**GND**: Ground pin.

**PB RST**: Logic input to be directly connected to a push-button. The  $\overline{\text{PB RST}}$  input requires an active low signal which is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset outputs remain in active states for a minimum of 250ms after  $\overline{\text{PB RST}}$  is released from logic low level.

**TOL**: Input to select 5% or 10% variation on V<sub>CC</sub>. When TOL is connected to GND, the reset pulse generator forces the reset outputs to active states as V<sub>CC</sub> falls below 4.75V (4.62V typical). When TOL is connected to V<sub>CC</sub>, the reset pulse generator forces the reset outputs to active states as V<sub>CC</sub> falls below 4.5V (4.37V typical).

**TD**: Time-out Delay, TD is a three level input to select three different time-out periods. The time-out period is set by the TD input to be 150ms with TD connected to GND, 600ms with TD left floating, and 1.2 seconds with TD connected to V<sub>CC</sub>.

## PIN FUNCTIONS

**$\overline{RST}$ :** Open drain logic output for  $\mu P$  reset control. The LTC1232 provides three ways to generate  $\mu P$  reset. First, when  $V_{CC}$  falls below  $V_{CC}$  trip point (4.75V with TOL = GND and 4.5V with TOL =  $V_{CC}$ ),  $\overline{RST}$  goes active low. After  $V_{CC}$  returns to 5V, the reset pulse generator forces  $\overline{RST}$  to remain active low for a minimum of 250ms. Second, when the watchdog timer is not serviced prior to a selected time-out period, the reset pulse generator also forces  $\overline{RST}$  to active low for a minimum of 250ms and repeats for every time-out period. Third and the last, when the PB  $\overline{RST}$  pin stays active low for a minimum of 40ms,  $\overline{RST}$  becomes active low. The  $\overline{RST}$  output will remain active low for a

minimum of 250ms from the moment the push-button reset input is released from logic low level.

**$RST$ :**  $RST$  is an active high logic output. It is the inverse of  $\overline{RST}$ .

**$\overline{ST}$ :** Logic input to reset the watchdog timer. Driving  $\overline{ST}$  either high or low longer than the time-out period set by the TD input, forces the reset outputs to active states for a minimum of 250ms. The timer resets itself and begins to time-out again with each high to low transition on the  $\overline{ST}$  input (see Figure 2).

## APPLICATIONS INFORMATION

### Power Monitoring

The LTC1232 uses a bandgap voltage reference and a precision voltage comparator, C1, to monitor the 5V supply input on  $V_{CC}$  (see BLOCK DIAGRAM). When  $V_{CC}$  falls below the  $V_{CC}$  trip point (4.62V typical with TOL = GND and 4.37V typical with TOL =  $V_{CC}$ ), the reset outputs are forced to active states. The  $V_{CC}$  trip point accounts for a 5% or 10% variation on  $V_{CC}$ , so the reset outputs become active when  $V_{CC}$  falls below the  $V_{CC}$  trip point. On power-up, the reset signals are held in active states for a minimum of 250ms after the  $V_{CC}$  trip point is reached to allow the power supply and microprocessor to stabilize. On power-down, the  $\overline{RST}$  signal remains active low even with  $V_{CC}$  as low as 1V. This capability helps hold the

microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the  $\overline{RST}$  signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at  $V_{CC}$  pin do not activate the reset outputs. Response time is typically 10 $\mu s$ . To help prevent mittriggering due to transient loads,  $V_{CC}$  pin should be bypassed with a 0.1 $\mu F$  capacitor with the leads trimmed as short as possible.

### Push-Button Reset

The LTC1232 provides a logic input pin,  $\overline{PB RST}$ , for direct connection to a push-button. This push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When

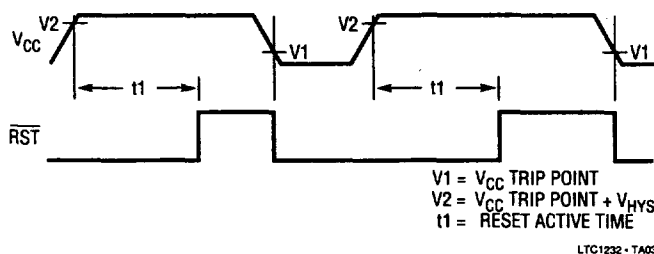


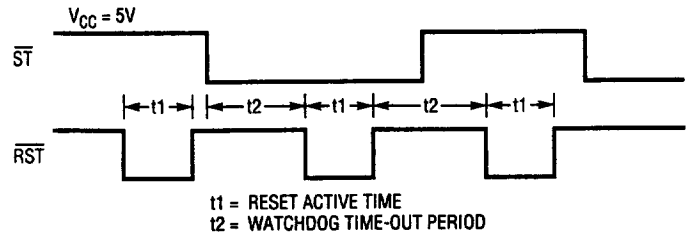
Figure 1. Reset Active Time

## APPLICATIONS INFORMATION

this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset signals will remain active for a minimum of 250ms from the moment the push-button reset input is released from logic low level (see TIMING DIAGRAM).

### Watchdog Timer

The LTC1232 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not stimulate the strobe input,  $\overline{ST}$ , within a selected time-out period, the reset outputs are forced to active states for a minimum of 250ms. The time-out period is selected by the Time-out Delay input, TD, to be 150ms with TD connected to GND, 600ms with TD left floating, and 1.2 seconds with TD connected to  $V_{CC}$ . The 1.2 second time-out period is adequate for many systems to serve the watchdog timer immediately after a reset. Figure 2 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as



LTC1232 - TA04

**Figure 2. Watchdog Time-Out Period and Reset Active Time**

soon as the reset outputs are inactive. When a high-to-low transition occurs at the  $\overline{ST}$  pin prior to time-out, the watchdog time is reset and begins to time-out again. To ensure the watchdog time does not time-out, a high-to-low transition on the  $\overline{ST}$  pin must occur at or less than the minimum time-out period. If the input to the  $\overline{ST}$  pin remains either high or low, reset pulses will be issued for every time-out period selected by the TD pin. The watchdog timer is disabled when  $V_{CC}$  falls below the  $V_{CC}$  trip point.