

# PROCESS CP667

## Small Signal Transistor

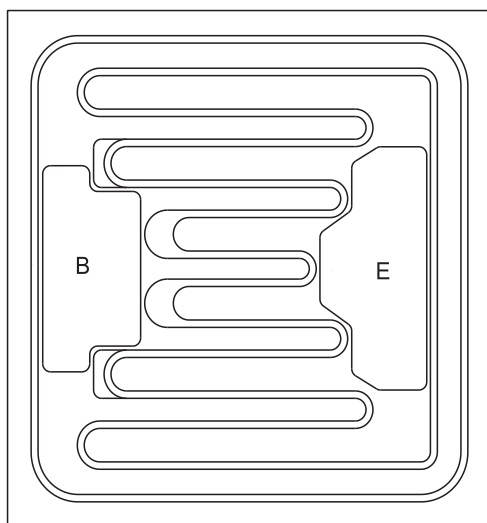
[查询"CP667"供应商](#) PNP Saturated Switch Transistor Chip

**Central**<sup>TM</sup>  
Semiconductor Corp.

### PROCESS DETAILS

|                          |                  |
|--------------------------|------------------|
| Process                  | EPITAXIAL PLANAR |
| Die Size                 | 31 x 31 MILS     |
| Die Thickness            | 9.0 MILS         |
| Base Bonding Pad Area    | 5.9 x 11.8 MILS  |
| Emitter Bonding Pad Area | 6.5 x 13.8 MILS  |
| Top Side Metalization    | Al - 30,000Å     |
| Back Side Metalization   | Au - 15,000Å     |

### GEOMETRY



BACKSIDE COLLECTOR

R0

### GROSS DIE PER 4 INCH WAFER

11,300

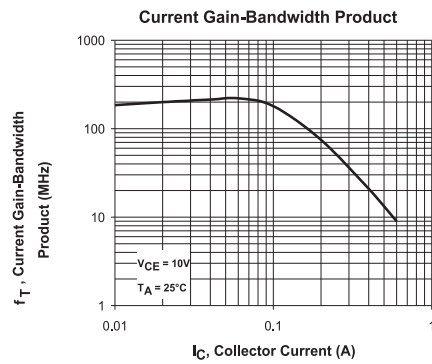
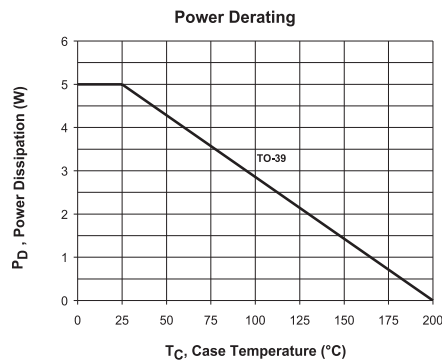
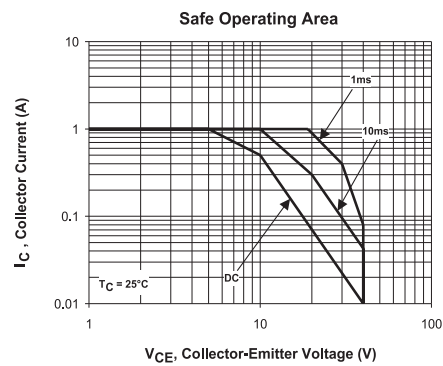
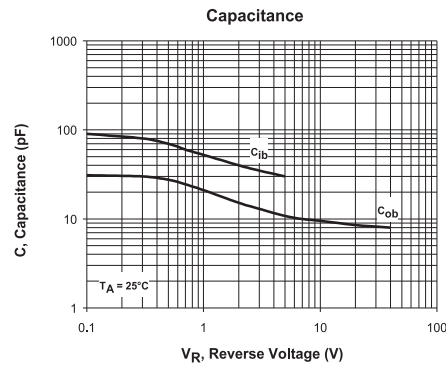
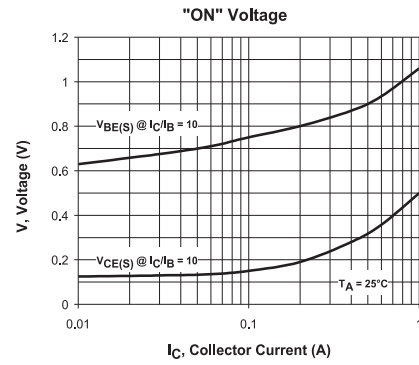
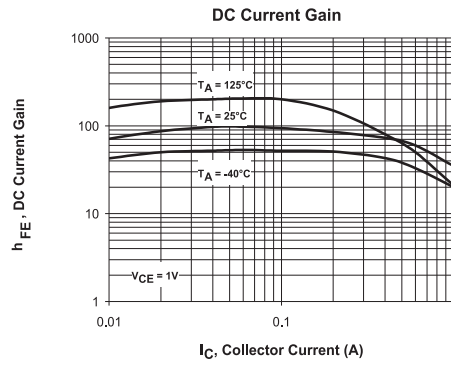
### PRINCIPAL DEVICE TYPES

2N3467

2N3468

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