High frequency operational amplifier

NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

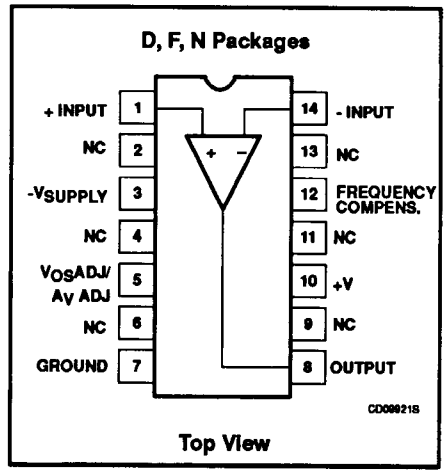
FEATURES

- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vμs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0 to +70°C	NE5539N	0405
14-Pin Plastic SO	0 to +70°C	NE5539D	0175
14-Pin Cerdip	0 to +70°C	NE5539F	0581
14-Pin Cerdip	-55 to +125°C	SE5539F	0581

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2] F package N package D package	 1.17 1.45 0.99	 W W W
T_A	Operating temperature range NE SE	 0 to 70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

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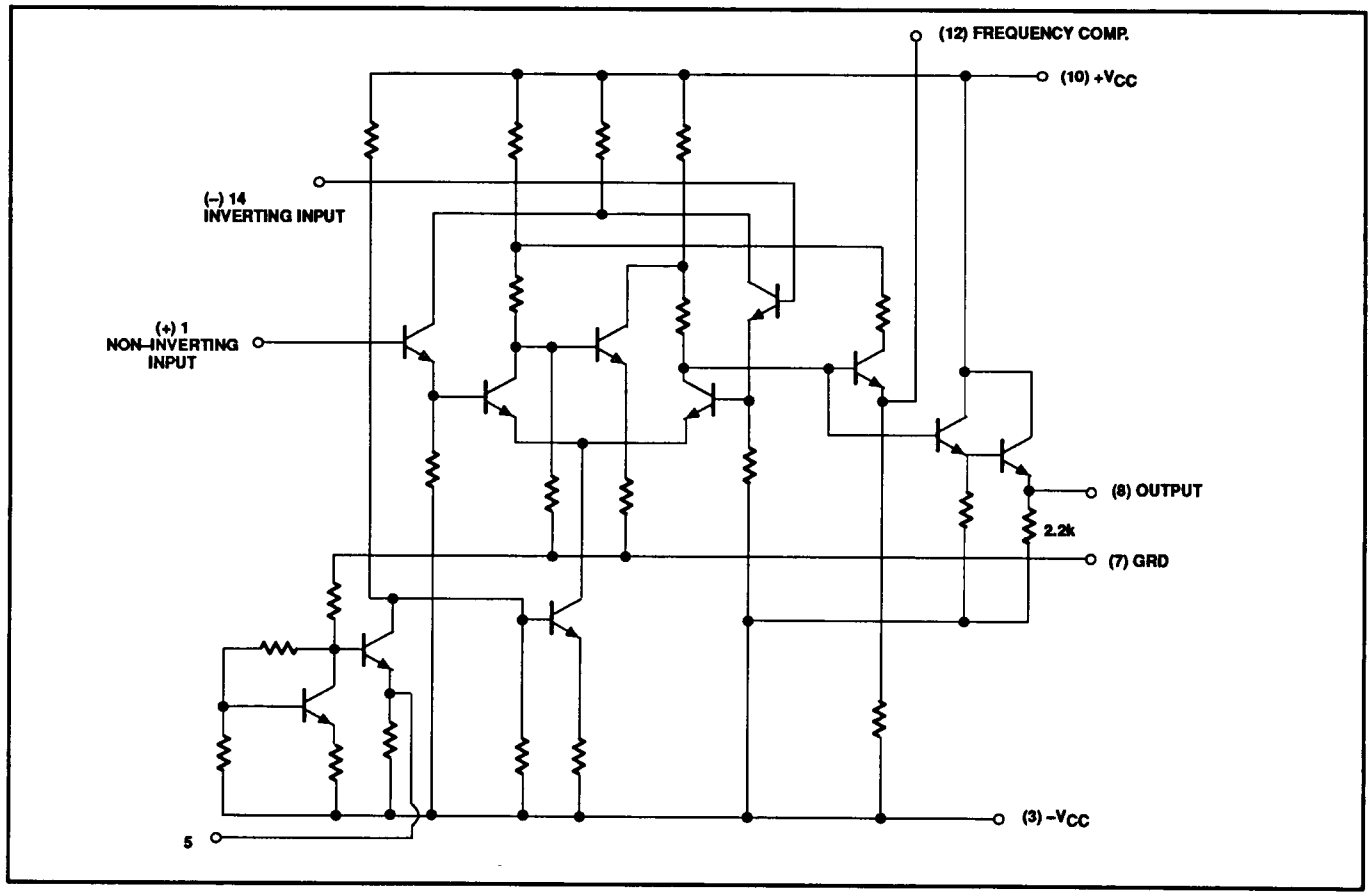
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to $-V_{CC}$	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	R_L = 25Ω to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		R_L = 25Ω to GND T_A = 25°C	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					V
I_{CC+}	Positive supply current	V_O = 0, R_1 = ∞, Over temp			14	18		2.8	3.5	mA
		V_O = 0, R_1 = ∞, T_A = 25°C			14	17		14	18	mA
I_{CC-}	Negative supply current	V_O = 0, R_1 = ∞, Over temp			11	15		2.8	3.5	mA
		V_O = 0, R_1 = ∞, T_A = 25°C			11	14		11	15	mA
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V, Over temp			300	1000				µV/V
		ΔV_{CC} = ±1V, T_A = 25°C						200	1000	µV/V
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V, R_L = 150Ω to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V R_L = 2Ω to GND	Over temp							dB
			T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, -2.0V R_L = 2Ω to GND	Over temp	46		60				dB
			T_A = 25°C	48	53	58				

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539			UNITS
					MIN	TYP	MAX	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				T_A = 25°C		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				T_A = 25°C		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				T_A = 25°C		4	10	
CMRR	Common-mode rejection ratio	V_{CM} = ±1.3V, R_S = 100Ω			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				T_A = 25°C		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				T_A = 25°CmA		8	10	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V		Over temp		300	1000	µV/V
				T_A = 25°C				
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			T_A = 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

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AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, R_L = 150Ω to GND and 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7, V_O = 0.1 V_{P-P}		1200			1200		MHz
	Small signal bandwidth	A_{CL} = 2, R_L = 150Ω[1]		110			110		MHz
t_S	Settling time	A_{CL} = 2, R_L = 150Ω[1]		15			15		ns
SR	Slew rate	A_{CL} = 2, R_L = 150Ω[1]		600			600		V/µs
t_{PD}	Propagation delay	A_{CL} = 2, R_L = 150Ω[1]		7			7		ns
	Full power response	A_{CL} = 2, R_L = 150Ω[1]		48			48		MHz
	Full power response	A_V = 7, R_L = 150Ω[1]		20			20		MHz
	Input noise voltage	R_S = 50Ω, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

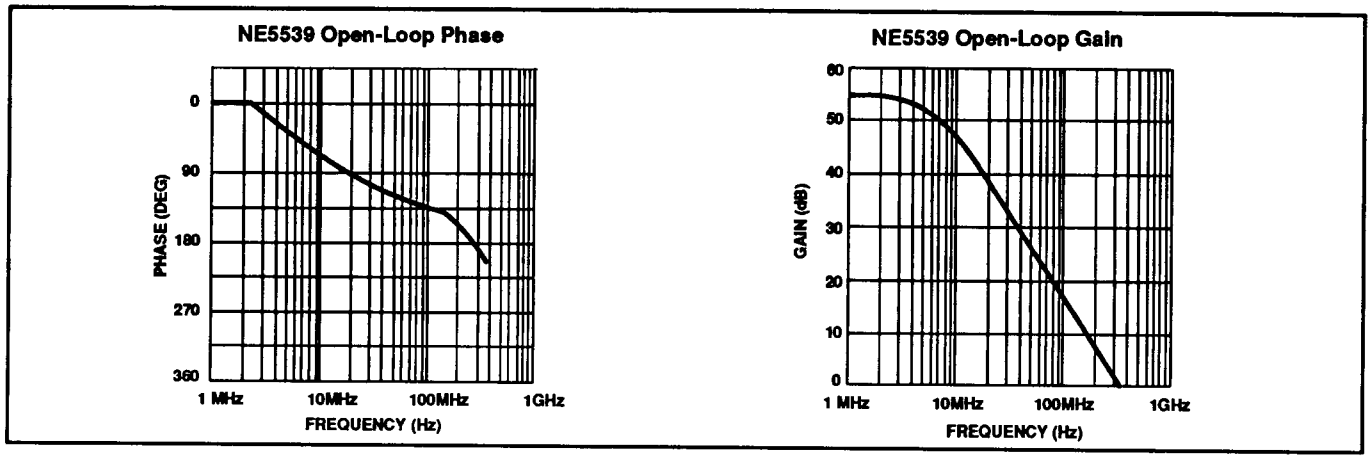
AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, R_L = 150Ω to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7		700		MHz
	Small signal bandwidth	A_{CL} = 2[1]		120		MHz
t_S	Settling time	A_{CL} = 2[1]		23		ns
SR	Slew rate	A_{CL} = 2[1]		330		V/µs
t_{PD}	Propagation delay	A_{CL} = 2[1]		4.5		ns
	Full power response	A_{CL} = 2[1]		20		MHz

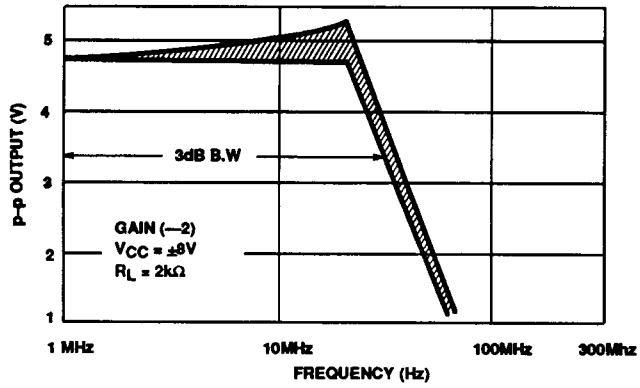
NOTES:
1. External compensation.

TYPICAL PERFORMANCE CURVES

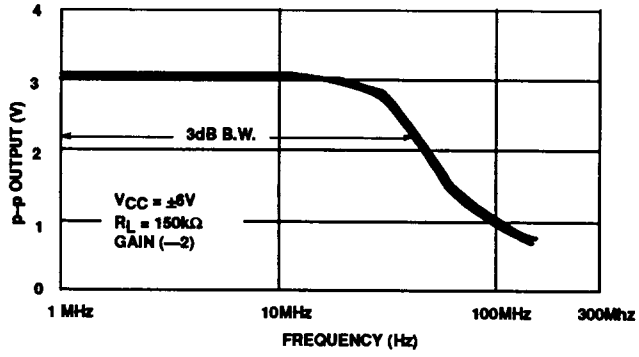


TYPICAL PERFORMANCE CURVES (Continued)

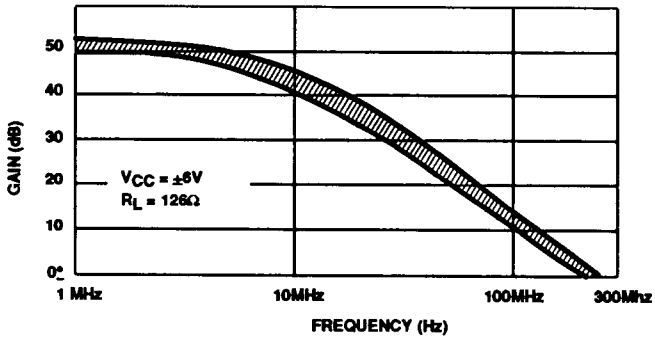
Power Bandwidth (SE)



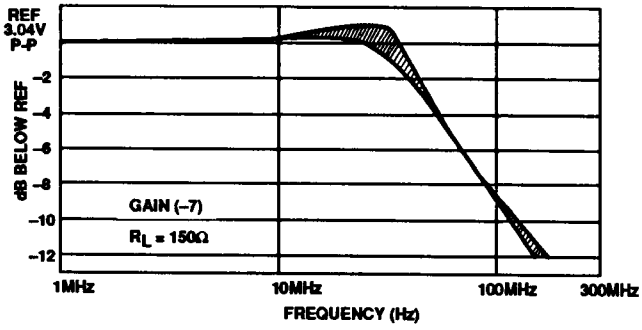
Power Bandwidth (NE)



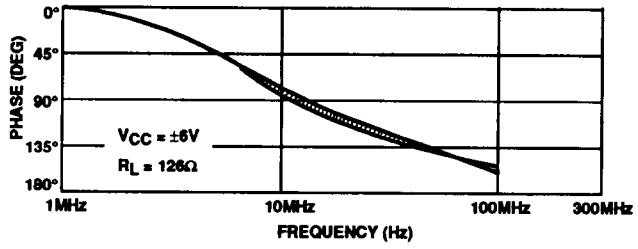
SE5539 Open-Loop Gain vs Frequency



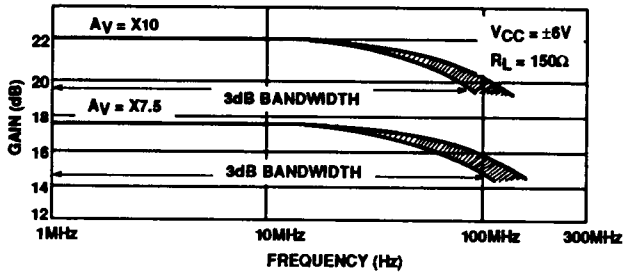
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency

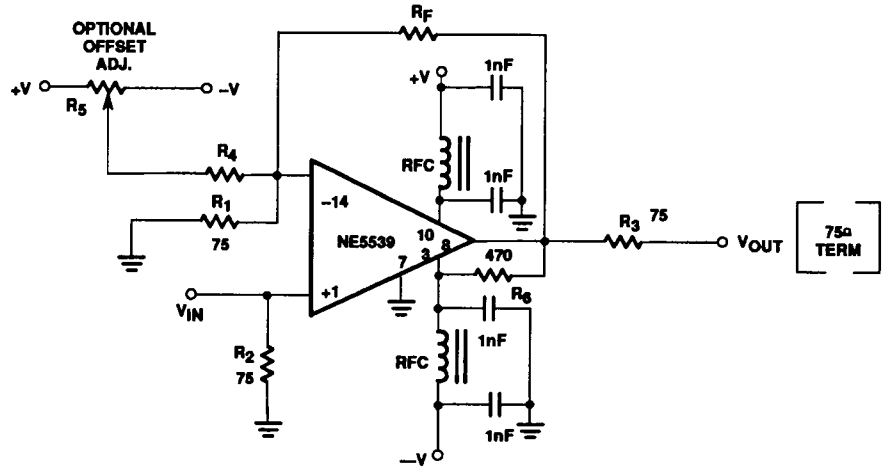


NOTE:

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in 1.

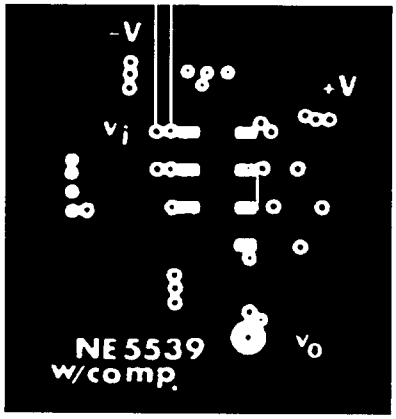


R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36K 5% CARBON

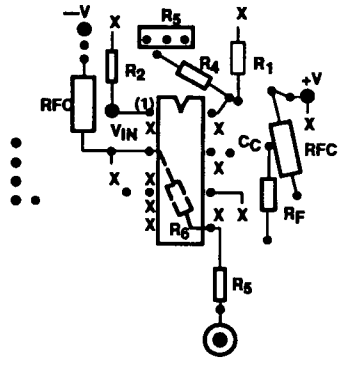
R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)



Component Side (Component Layout)



Bottom Plane Copper[1]

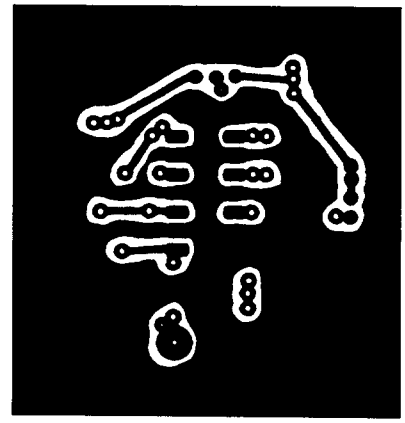


Figure 1. 28dB Non-Inverting Amp Sample PC Layout

High frequency operational amplifier

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75W input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

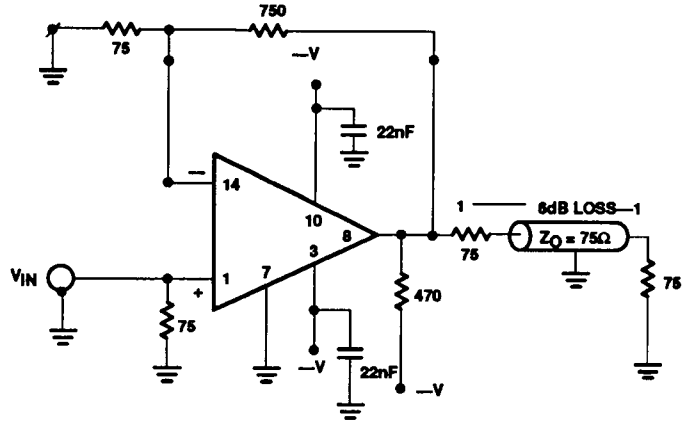


Figure 2. NE5539 Video Amplifier

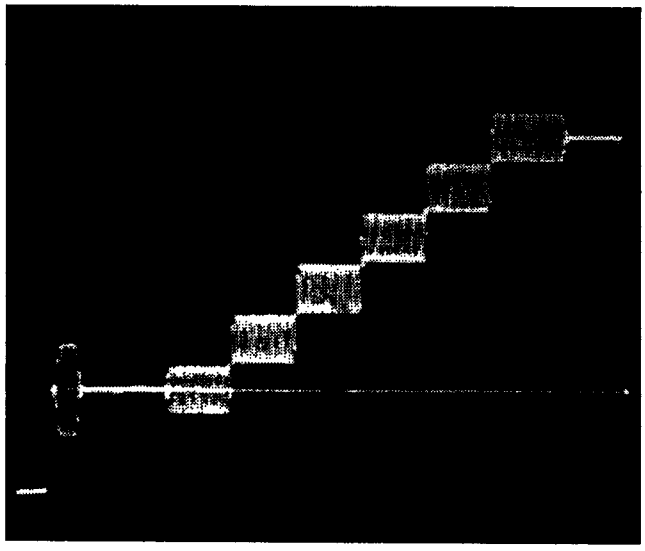


Figure 3. Input Signal

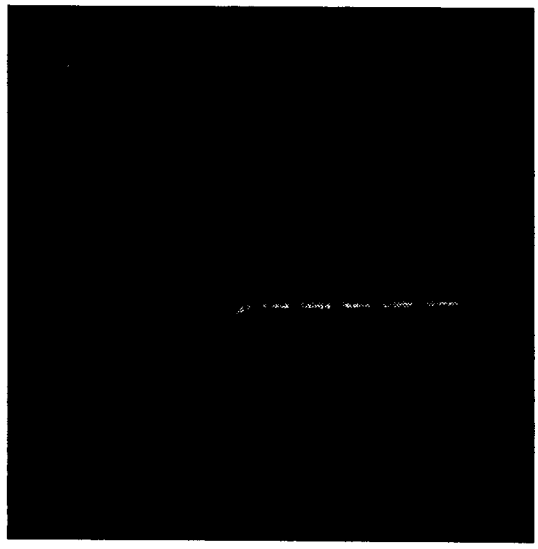


Figure 4. Differential Gain <0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

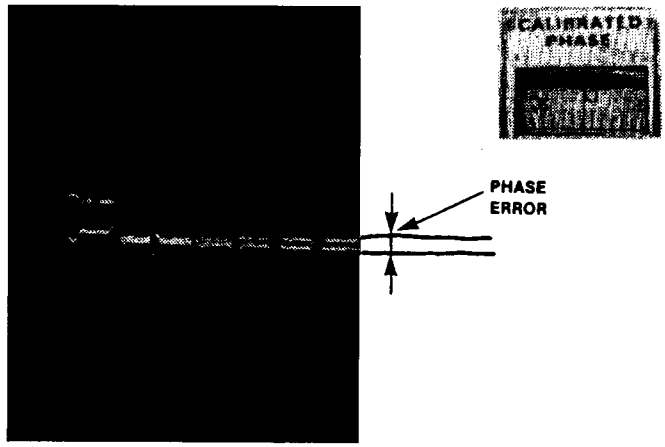


Figure 5. Differential Gain +0.1°

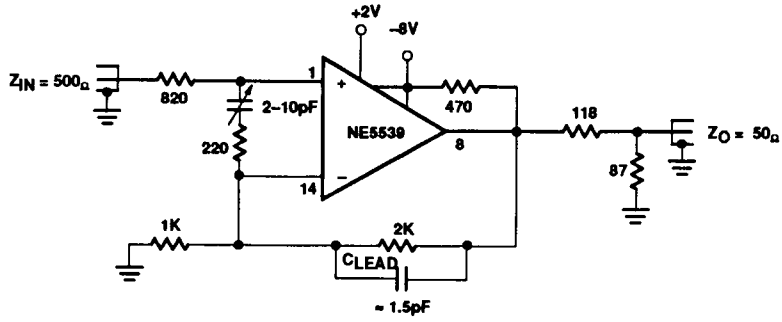


Figure 6. Non-Inverting Follower

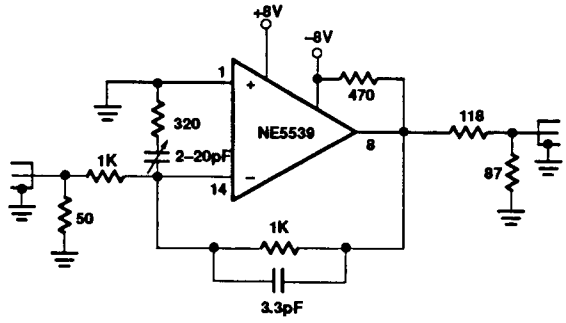


Figure 7. Inverting Follower

Packaging Information

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SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

Packaging Information

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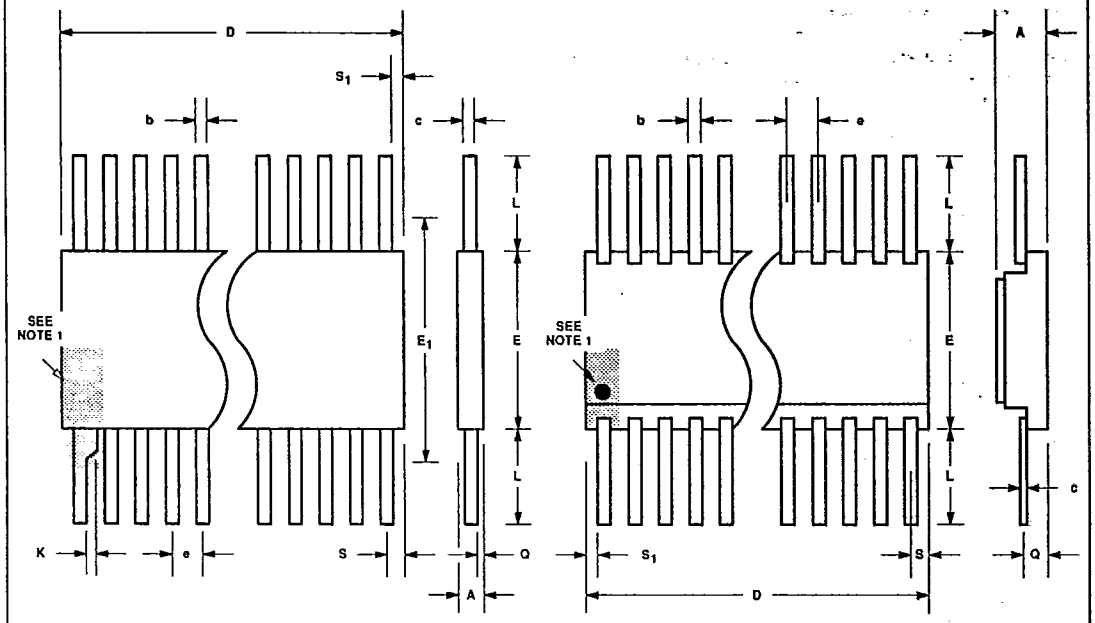
CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1

Configuration 2

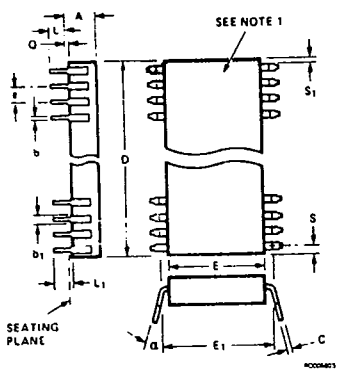
NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counter-clockwise (as viewed from the top of the device.
2. This dimension allows for off-center lid, meniscus and glass overrun.
3. The reference pin spacing is 0.050 between center-lines. Each pin centerline is located within ±0.005 of its longitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish

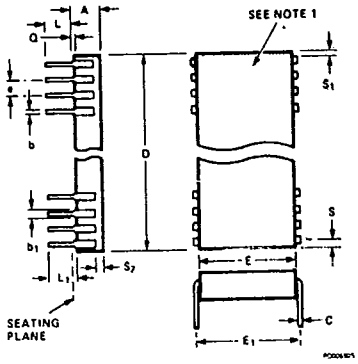
OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	–	1.330	2
E	0.620	0.660	
e	0.050BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	–	0.045	5
S1	0.005	–	5

Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1



Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

Packaging Information

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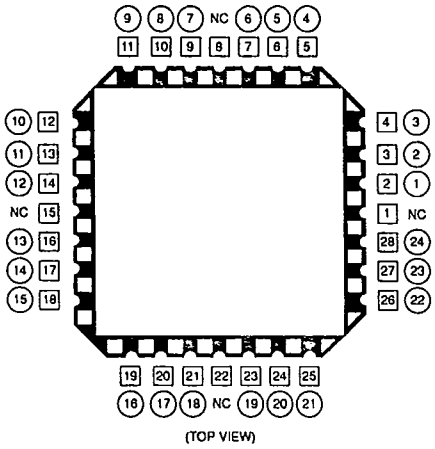
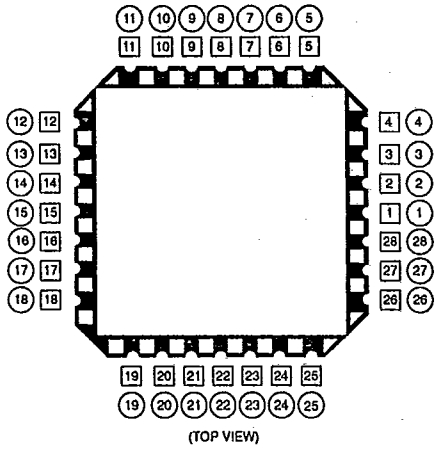
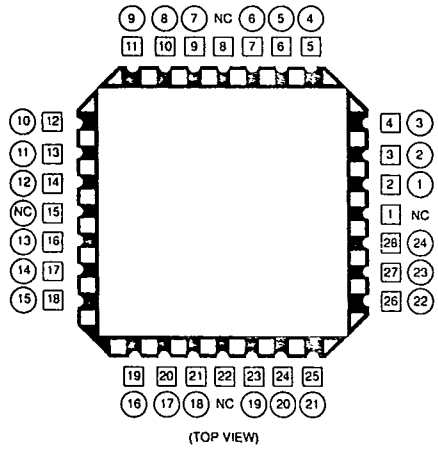
LEADLESS CHIP CARRIER (LLCC) PINOUTS



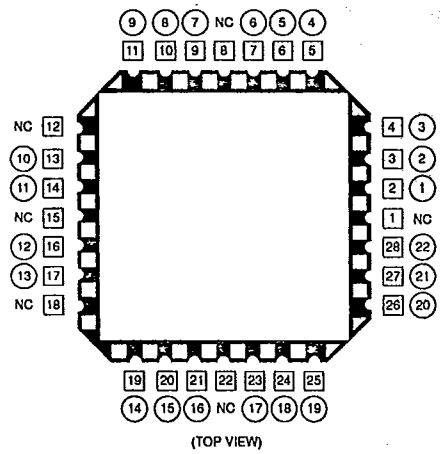
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



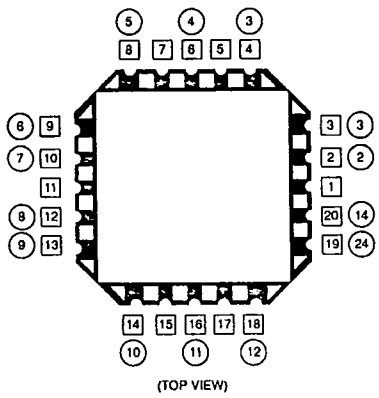
22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect

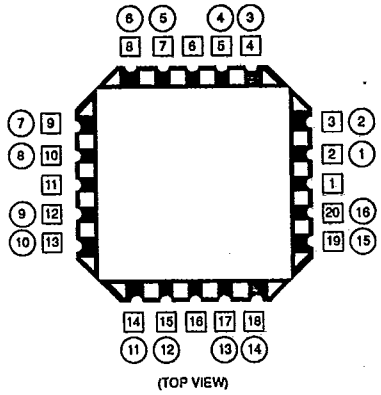
Packaging Information

T-90-20

LEADLESS CHIP CARRIER (LLCC) PINOUTS



14-Pin Logic Pinout for 20 Terminal Chip Carrier



16-Pin Logic Pinout for 20 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number