Five/Ten Output Clock Generator/Jitter Cleaner With Integrated Dual VCOs

Check for Samples: CDCE62005

FEATURES

- Frequency Synthesizer With PLL/VCO and Partially Integrated Loop Filter.
- Fully Configurable Outputs Including Frequency, Output Format, and Output Skew.
- Smart Input Multiplexer Automatically Switches Between One of Three Reference Inputs.
- Multiple Operational Modes Include Clock Generation via Crystal, SERDES Startup Mode, Jitter Cleaning, and Oscillator Holdover Mode
- Integrated EEPROM Determines Device Configuration at Power-up
- Excellent Jitter Performance
- Integrated Frequency Synthesizer including PLL, Multiple VCOs, and Loop Filter:
  - Full Programmability Facilitates Phase Noise Performance Optimization Enabling Jitter Cleaner Mode.
  - Programmable Charge Pump Gain and Loop Filter Settings
  - Unique Dual-VCO Architecture Supports a Wide Tuning Range 1.750 GHz–2.356 GHz
- Universal Output Blocks Support up to 5 Differential, 10 Single-ended, or Combinations of Differential or Single-ended:
  - 0.35 ps RMS (10 kHz to 20 MHz) Output Jitter Performance
  - Low Output Phase Noise: –130 dBc/Hz at 1 MHz offset, F_c = 491.52 MHz
  - Output Frequency Ranges From 4.25 MHz to 1.175 GHz in Synthesizer Mode
  - Output Frequency up to 1.5 GHz in Fan-out Mode
  - LVPECL, LVDS, LVCMOS, and Special High Output Swing Modes
  - Independent Output Dividers Support Divide Ratios from 1–80, Non-continuous values supported.
  - Independent Coarse Skew Control on all Outputs, The coarse skew control does not operate for reference input frequencies less than 1 MHz
- Flexible Inputs With Innovative Smart Multiplexer Feature:
  - Two Universal Differential Inputs Accept Frequencies in the Range of 40 kHz to 1500 MHz (LVPECL), 800 MHz (LVDS), or 250 MHz (LVCMOS).
  - One Auxiliary Input Accepts Crystals in the Range of 2 MHz–42 MHz
  - Clock Generator Mode Using Crystal Input.
  - Smart Input Multiplexer can be Configured to Automatically Switch Between Highest Priority Clock Source Available Allowing for Fail-safe Operation and Holdover Modes.
- Typical Power Consumption 1.7W (See Table 44) at 3.3V
- Integrated EEPROM Stores Default Settings; Therefore, The Device Can Power up in a Known, Predefined State.
- Offered in QFN-48 Package
- ESD Protection Exceeds 2kV HBM
- Industrial Temperature Range –40°C to 85°C

APPLICATIONS

- Data Converter and Data Aggregation Clocking
- Wireless Infrastructure
- Switches and Routers
- Medical Electronics
- Military and Aerospace
- Industrial
- Clock Generation and Jitter Cleaning

DESCRIPTION

The CDCE62005 is a high performance clock generator and distributor featuring low output jitter, a high degree of configurability via a SPI interface, and programmable start up modes determined by on-chip EEPROM. Specifically tailored for clocking data converters and high-speed digital signals, the CDCE62005 achieves jitter performance well under 1 ps RMS(1). It incorporates a synthesizer block with partially integrated loop filter, a clock distribution block including programmable output formats, and an input block featuring an innovative smart multiplexer. The clock distribution block includes five individually programmable outputs that can be configured to provide different combinations of output formats (LVPECL, LVDS, LVCMOS). Each output can also be programmed to a unique output frequency (ranging from 125 kHz to 1.5 GHz (2)) and skew relationship via a programmable delay block. If all outputs are configured in single-ended mode (e.g., LVCMOS), the CDCE62005 supports up to ten outputs. Each output can select one of four clock sources to condition and distribute including any of the three clock inputs or the output of the frequency synthesizer. The input block includes two universal differential inputs which support frequencies in the range of 80 kHz to 500 MHz and an auxiliary input that can be configured to connect to an external crystal via an on board oscillator block. The smart input multiplexer has two modes of operation, manual and automatic. In manual mode, the user selects the synthesizer reference via the SPI interface. In automatic mode, the input multiplexer will automatically select between the highest priority input clock available.

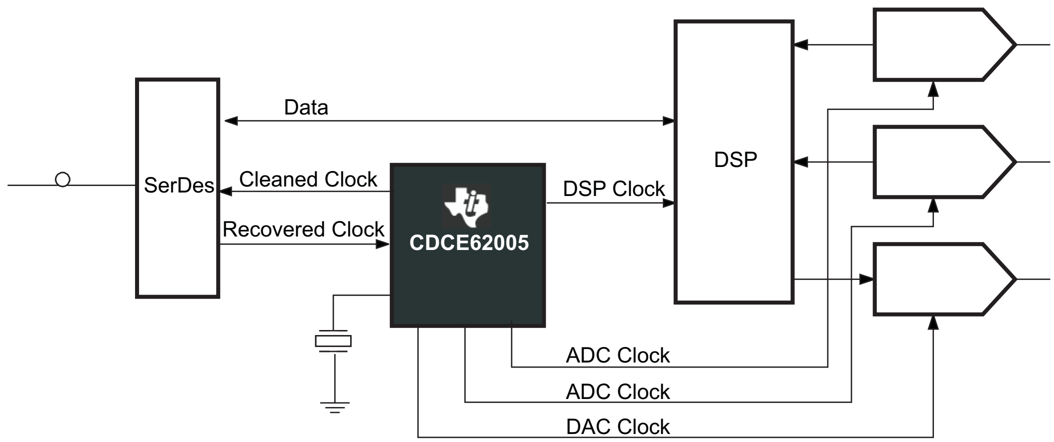


Figure 1. CDCE62005 Application Example

(1) 10 kHz to 20 MHz integration bandwidth.
(2) Frequency range depends on operational mode and output format selected.

DEVICE INFORMATION

PACKAGE

The CDCE62005 is packaged in a 48-Pin Plastic Quad Flatpack Package with enhanced bottom thermal pad for heat dissipation. The Texas Instruments Package Designator is: **RGZ (S-PQFP-N48)**

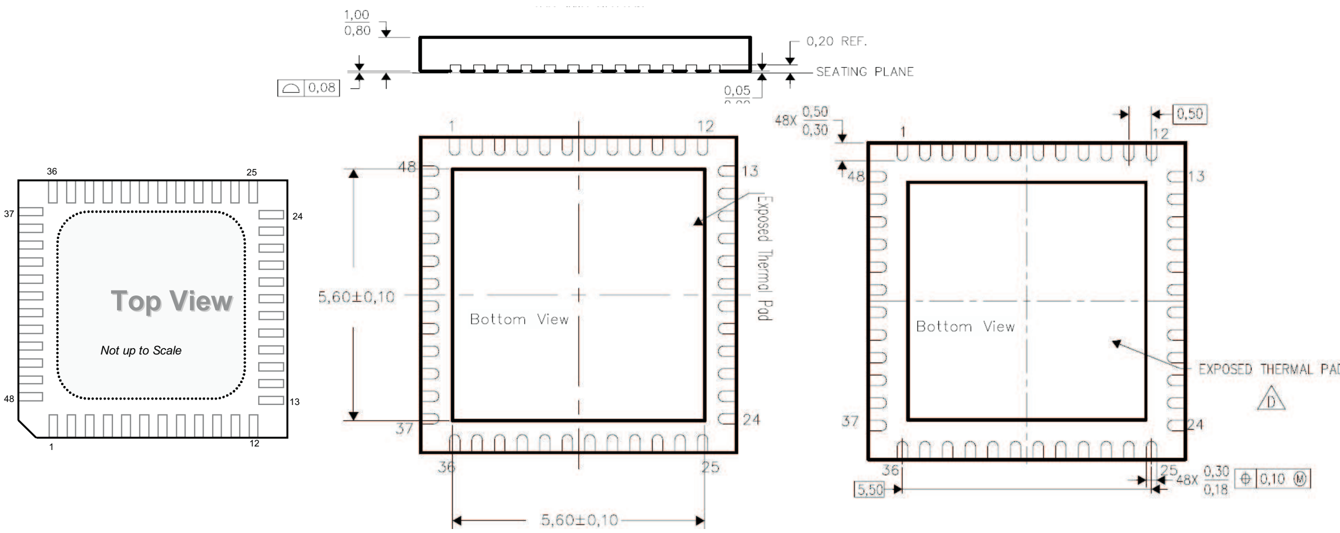


Figure 2. 48-Pin QFN Package Outline

PIN FUNCTIONS(1)

PIN		TYPE	DESCRIPTION
NAME	QFN		
VCC_OUT	8, 11, 18, 21, 26, 29, 32	Power	3.3V Supply for the Output Buffers and Output Dividers
VCC_AUXOUT	15	Power	3.3V to Power the AUX_OUT circuitry
VCC1_PLL	5	A. Power	3.3V PLL Supply Voltage for the PLL circuitry. (Filter Required)
VCC2_PLL	39, 42	A. Power	3.3V PLL Supply Voltage for the PLL circuitry. (Filter Required)
VCC_VCO	34, 35	A. Power	3.3V VCO Input Buffer and Circuitry Supply Voltage. (Filter Required)
VCC_IN_PRI	47	A. Power	3.3V References Input Buffer and Circuitry Supply Voltage.
VCC_IN_SEC	1	A. Power	3.3V References Input Buffer and Circuitry Supply Voltage.
VCC_AUXIN	44	A. Power	3.3V Crystal Oscillator Input Circuitry.
GND_VCO	36	Ground	Ground that connects to VCO Ground. (VCO_GND is shorted to GND)
GND	PAD	Ground	Ground is on Thermal PAD. See Layout recommendation
SPI_MISO	22	OD	In SPI Mode it is an Open Drain Output and it functions as a Master In Slave Out as a serial Control Data Output to CDCE62005 .
SPI_LE	25	I	LVCMOS input, control Latch Enable for Serial Programmable Interface (SPI), with Hysteresis in SPI Mode. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level “1”.
SPI_CLK	24	I	LVCMOS input, serial Control Clock Input for the SPI bus interface, with Hysteresis. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level “1”.
SPI_MOSI	23	I	LVCMOS input, Master Out Slave In as a serial Control Data Input to **CDCE62005** for the SPI bus interface. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level “1”.
TEST_MODE	33	I	This pin should be tied high or left unconnected.

(1) Note: The internal memory (EEPROM and RAM) are sourced from various power pins. All VCC connections must be powered for proper functionality of the device.

PIN FUNCTIONS [(1)] (continued)

PIN		TYPE	DESCRIPTION
NAME	QFN		
REF_SEL	31	I	If Auto Reference Select Mode is OFF this Pin acts as External Input Reference Select Pin; The REF_SEL signal selects one of the two input clocks: REF_SEL [1]: PRI_IN is selected; REF_SEL [0]: SEC_IN is selected; The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". If Auto Reference Select Mode in ON this Pin not used.
Power_Down	12	I	Active Low. Power down mode can be activated via this pin. See Table 15 for more details. The input has an internal 150-kΩ pull-up resistor if left unconnected it will default to logic level "1". SPI_LE has to be HIGH in order for the rising edge of Power_Down signal to load the EEPROM.
SYNC	14	I	Active Low. Sync mode can be activated via this pin. See Table 15 for more details. The input has an internal 150-kΩ, pull-up resistor if left unconnected it will default to logic level "1".
AUX IN	43	I	Auxiliary Input is a single ended input including an on-board oscillator circuit so that a crystal may be connected.
AUX OUT	13	O	Auxiliary Output LVCMOS level that can be programmed via SPI interface to be driven by Output 2 or Output 3.
PRI REF+	45	I	Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Primary Reference Clock,
PRI REF–	46	I	Universal Input Buffer (LVPECL, LVDS) negative input for the Primary Reference Clock. In case of LVCMOS signaling Ground this pin.
SEC REF+	3	I	Universal Input Buffer (LVPECL, LVDS, LVCMOS) positive input for the Secondary Reference Clock,
SEC REF–	2	I	Universal Input Buffer (LVPECL, LVDS,) negative input for the Secondary Reference Clock.
TESTOUTA	30	Analog	Analog Test Point for Use for TI Internal Testing. Pull Down to GND Via a 1kΩs Resistor.
REG_CAP1	4	Analog	Capacitor for the internal Regulator. Connect to a 10uF Capacitor (Y5V)
REG_CAP2	38	Analog	Capacitor for the internal Regulator. Connect to a 10uF Capacitor (Y5V)
VBB	48	Analog	Capacitor for the internal termination Voltage. Connect to a 1uF Capacitor (Y5V)
EXT_LFP	40	Analog	External Loop Filter Input Positive
EXT_LFN	41	Analog	External Loop Filter Input Negative.
PLL_LOCK	37	AI/O	Output that indicates PLL Lock Status. See Figure 37.
U0P:U0N U1P:U1N: U2P:U2N U3P:U3N U4P:U4N	27, 28 19, 20 16,17 9, 10 6, 7	O	The Main outputs of **CDCE62005** are user definable and can be any combination of up to 5 LVPECL outputs, 5 LVDS outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI interface. The power-up setting is EEPROM configurable.

FUNCTIONAL DESCRIPTION

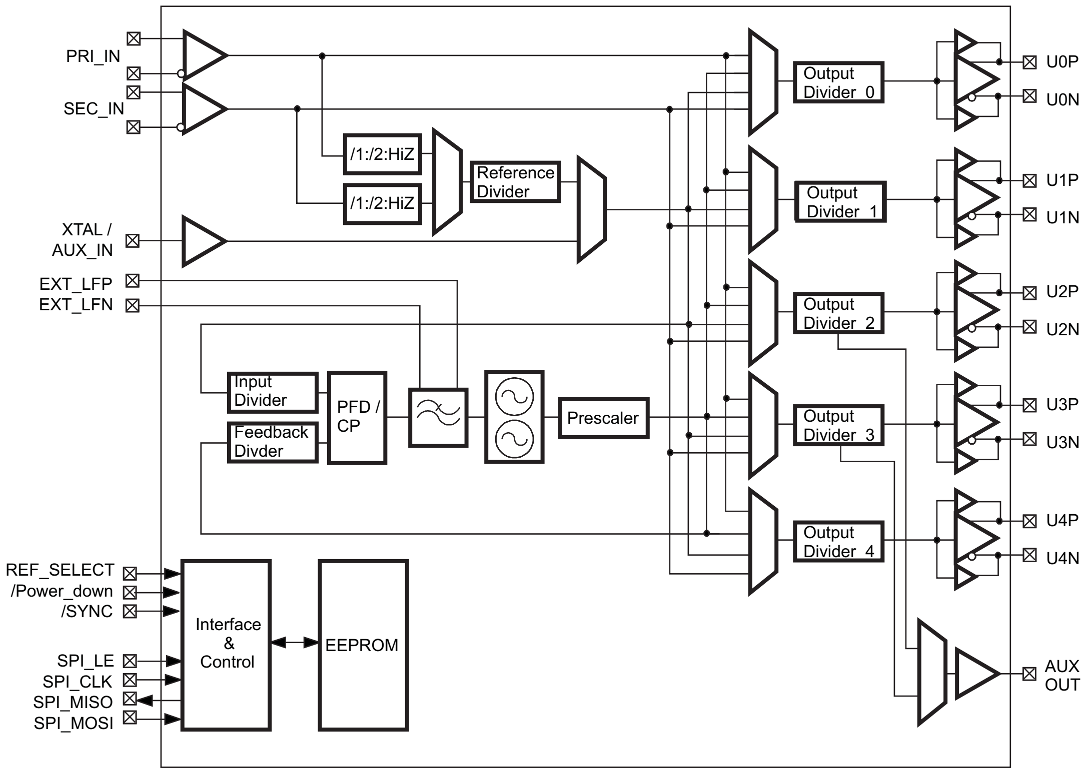


Figure 3. CDCE62005 Block Diagram

The CDCE62005 comprises of four primary blocks: the interface and control block, the input block, the output block, and the synthesizer block. In order to determine which settings are appropriate for any specific combination of input/output frequencies, a basic understanding of these blocks is required. The interface and control block determines the state of the CDCE62005 at power-up based on the contents of the on-board EEPROM. In addition to the EEPROM, the SPI port is available to configure the CDCE62005 by writing directly to the device registers after power-up. The input block selects which of the three input ports is available for use by the synthesizer block and buffers all clock inputs. The output block provides five separate clock channels that are fully programmable and configurable to select and condition one of four internal clock sources. The synthesizer block multiplies and filters the input clock selected by the input block.

NOTE

This Section of the data sheet provides a high-level description of the features of the CDCE62005 for purpose of understanding its capabilities. For a complete description of device registers and I/O, please refer to the Device Configuration Section.

Interface and Control Block

The CDCE62005 is a highly flexible and configurable architecture and as such contains a number of registers so that the user may specify device operation. The contents of nine 28-bit wide registers implemented in static RAM determine device configuration at all times. On power-up, the CDCE62005 copies the contents of the EEPROM into the RAM and the device begins operation based on the default configuration stored in the EEPROM. Systems that do not have a host system to communicate with the CDCE62005 use this method for device configuration. The CDCE62005 provides the ability to lock the EEPROM; enabling the designer to implement a fault tolerant design. After power-up, the host system may overwrite the contents of the RAM via the SPI (Serial Peripheral Interface) port. This enables the configuration and reconfiguration of the CDCE62005 during system operation. Finally, the device offers the ability to copy the contents of the RAM into EEPROM, if the EEPROM is unlocked.

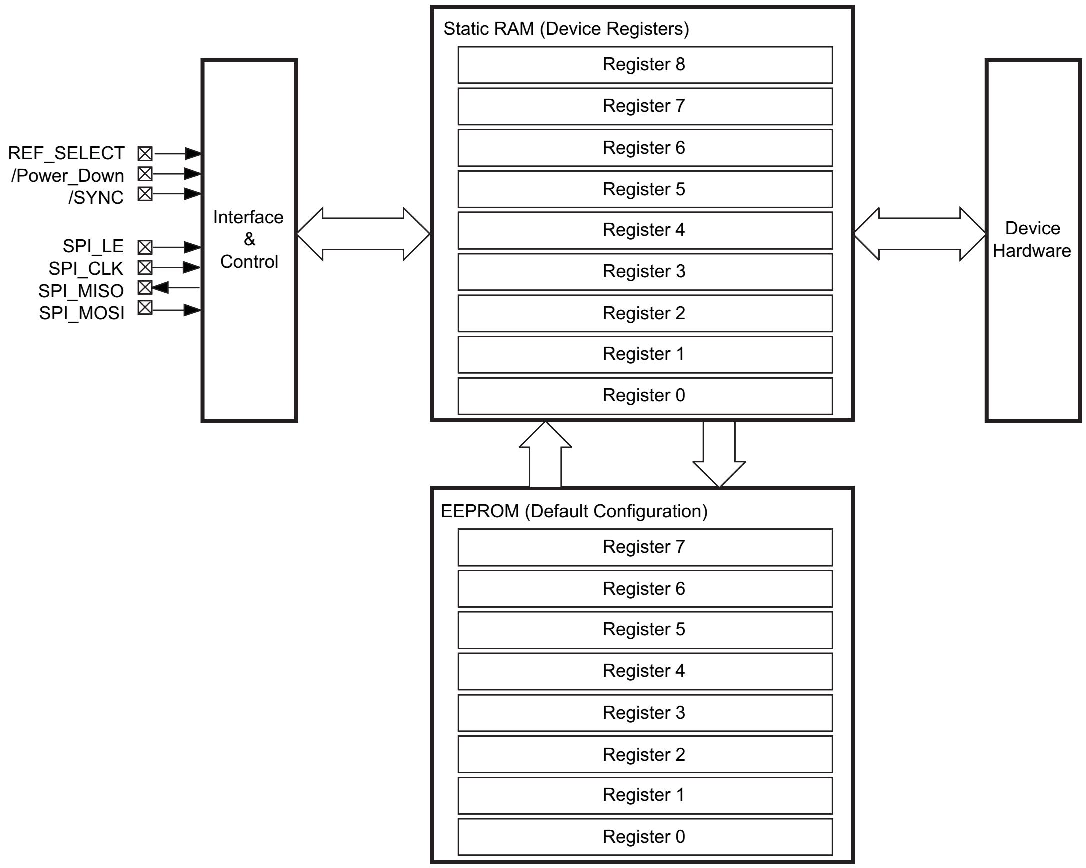


Figure 4. CDCE62005 Interface and Control Block

Input Block

The Input Block includes a pair of Universal Input Buffers and an Auxiliary Input. The Input Block buffers the incoming signals and facilitates signal routing to the Internal Clock Distribution bus and the Synthesizer Block via the smart multiplexer (called the Smart MUX). The Internal Clock Distribution Bus connects to all output blocks discussed in the next section. Therefore, a clock signal present on the Internal Clock Distribution bus can appear on any or all of the device outputs. The CDCE62005 routes the PRI_IN and SEC_IN inputs directly to the Internal Clock Distribution Bus. Additionally, it can divide these signals via the dividers present on the inputs and output of the first stage of the Smart MUX.

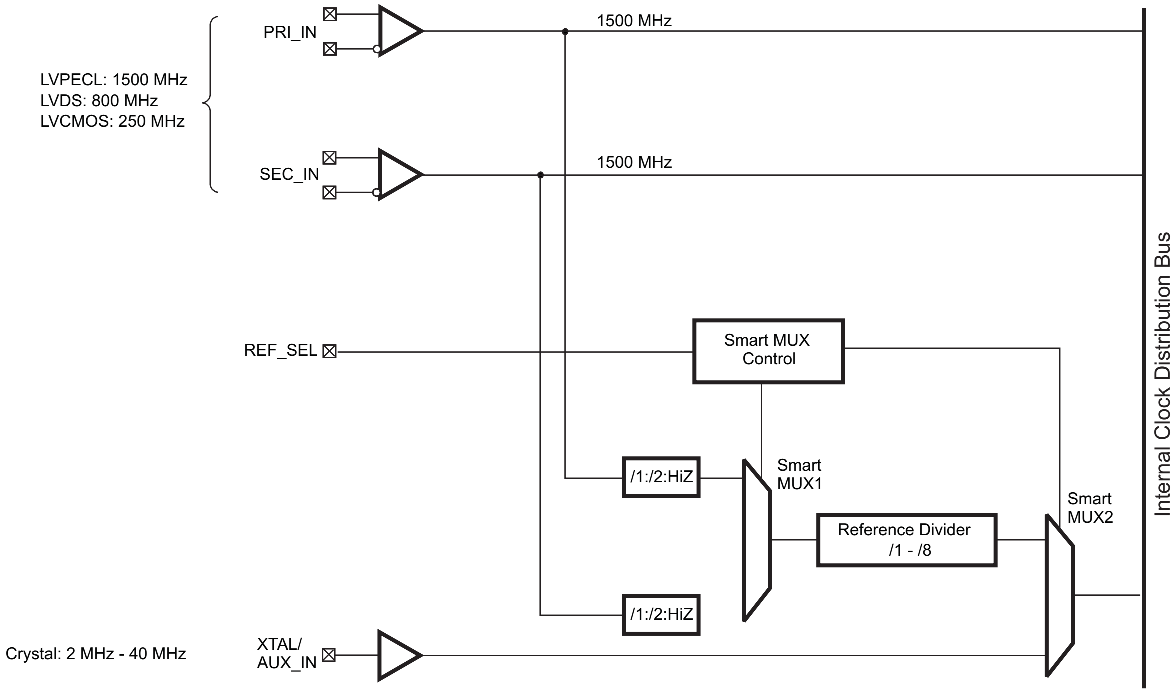


Figure 5. CDCE62005 Input Block

Output Block

Each of the five identical output blocks incorporates an output multiplexer, a clock divider module, and a universal output array as shown.

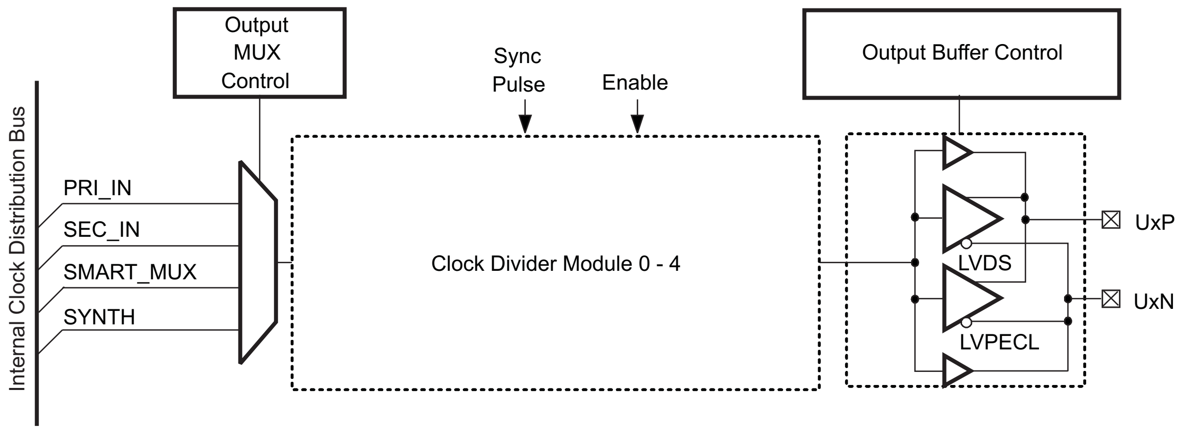


Figure 6. CDCE62005 Output Block (1 of 5)

Clock Divider Module 0–4

The following shows a simplified version of a Clock Divider Module (CDM). If an individual clock output channel is not used, then the user should disable the CDM and Output Buffer for the unused channel to save device power. Each channel includes two 7-bit registers to control the divide ratio used and the clock phase for each output. The output divider supports divide ratios from divide by 1 (bypass the divider) to divide by 80; the divider does not support all integer values between 1 and 80. Refer to for a complete list of divide ratios supported.

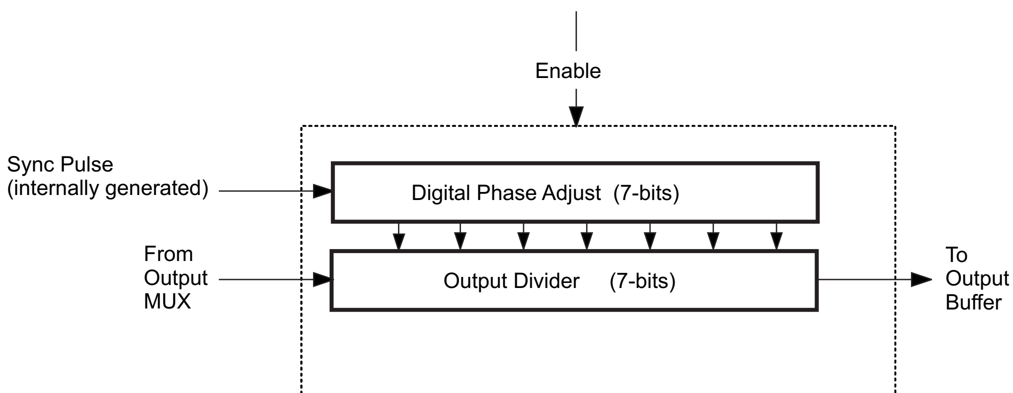


Figure 7. CDCE62005 Output Divider Module (1 of 5)

Synthesizer Block

Figure 8 presents a high-level overview of the Synthesizer Block on the CDCE62005.

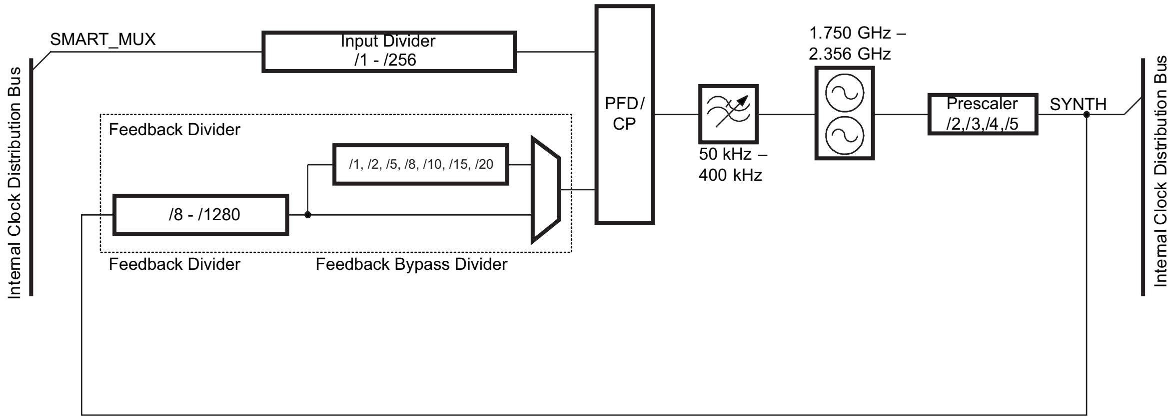


Figure 8. CDCE62005 Synthesizer Block

COMPUTING THE OUTPUT FREQUENCY

Figure 9 presents the block diagram of the CDCE62005 in synthesizer mode highlighting the clock path for a single output. It also identifies the following regions containing dividers comprising the complete clock path

- R: Includes the cumulative divider values of all dividers included from the Input Ports to the output of the Smart Multiplexer (see Input Block for more details)
- O: The output divider value (see Output Block for more details)
- I: The input divider value (see Synthesizer Block for more details)
- P: The Prescaler divider value (see Synthesizer Block of more details)
- F: The cumulative divider value of all dividers falling within the feedback divider (see Synthesizer Block for more details)

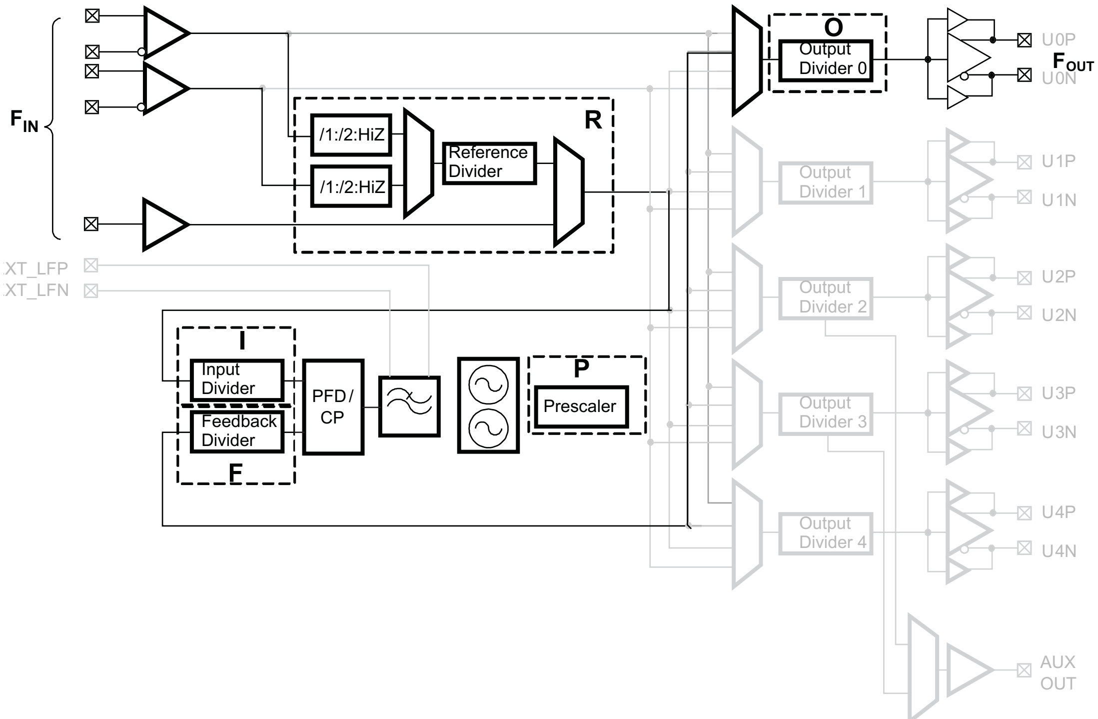


Figure 9. CDCE62005 Clock Path – Synthesizer Mode

With respect to Figure 9, any output frequency generated by the CDCE62005 relates to the input frequency connected to the Synthesizer Block by Equation 1.

$$F_{OUT} = F_{IN} \times \frac{F}{R \times I \times O} \quad (1)$$

Equation 1 holds true when subject to the following constraints:

$$1.750 \text{ Ghz} < O \times P \times F_{OUT} < 2.356 \text{ GHz} \quad (2)$$

And the comparison frequency F_{COMP},

$$40 \text{ kHz} \le F_{COMP} < 40 \text{ MHz}$$

Where:

$$F_{COMP} = \frac{F_{IN}}{R \times I}$$

Note: This device cannot output the frequencies between 780 MHz to 880 MHz (3)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{CC}	Supply voltage range(2)	-0.5 to 4.6	V
V_I	Input voltage range(3)	–0.5 to VCC + 0.5	V
V_O	Output voltage range(3)	–0.5 to VCC + 0.5	V
	Input Current ($V_I < 0$, $V_I > V_{CC}$)	±20	mA
	Output current for LVPECL/LVCMOS Outputs ($0 < V_O < V_{CC}$)	±50	mA
T_J	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated *under recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All supply voltages have to be supplied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed.

THERMAL CHARACTERISTICS

Package Thermal Resistance for QFN (RGZ) Package (1) (2)

AIRFLOW (lfm)		θ_{JP} (°C/W)(3)	θ_{JA} (°C/W)
0	JEDEC Compliant Board (6X6 VIAs on PAD)	2	28.9
100	JEDEC Compliant Board (6X6 VIAs on PAD)	2	20.4
0	Recommended Layout (7X7 VIAs on PAD)	2	27.3
100	Recommended Layout (7X7 VIAs on PAD)	2	20.3

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) Connected to GND with 36 thermal vias (0,3 mm diameter).
(3) θ_{JP} (Junction – Pad) is used for the QFN Package, because the main heat flow is from the Junction to the GND-Pad of the QFN.

ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS

recommended operating conditions for the **CDCE62005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{CC_PLL}, V_{CC_IN}, V_{CC_VCO} & V_{CCA}	Analog supply voltage		3	3.3	3.6	
P_{LVPECL}	REF at 30.72,MHz, Outputs are LVPECL	Output 1 = 491.52 MHz Output 2 = 245.76 MHz Output 3 = 122.88 MHz Output 4 = 61.44 MHz Output 5 = 30.72 MHz In case of LVCMOS Outputs = 245.76 MHz		1.9		W
P_{LVDS}	REF at 30.72 MHz, Outputs are LVDS			1.65		W
P_{LVCMOS}	REF at 30.72 MHz, Outputs are LVCMOS			1.8		W
P_{OFF}	REF at 30.72 MHz	Dividers are disabled. Outputs are disabled.		0.75		W
P_{PD}		Device is powered down		20		mW
DIFFERENTIAL INPUT MODE (PRI_IN, SEC_IN)						
V_{INPP}	Input amplitude ($V_{IN} – V_{/IN}$)(1)		0.1		1.3	V
V_{IC}	Common-mode input voltage		1.0		V_{CC}–0.3	V
I_{IH}	Differential input current high (no internal termination)	$V_I = V_{CC}$, V_{CC} = 3.6 V			20	µA
I_{IL}	Differential input current low (no internal termination)	V_I = 0 V, V_{CC} = 3.6 V	–20		20	µA
	Input Capacitance on PRI_IN, SEC_IN			3		pF
CRYSTAL INPUT SPECIFICATIONS						
	Crystal load capacitance		8		10	pF
	Equivalent series resistance (ESR)				50	Ω
LVCMOS INPUT MODE (SPI_CLK,SPI_MOSI,SPI_LE,PD,SYNC,REF_SEL, PRI_IN, SEC_IN)						
	Low-level input voltage LVCMOS,		0		0.3 x V_{CC}	V
	High-level input voltage LVCMOS		0.7 x V_{CC}		V_{CC}	V
V_{IK}	LVCMOS input clamp voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_{IH}	LVCMOS input current	$V_I = V_{CC}$, V_{CC} = 3.6 V			20	µA
I_{IL}	LVCMOS input (Except PRI_IN and SEC_IN)	V_I = 0 V, V_{CC} = 3.6 V	–10		–40	µA
I_{IL}	LVCMOS input (PRI_IN and SEC_IN)	V_I = 0 V, V_{CC} = 3.6 V	–10		10	µA
C_I	Input capacitance (LVCMOS signals)	V_I = 0 V or V_{CC}		3		pF

(1) V_{INPP} minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum V_{INPP} of 100mV.

ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE62005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
SPI OUTPUT (MISO) / PLL DIGITAL (OUTPUT MODE)							
I_{OH}	High-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V,	V_O = 1.65 V		33		mA
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OH} = −100 µA	V_{CC}–0.5			V
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = 3 V,	I_{OL} = 100 µA			0.3	V
C_O	Output capacitance on MISO	VCC = 3.3 V; VO = 0 V or VCC			3		pF
I_{OZH}	3-state output current	V_O = V_{CC}			5		µA
I_{OZL}		V_O = 0 V			–5		
PLL ANALOG (INPUT MODE)							
$I_{OZH\ LOCK}$	High-impedance state output current for PLL LOCK output(2)	V_O = 3.6 V ($\overline{PD}$ is set low)			22		µA
$I_{OZL\ LOCK}$	High-impedance state output current for PLL LOCK output	V_O = 0 V ($\overline{PD}$ is set low)			–1		µA
V_{T+}	Positive input threshold voltage V_{CC} = min to max				V_{CC}×0.55		V
V_{T-}	Negative input threshold voltage V_{CC} c= min to max				V_{CC}×0.35		V
VBB							
VBB	Termination voltage for reference inputs.	I_{BB} = –0.2 mA, Depending on the setting.		0.9		1.9	V
INPUT BUFFERS INTERNAL TERMINATION RESISTORS (PRI_IN and SEC_IN)							
	Termination resistance	Single ended			50		Ω
PHASE DETECTOR							
f_{CPmax}	Charge pump frequency			0.04		40	MHz

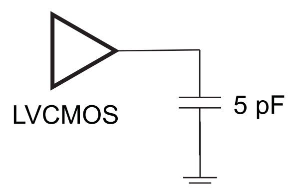
(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C
(2) Lock output has a 80kΩ pull-down resistor.

ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE62005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
LVCMOS OUTPUT OR AUXILIARY OUTPUT							
f_{clk}	Output frequency, see Figure Below	Load = 5 pF to GND		0		250	MHz
V_{OH}	High-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OH} = –100 μA	V_{CC} –0.5			
V_{OL}	Low-level output voltage for LVCMOS outputs	V_{CC} = min to max	I_{OL} =100 μA			0.3	V
I_{OH}	High-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		–30		mA
I_{OL}	Low-level output current	V_{CC} = 3.3 V	V_O = 1.65 V		33		mA
t_{pho}	Reference (PRI_IN or SEC_IN) to Output Phase offset	Outputs are set to 122.88 MHz, Reference at 30.72 MHz			0.35		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay from PRI_IN or SEC_IN to Outputs	Crosspoint to V_{CC}/2, load In Bypass Mode			4		ns
$t_{sk(o)}$	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz in bypass mode only, Reference = 200 MHz			75		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}			5		pF
I_{OZH}	3-State LVCMOS output current	V_O = V_{CC}			5		μA
I_{OZL}		V_O = 0 V			–5		μA
I_{OPDH}	Power Down output current	V_O = V_{CC}				25	μA
I_{OPDL}		V_O = 0 V				5	μA
	Duty cycle LVCMOS			45%		55%	
$t_{slew-rate}$	Output rise/fall slew rate			3.6	5.2		V/ns

(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C



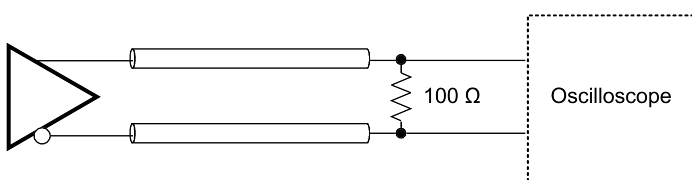
ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)[1] [2] [3] [4]

recommended operating conditions for the **CDCE62005** device for under the specified Industrial temperature range of –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP[5]	MAX	UNIT
LVDS OUTPUT						
f_{clk}	Output frequency	Configuration Load	0		800	MHz
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω	270		550	mV
ΔV_{OD}	LVDS VOD magnitude change				50	mV
V_{OS}	Offset Voltage	–40°C to 85°C		1.24		V
ΔV_{OS}	VOS magnitude change			40		mV
	Short circuit Vout+ to ground	VOUT = 0			27	mA
	Short circuit Vout– to ground	VOUT = 0			27	mA
t_{pho}	Reference (PRI_IN or SEC_IN) to output phase offset	Outputs are set to 491.52 MHz Reference at 30.72 MHz		1.65		ns
$t_{pd(LH)}/t_{pd(HL)}$	Propagation delay from PRI_IN or SEC_IN to outputs	Crosspoint to Crosspoint, load In Bypass Mode		3.1		ns
$t_{sk(o)}$ [6]	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz In Bypass Mode Only Reference = 200 MHz		25		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
I_{OPDH}	Power down output current	$V_O = V_{CC}$			25	µA
I_{OPDL}	Power down output current	V_O = 0 V			5	µA
	Duty cycle		45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of $V_{OUT(PP)}$	110	160	190	ps
	LVCMOS-TO-LVDS					
t_{skP_c}	Output skew between LVCMOS and LVDS outputs[7]	V_{CC}/2 to Crosspoint	0.9	1.4	1.9	ns

(1) This is valid only for same REF_IN clock and Y output clock frequency
(2) VINPP minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum VINPP of 100mV.
(3) Lock output has a 80 kΩ pull-down resistor.
(4) The phase of LVCMOS is lagging in reference to the phase of LVDS.
(5) All typical values are at V_{CC} = 3.3 V, temperature = 25°C
(6) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
(7) Operating the LVCMOS or LVDS output above the maximum frequency will not cause a malfunction to the device, but the output signal swing might no longer meet the output specification

LVDS DC Termination Test



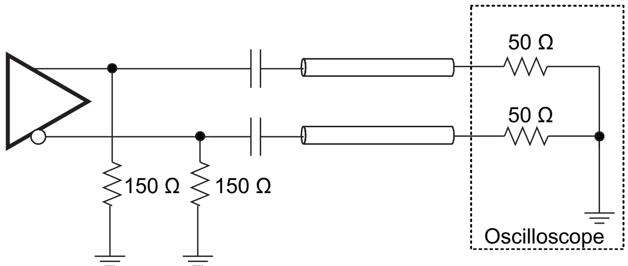
ELECTRICAL CHARACTERISTICS OPERATING CONDITIONS (Continued)

recommended operating conditions for the **CDCE62005** device for under the specified Industrial temperature range of –40°C to 85°C

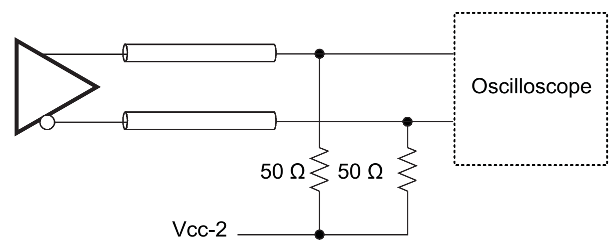
PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
LVPECL OUTPUT						
f_{clk}	Output frequency, Configuration load		0		1500	MHz
V_{OH}	LVPECL high-level output voltage load		V_{CC} –1.06		V_{CC} –0.88	V
V_{OL}	LVPECL low-level output voltage load		V_{CC}–2.02		V_{CC}–1.58	V
$\|V_{OD}\|$	Differential output voltage		610		970	mV
t_{pho}	Reference to Output Phase offset	Outputs are set to 491.52 MHz, Reference at 30.72 MHz		1.47		ns
$t_{pd(LH)}$/ $t_{pd(HL)}$	Propagation delay from PRI_IN or SEC_IN to outputs	Crosspoint to Crosspoint, load In Bypass Mode		3.4		ns
$t_{sk(o)}$	Skew, output to output For Y0 to Y4	All Outputs set at 200 MHz In Bypass Mode Only Reference = 200MHz		25		ps
C_O	Output capacitance on Y0 to Y4	V_{CC} = 3.3 V; V_O = 0 V or V_{CC}		5		pF
I_{OPDH}	Power Down output current	$V_O = V_{CC}$			25	µA
I_{OPDL}		V_O = 0 V			5	µA
	Duty Cycle		45%		55%	
t_r / t_f	Rise and fall time	20% to 80% of $V_{OUT(PP)}$	55	75	135	ps
LVDS-TO-LVPECL						
t_{skP_C}	Output skew between LVDS and LVPECL outputs	Crosspoint to Crosspoint	0.9	1.1	1.3	ns
LVCMOS-TO-LVPECL						
t_{skP_C}	Output skew between LVCMOS and LVPECL outputs	V_{CC}/2 to Crosspoint	–150	260	700	ps
LVPECL HI-PERFORMANCE OUTPUT						
V_{OH}	LVPECL high-level output voltage load		V_{CC} –1.11		V_{CC} –0.87	V
V_{OL}	LVPECL low-level output voltage load		V_{CC} –2.06		V_{CC} –1.73	V
$\|V_{OD}\|$	Differential output voltage		760		1160	mV
t_r / t_f	Rise and fall time	20% to 80% of $V_{OUT(PP)}$	55	75	135	ps

(1) All typical values are at V_{CC} = 3.3 V, temperature = 25°C

LVPECL AC Termination Test



LVPECL DC Termination Test



LVPECL OUTPUT SWING
vs
FREQUENCY

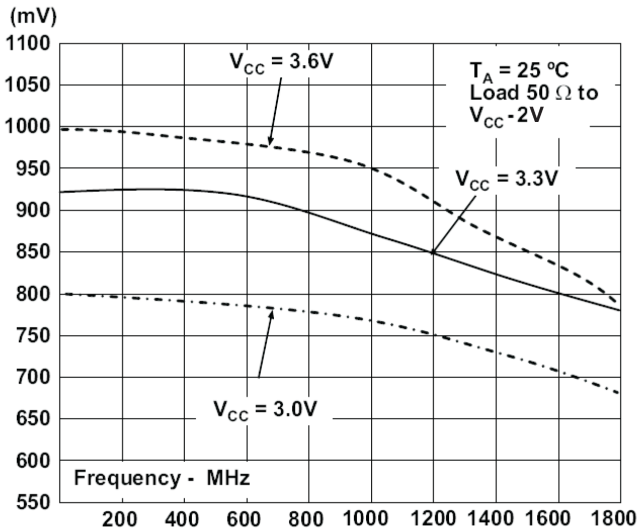


Figure 10.

HI SWING LVPECL OUTPUT SWING
vs
FREQUENCY

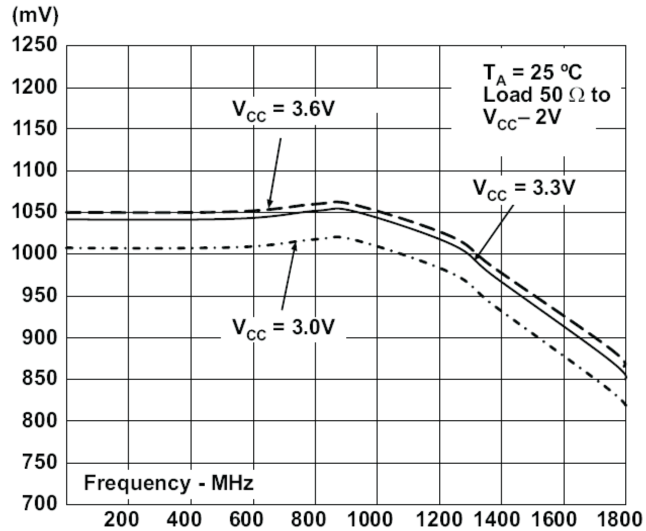


Figure 11.

LVDS OUTPUT SWING
vs
FREQUENCY

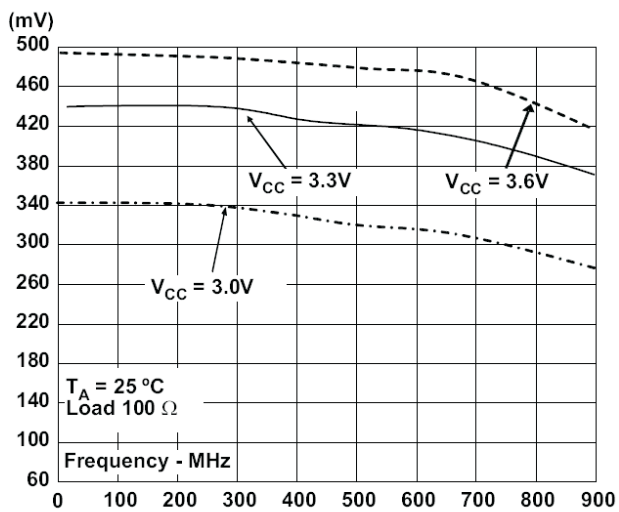


Figure 12.

LVCMOS OUTPUT SWING
vs
FREQUENCY

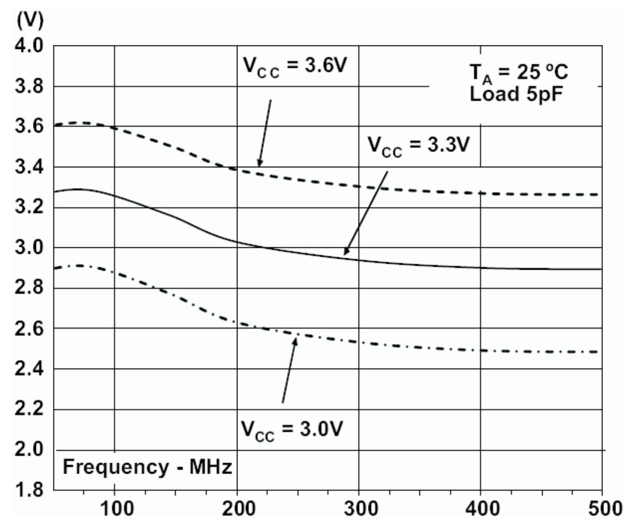


Figure 13.

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
PRI_IN/SEC_IN_IN REQUIREMENTS					
f_{max}	Maximum Clock Frequency Applied to PRI_IN & SEC_IN in fan-out mode			1500	MHz
	Maximum Clock Frequency Applied to Smart Multiplexer input Divider			500	MHz
	Maximum Clock Frequency Applied to Reference Divider			250	MHz
	For Single ended Inputs (LVCMOS) on PRI_IN and SEC_IN			250	MHz
	Single duty cycle of PRI_IN or SEC_IN at V_{CC} / 2	40%		60%	
	Differential duty cycle of PRI_IN or SEC_IN at V_{CC} / 2	40%		60%	
AUXILARY_IN REQUIREMENTS					
f_{REF}	Crystal single ended Inputs (AT-Cut Crystal Input)	2		42	MHz
$\overline{PD}$, $\overline{SYNC}$, REF_SEL REQUIREMENTS					
t_r/ t_f	Rise and fall time of the PD, SYNC, REF_SEL signal from 20% to 80% of V_{CC}			4	ns

PHASE NOISE ANALYSIS

Table 1. Device Output Phase Noise for 30.72 MHz External Reference

Phase Noise Specifications under following configuration: VCO = 1966.08 MHz, REF = 30.72 MHz, PFD Frequency = 30.72 MHz, Charge Pump Current = 1.5 mA Loop BW = 400 kHz at 3.3 V and 25°C					
Phase Noise	**Reference 30.72 MHz**	**LVPECL 491.52 MHz**	**LVDS 491.52 MHz**	**LVCMOS 122.88 MHz**	**Unit**
10 Hz	-108	–81	–81	–92	dBc/Hz
100 Hz	-130	–94	–96	–108	dBc/Hz
1 kHz	-134	–106	–106	–118	dBc/Hz
10 kHz	-152	–119	–119	–132	dBc/Hz
100 kHz	-156	–121	–122	–134	dBc/Hz
1 MHz	-157	–131	–131	–143	dBc/Hz
10 MHz	—	–145	–144	–150	dBc/Hz
20 MHz	—	–145	–144	–150	dBc/Hz
Jitter(RMS) 10k~20 MHz	193	307	315	377	fs

Table 2. Device Output Phase Noise for 25 MHz Crystal Reference

Phase Noise Specifications under following configuration: VCO = 2000.00 MHz, AUX-REF = 25.00 MHz, PFD Frequency = 25.00 MHz, Charge Pump Current = 1.5 mA Loop BW = 400 kHz at 3.3 V and 25°C					
Phase Noise	**Reference 25 MHz**	**LVPECL 500 MHz**	**LVDS 250 MHz**	**LVCMOS 125 MHz**	**Unit**
10 Hz	—	-57	-62	-68	dBc/Hz
100 Hz	—	-90	-95	-102	dBc/Hz
1 kHz	—	-107	-113	-119	dBc/Hz
10 kHz	—	-115	-122	-128	dBc/Hz
100 kHz	—	-118	-124	-130	dBc/Hz
1 MHz	—	-130	-137	-143	dBc/Hz
10 MHz	—	-145	-147	-150	dBc/Hz
20 MHz	—	-145	-147	-150	dBc/Hz
Jitter(RMS) 10k~20 MHz		389	405	437	fs

OUTPUT TO OUTPUT ISOLATION

Measurement Method

1. Connect output 2 to a spectrum analyzer. Disable Outputs 0, 1, 3, 4.
2. Measure spurious on Output 2.
3. Enable aggressor channels individually per Table 3.
4. Measure spurious on Output 2.
5. The difference between the spurious levels of Output 2 before and after enabling the aggressor channels determine the output-to-output isolation performance recorded.

Table 3. Output to Output Isolation

			M SPUR	Unit
The Output to Output Isolation was tested under following settings are 25°C				
Output 2	Measured Channel	**In LVPECL Signaling 15.5 MHz**	**–67**	**db**
Output 2	Measured Channel	**In LVPECL Signaling 93 MHz**	**–60**	**db**
Output 2	Measured Channel	**In LVPECL Signaling 930 MHz**	**–59**	**db**
Output 0	*Aggressor Channel*	*LVPECL 22.14 MHz*		
Output 1	*Aggressor Channel*	*LVPECL 22.14 MHz*		
Output 3	*Aggressor Channel*	*LVPECL 22.14 MHz*		
Output 4	*Aggressor Channel*	*LVPECL 22.14 MHz*		

SPI CONTROL INTERFACE TIMING

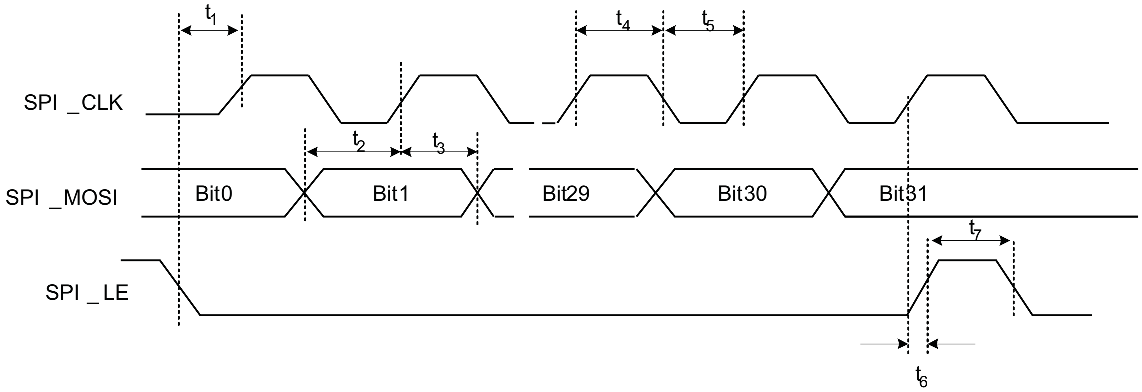


Figure 14. Timing Diagram for SPI Write Command

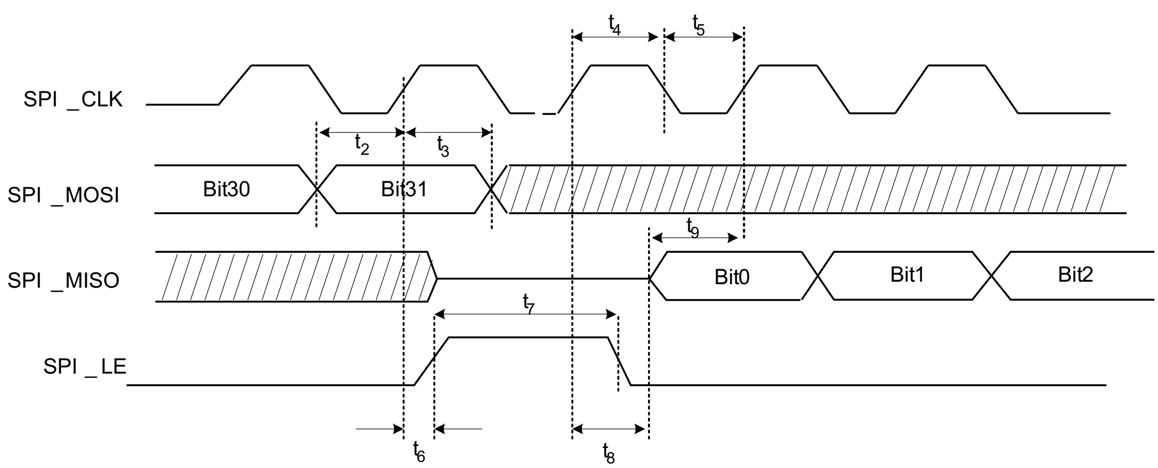


Figure 15. Timing Diagram for SPI Read Command

Table 4. SPI Bus Timing Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
f_{Clock}	Clock Frequency for the SPI_CLK			20	MHz
t_1	SPI_LE to SPI_CLK setup time	10			ns
t_2	SPI_MOSI to SPI_CLK setup time	10			ns
t_3	SPI_MOSI to SPI_CLK hold time	10			ns
t_4	SPI_CLK high duration	25			ns
t_5	SPI_CLK low duration	25			ns
t_6	SPI_CLK to SPI_LE Setup time	10			ns
t_7	SPI_LE Pulse Width	20			ns
t_8	SPI_MISO to SPI_CLK Data Valid (First Valid Bit after LE)	10			ns

DEVICE CONFIGURATION

The Functional Description Section described four different functional blocks contained within the CDCE62005. Figure 16 depicts these blocks along with a high-level functional block diagram of the circuit elements comprising each block. The balance of this section focuses on a detailed discussion of each functional block from the perspective of how to configure them.

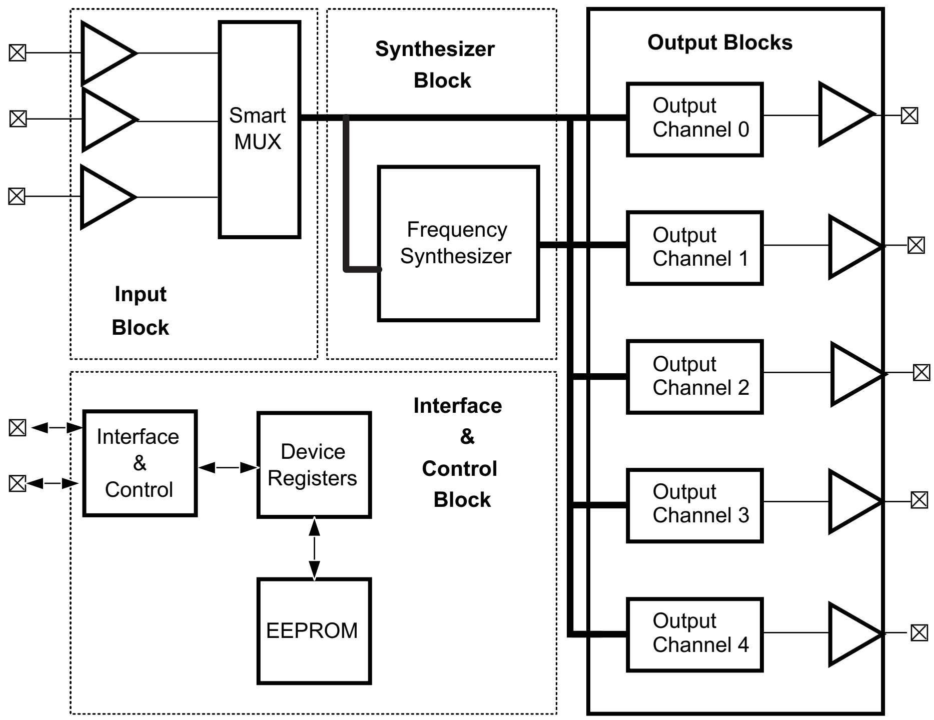


Figure 16. CDCE62005 Circuit Blocks

Throughout this section, references to Device Register memory locations follow the following convention:

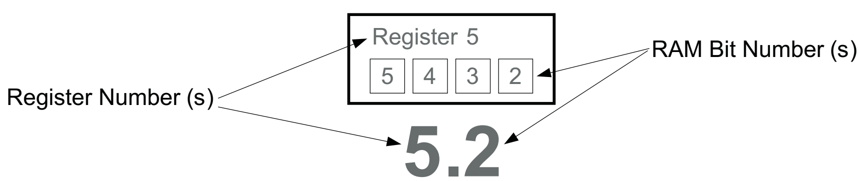


Figure 17. Device Register Reference Convention

INTERFACE AND CONTROL BLOCK

The Interface & Control Block includes a SPI interface, four control pins, a non-volatile memory array in which the device stores default configuration data, and an array of device registers implemented in Static RAM. This RAM, also called the device registers, configures all hardware within the CDCE62005.

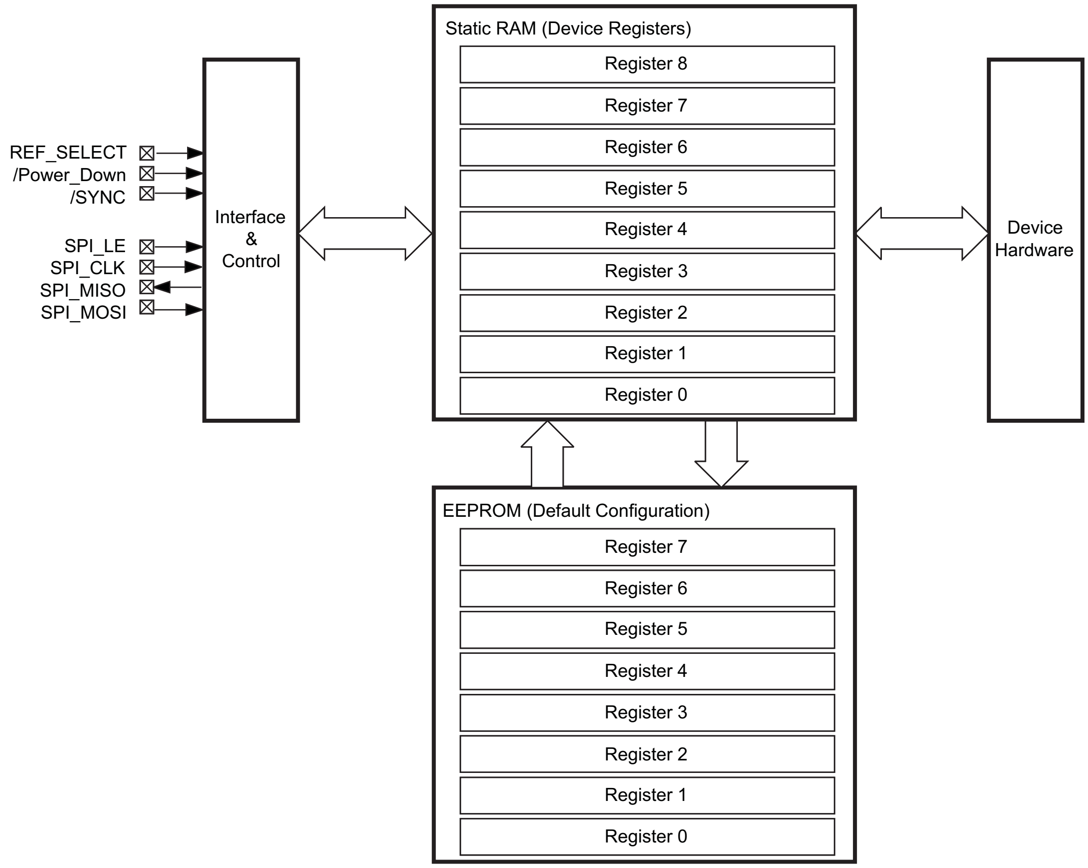


Figure 18. CDCE62005 Interface and Control Block

SPI (Serial Peripheral Interface)

The serial interface of CDCE62005 is a simple bidirectional SPI interface for writing and reading to and from the device registers. It implements a low speed serial communications link in a master/slave topology in which the CDCE62005 is a slave. The SPI consists of four signals:

- **SPI_CLK:** Serial Clock (Output from Master) – the CDCE62005 clocks data in and out on the rising edge of SPI_CLK. Data transitions therefore occur on the falling edge of the clock.
- **SPI_MOSI:** Master Output Slave Input (Output from Master) .
- **SPI_MISO:** Master Input Slave Output (Output from Slave)
- **SPI_LE:** Latch Enable (Output from Master). The falling edge of SPI_LE initiates a transfer. If SPI_LE is high, no data transfer can take place.

The CDCE62005 implements data fields that are 28-bits wide. In addition, it contains 9 registers, each comprising a 28 bit data field. Therefore, accessing the CDCE62005 requires that the host program append a 4-bit address field to the front of the data field as follows:

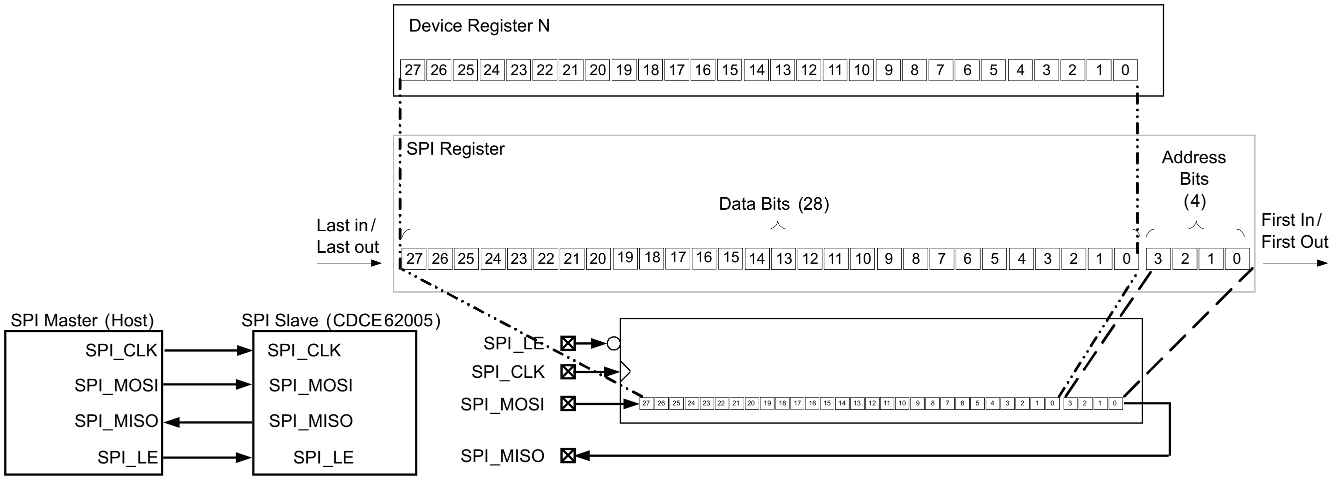


Figure 19. CDCE62005 SPI Communications Format

CDCE62005 SPI Command Structure

The CDCE62005 supports four commands issued by the Master via the SPI:

- Write to RAM
- Read Command
- Copy RAM to EEPROM – unlock
- Copy RAM to EEPROM – lock

Table 5 provides a summary of the CDCE62005 SPI command structure. The host (master) constructs a Write to RAM command by specifying the appropriate register address in the address field and appends this value to the beginning of the data field. Therefore, a valid command stream must include 32 bits, transmitted LSB first. The host must issue a Read Command to initiate a data transfer from the CDCE62005 back to the host. This command specifies the address of the register of interest in the data field.

Table 5. CDCE62005 SPI Command Structure

			Data Field (28 Bits)																												Addr Field (4 Bits)			
Register	**Operation**	**NVM**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
0	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
1	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1
2	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0
3	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1
4	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	0
5	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	1
6	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0
7	Write to RAM	Yes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	1
8	Status/Control	No	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0
Instruction	Read Command	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A	A	A	A	1	1	1	0
Instruction	RAM EEPROM	Unlock	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Instruction	RAM EEPROM	Lock (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1

(1) **CAUTION:** After execution of this command, the EEPROM is permanently locked. After locking the EEPROM, device configuration can only be changed via Write to RAM after power-up; however, the EEPROM can no longer be changed

The CDCE62005 on-board EEPROM has been factory preset to the default settings listed in the table below.

REGISTER	DEFAULT SETTING
REG0000	8184032
REG0001	8184030
REG0002	8186030
REG0003	EB86030
REG0004	0186031
REG0005	101C0BE
REG0006	04BE19A
REG0007	BD0037F
REG0008 (RAM)	80005DD

The Default configurations programmed in the device is set to: Primary and Secondary are set to LVPECL AC termination and the Auxiliary input is enabled. The Smart Mux is set to auto select among Primary, Secondary and Auxiliary. Reference is set at 25MHz and the dividers are selected to run the VCO at 1875MHz.

Output 0 & 1 are set to output 156.25MHz with LVPECL signaling

Output 2 is set to output 125MHz/ LVPECL

Output 3 is set to output 125MHz/ LVDS

Output 4 is set to output 125MHz/ LVCMOS

Writing to the CDCE62005

Figure 20 illustrates a Write to RAM operation. Notice that the latching of the first data bit in the data stream (Bit 0) occurs on the first rising edge of SPI_CLK after SPI_LE transitions from a high to a low. For the CDCE62005, data transitions occur on the falling edge of SPI_CLK. A rising edge on SPI_LE signals to the CDCE62005 that the transmission of the last bit in the stream (Bit 31) has occurred.

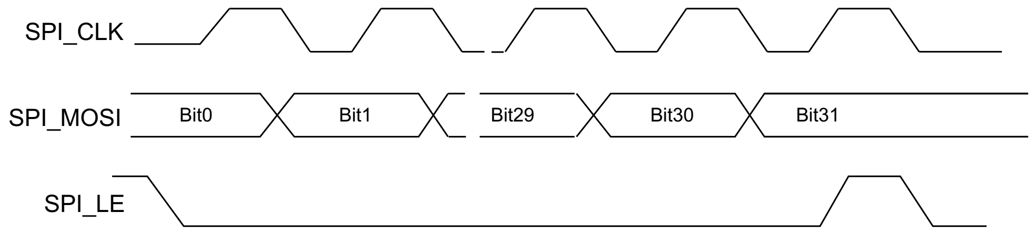


Figure 20. CDCE62005 SPI Write Operation

Reading from the CDCE62005

Figure 21 shows how the CDCE62005 executes a Read Command. The SPI master first issues a Read Command to initiate a data transfer from the CDCE62005 back to the host (see Table 6). This command specifies the address of the register of interest. By transitioning SPI_LE from a low to a high, the CDCE62005 resolves the address specified in the appropriate bits of the data field. The host drives SPI_LE low and the CDCE62005 presents the data present in the register specified in the Read Command on SPI_MISO.

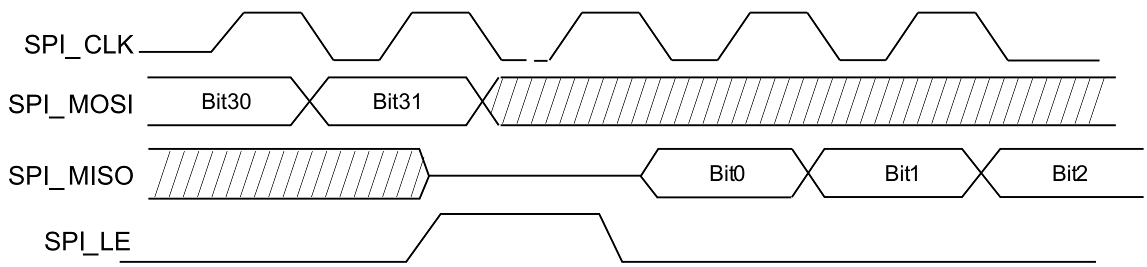


Figure 21. CDCE62005 Read Operation

Writing to EEPROM

After the CDCE62005 detects a power-up and completes a reset cycle, it copies the contents of the on-board EEPROM into the Device Registers. Therefore, the CDCE62005 initializes into a known state pre-defined by the user. The host issues one of two special commands shown in Table 6 to copy the contents of Device Registers 0 through 7 (a total of 184 bits) into EERPOM. They include:

- Copy RAM to EEPROM – Unlock, Execution of this command can happen many times.
- Copy RAM to EEPROM – Lock: Execution of this command can happen only once; after which the EEPROM is **permanently locked**.

After either command is initiated, power must remain stable and the host must not access the CDCE62005 for at least 50 ms to allow the EEPROM to complete the write cycle and to avoid the possibility of EEPROM corruption.

Device Registers: Register 0

Table 6. CDCE62005 Register 0 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	0
1		A1		Address 1	0
2		A2		Address 2	0
3		A3		Address 3	0
4	0	DIV2PRIX	Primary Reference	Pre-Divider Selection for the Primary Reference (X,Y)=00:3-state, 01:Divide by "1", 10:Divide by "2", 11:Reserved	EEPROM
5	1	DIV2PRIY			EEPROM
6	2	RESERVED		*Used in Test Mode*	EEPROM
7	3	RESERVED		*Used in Test Mode*	EEPROM
8	4	OUTMUX0SELX	Output 0	OUTPUT MUX "0" Select. Selects the Signal driving Output Divider"0" (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:VCO_CORE	EEPROM
9	5	OUTMUX0SELY	Output 0		EEPROM
10	6	PH0ADJC0	Output 0	Coarse phase adjust select for output divider "0"	EEPROM
11	7	PH0ADJC1	Output 0		EEPROM
12	8	PH0ADJC2	Output 0		EEPROM
13	9	PH0ADJC3	Output 0		EEPROM
14	10	PH0ADJC4	Output 0		EEPROM
15	11	PH0ADJC5	Output 0		EEPROM
16	12	PH0ADJC6	Output 0		EEPROM
17	13	OUT0DIVRSEL0	Output 0	OUTPUT DIVIDER "0" Ratio Select	EEPROM
18	14	OUT0DIVRSEL1	Output 0		EEPROM
19	15	OUT0DIVRSEL2	Output 0		EEPROM
20	16	OUT0DIVRSEL3	Output 0		EEPROM
21	17	OUT0DIVRSEL4	Output 0		EEPROM
22	18	OUT0DIVRSEL5	Output 0		EEPROM
23	19	OUT0DIVRSEL6	Output 0		EEPROM
24	20	OUT0DIVSEL	Output 0	When set to "0", the divider is disabled When set to "1", the divider is enabled	EEPROM
25	21	HiSWINGLVPECL0	Output 0	High Swing LVPECL When set to "1" and Normal Swing when set to "0" – If LVCMOS or LVDS is selected the Output swing will stay at the same level. – If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to "1" and Normal LVPECL if it is set to "0".	EEPROM
26	22	CMOSMODE0PX	Output 0	LVCMOS mode select for OUTPUT "0" Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
27	23	CMOSMODE0PY	Output 0		EEPROM
28	24	CMOSMODE0NX	Output 0	LVCMOS mode select for OUTPUT "0" Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
29	25	CMOSMODE0NY	Output 0		EEPROM
30	26	OUTBUFSEL0X	Output 0		EEPROM
31	27	OUTBUFSEL0Y	Output 0		EEPROM

OUTPUT TYPE	RAM BITS					
	22	**23**	**24**	**25**	**26**	**27**
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	*See Settings Above**				0	0
Output Disabled	0	1	0	1	1	0

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

Device Registers: Register 1

Table 7. CDCE62005 Register 1 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	1
1		A1		Address 1	0
2		A2		Address 2	0
3		A3		Address 3	0
4	0	DIV2SECX	Secondary Reference	Pre-Divider Selection for the Secondary Reference (X,Y)=00:3-state, 01:Divide by "1", 10:Divide by "2", 11:Reserved	EEPROM
5	1	DIV2SECY			EEPROM
6	2	RESERVED		*Used in Test Mode*	EEPROM
7	3	RESERVED		*Used in Test Mode*	EEPROM
8	4	OUTMUX1SELX	Output 1	OUTPUT MUX "1" Select. Selects the Signal driving Output Divider"1" (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:VCO_CORE	EEPROM
9	5	OUTMUX1SELY	Output 1		EEPROM
10	6	PH1ADJC0	Output 1	Coarse phase adjust select for output divider "1"	EEPROM
11	7	PH1ADJC1	Output 1		EEPROM
12	8	PH1ADJC2	Output 1		EEPROM
13	9	PH1ADJC3	Output 1		EEPROM
14	10	PH1ADJC4	Output 1		EEPROM
15	11	PH1ADJC5	Output 1		EEPROM
16	12	PH1ADJC6	Output 1		EEPROM
17	13	OUT1DIVRSEL0	Output 1	OUTPUT DIVIDER "1" Ratio Select	EEPROM
18	14	OUT1DIVRSEL1	Output 1		EEPROM
19	15	OUT1DIVRSEL2	Output 1		EEPROM
20	16	OUT1DIVRSEL3	Output 1		EEPROM
21	17	OUT1DIVRSEL4	Output 1		EEPROM
22	18	OUT1DIVRSEL5	Output 1		EEPROM
23	19	OUT1DIVRSEL6	Output 1		EEPROM
24	20	OUT1DIVSEL	Output 1	When set to "0", the divider is disabled When set to "1", the divider is enabled	EEPROM
25	21	HiSWINGLVPECL1	Output 1	High Swing LVPECL When set to "1" and Normal Swing when set to "0" – If LVCMOS or LVDS is selected the Output swing will stay at the same level. – If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to "1" and Normal LVPECL if it is set to "0".	EEPROM
26	22	CMOSMODE1PX	Output 1	LVCMOS mode select for OUTPUT "1" Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
27	23	CMOSMODE1PY	Output 1		EEPROM
28	24	CMOSMODE1NX	Output 1	LVCMOS mode select for OUTPUT "1" Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
29	25	CMOSMODE1NY	Output 1		EEPROM
30	26	OUTBUFSEL1X	Output 1	(see table below)	EEPROM
31	27	OUTBUFSEL1Y	Output 1		EEPROM

OUTPUT TYPE	RAM BITS					
	22	**23**	**24**	**25**	**26**	**27**
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	*See Settings Above**				0	0
Output Disabled	0	1	0	1	1	0

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

Device Registers: Register 2

Table 8. CDCE62005 Register 2 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	0
1		A1		Address 1	1
2		A2		Address 2	0
3		A3		Address 3	0
4	0	REFDIV0	Reference Divider	Reference Divider Bit “0”	EEPROM
5	1	REFDIV1		Reference Divider Bit “1”	EEPROM
6	2	RESERVED		*Used in Test Mode*	EEPROM
7	3	RESERVED		*Used in Test Mode*	EEPROM
8	4	OUTMUX2SELX	Output 2	OUTPUT MUX “2” Select. Selects the Signal driving Output Divider”2” (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:VCO_CORE	EEPROM
9	5	OUTMUX2SELY	Output 2		EEPROM
10	6	PH2ADJC0	Output 2	Coarse phase adjust select for output divider “2”	EEPROM
11	7	PH2ADJC1	Output 2		EEPROM
12	8	PH2ADJC2	Output 2		EEPROM
13	9	PH2ADJC3	Output 2		EEPROM
14	10	PH2ADJC4	Output 2		EEPROM
15	11	PH2ADJC5	Output 2		EEPROM
16	12	PH2ADJC6	Output 2		EEPROM
17	13	OUT2DIVRSEL0	Output 2	OUTPUT DIVIDER “2” Ratio Select	EEPROM
18	14	OUT2DIVRSEL1	Output 2		EEPROM
19	15	OUT2DIVRSEL2	Output 2		EEPROM
20	16	OUT2DIVRSEL3	Output 2		EEPROM
21	17	OUT2DIVRSEL4	Output 2		EEPROM
22	18	OUT2DIVRSEL5	Output 2		EEPROM
23	19	OUT2DIVRSEL6	Output 2		EEPROM
24	20	OUT2DIVSEL	Output 2	When set to “0”, the divider is disabled When set to “1”, the divider is enabled	EEPROM
25	21	HiSWINGLVPEC2	Output 2	High Swing LVPECL When set to “1” and Normal Swing when set to “0” – If LVCMOS or LVDS is selected the Output swing will stay at the same level. – If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to “1” and Normal LVPECL if it is set to “0”.	EEPROM
26	22	CMOSMODE2PX	Output 2	LVCMOS mode select for OUTPUT “2” Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
27	23	CMOSMODE2PY	Output 2		EEPROM
28	24	CMOSMODE2NX	Output 2	LVCMOS mode select for OUTPUT “2” Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
29	25	CMOSMODE2NY	Output 2		EEPROM
30	26	OUTBUFSEL2X	Output 2	(see table below)	EEPROM
31	27	OUTBUFSEL2Y	Output 2		EEPROM

OUTPUT TYPE	RAM BITS					
	22	23	24	25	26	27
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	*See Settings Above**				0	0
Output Disabled	0	1	0	1	1	0

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

Device Registers: Register 3

Table 9. CDCE62005 Register 3 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	1
1		A1		Address 1	1
2		A2		Address 2	0
3		A3		Address 3	0
4	0	REFDIV2	Reference Divider	Reference Divider Bit "2"	EEPROM
5	1	RESERVED			EEPROM
6	2	RESERVED		*Used in Test Mode*	EEPROM
7	3	RESERVED		*Used in Test Mode*	EEPROM
8	4	OUTMUX3SELX	Output 3	OUTPUT MUX "3" Select. Selects the Signal driving Output Divider"3" (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:VCO_CORE	EEPROM
9	5	OUTMUX3SELY	Output 3		EEPROM
10	6	PH3ADJC0	Output 3	Coarse phase adjust select for output divider "3"	EEPROM
11	7	PH3ADJC1	Output 3		EEPROM
12	8	PH3ADJC2	Output 3		EEPROM
13	9	PH3ADJC3	Output 3		EEPROM
14	10	PH3ADJC4	Output 3		EEPROM
15	11	PH3ADJC5	Output 3		EEPROM
16	12	PH3ADJC6	Output 3		EEPROM
17	13	OUT3DIVRSEL0	Output 3	OUTPUT DIVIDER "3" Ratio Select	EEPROM
18	14	OUT3DIVRSEL1	Output 3		EEPROM
19	15	OUT3DIVRSEL2	Output 3		EEPROM
20	16	OUT3DIVRSEL3	Output 3		EEPROM
21	17	OUT3DIVRSEL4	Output 3		EEPROM
22	18	OUT3DIVRSEL5	Output 3		EEPROM
23	19	OUT3DIVRSEL6	Output 3		EEPROM
24	20	OUT3DIVSEL	Output 3	When set to "0", the divider is disabled When set to "1", the divider is enabled	EEPROM
25	21	HiSWINGLVPEC3	Output 3	High Swing LVPECL When set to "1" and Normal Swing when set to "0" – If LVCMOS or LVDS is selected the Output swing will stay at the same level. – If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to "1" and Normal LVPECL if it is set to "0".	EEPROM
26	22	CMOSMODE3PX	Output 3	LVCMOS mode select for OUTPUT "3" Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
27	23	CMOSMODE3PY	Output 3		EEPROM
28	24	CMOSMODE3NX	Output 3	LVCMOS mode select for OUTPUT "3" Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
29	25	CMOSMODE3NY	Output 3		EEPROM
30	26	OUTBUFSEL3X	Output 3		EEPROM
31	27	OUTBUFSEL3Y	Output 3		EEPROM

OUTPUT TYPE	RAM BITS					
	22	23	24	25	26	27
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	*See Settings Above**				0	0
Output Disabled	0	1	0	1	1	0

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

Device Registers: Register 4

Table 10. CDCE62005 Register 4 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	0
1		A1		Address 1	0
2		A2		Address 2	1
3		A3		Address 3	0
4	0	RESERVED	—	This bit must be set to a "1"	EEPROM
5	1	ATETEST	TI Test Bit	0 (default): normal operation, 1: outputs have deterministic delay relative to low-to-high pulse of $\overline{\text{SYNC}}$ pin when the $\overline{\text{SYNC}}$ signal is synchronized with the reference input	EEPROM
6	2	RESERVED		*Used in Test Mode*	EEPROM
7	3	RESERVED		*Used in Test Mode*	EEPROM
8	4	OUTMUX4SELX	Output 4	OUTPUT MUX "4" Select. Selects the Signal driving Output Divider"4" (X,Y) = 00: PRI_IN, 01:SEC_IN, 10:SMART_MUX, 11:VCO_CORE	EEPROM
9	5	OUTMUX4SELY	Output 4		EEPROM
10	6	PH4ADJC0	Output 4	Coarse phase adjust select for output divider "4"	EEPROM
11	7	PH4ADJC1	Output 4		EEPROM
12	8	PH4ADJC2	Output 4		EEPROM
13	9	PH4ADJC3	Output 4		EEPROM
14	10	PH4ADJC4	Output 4		EEPROM
15	11	PH4ADJC5	Output 4		EEPROM
16	12	PH4ADJC6	Output 4		EEPROM
17	13	OUT4DIVRSEL0	Output 4	OUTPUT DIVIDER "4" Ratio Select	EEPROM
18	14	OUT4DIVRSEL1	Output 4		EEPROM
19	15	OUT4DIVRSEL2	Output 4		EEPROM
20	16	OUT4DIVRSEL3	Output 4		EEPROM
21	17	OUT4DIVRSEL4	Output 4		EEPROM
22	18	OUT4DIVRSEL5	Output 4		EEPROM
23	19	OUT4DIVRSEL6	Output 4		EEPROM
24	20	OUT4DIVSEL	Output 4	When set to "0", the divider is disabled When set to "1", the divider is enabled	EEPROM
25	21	HiSWINGLVPEC4	Output 4	High Swing LVPECL When set to "1" and Normal Swing when set to "0" – If LVCMOS or LVDS is selected the Output swing will stay at the same level. – If LVPECL buffer is selected the Output Swing will be 30% higher if this bit is set to "1" and Normal LVPECL if it is set to "0".	EEPROM
26	22	CMOSMODE4PX	Output 4	LVCMOS mode select for OUTPUT "4" Positive Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
27	23	CMOSMODE4PY	Output 4		EEPROM
28	24	CMOSMODE4NX	Output 4	LVCMOS mode select for OUTPUT "3" Negative Pin. (X,Y)=00:Active, 10:Inverting, 11:Low, 01:3-State	EEPROM
29	25	CMOSMODE4NY	Output 4		EEPROM
30	26	OUTBUFSEL4X	Output 4	(see output type table below)	EEPROM
31	27	OUTBUFSEL4Y	Output 4		EEPROM

OUTPUT TYPE	RAM BITS					
	22	23	24	25	26	27
LVPECL	0	0	0	0	0	1
LVDS	0	1	0	1	1	1
LVCMOS	*See Settings Above**				0	0
Output Disabled	0	1	0	1	1	0

** Use Description for Bits 22,23,24 and 25 for setting the LVCMOS Outputs*

Device Registers: Register 5

Table 11. CDCE62005 Register 5 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	1
1		A1		Address 1	0
2		A2		Address 2	1
3		A3		Address 3	0
4	0	INBUFSELX	INBUFSELX	Input Buffer Select (LVPECL,LVDS or LVCMOS) XY(01) LVPECL, (11) LVDS, (00) LVCMOS- Input is Positive Pin	EEPROM
5	1	INBUFSELY	INBUFSELY		EEPROM
6	2	PRISEL	Smart MUX	WHEN EECLKSEL = 1; Bit (6,7,8) 100 – PRISEL, 010 – SECSEL , 001 – AUXSEL 110 – Auto Select (PRI then SEC) 111 – Auto Select (PRI then SEC and then AUX) When EECLKSEL = 0, REF_SEL pin determines the Reference Input to the Smart Mux circuitry.	EEPROM
7	3	SECSEL			EEPROM
8	4	AUXSEL			EEPROM
9	5	EECLKSEL	Smart MUX	If EEPROM Clock Select Input is set to “1” The Clock selections follows internal EEPROM settings and ignores REF_SEL Pin status, when Set to “0” REF_SEL is used to control the Mux, Auto Select Function is not available and AUXSEL is not available.	EEPROM
10	6	ACDCSEL	Input Buffers	If Set to “1” DC Termination, If set to “0” AC Termination	EEPROM
11	7	HYSTEN	Input Buffers	If Set to “1” Input Buffers Hysteresis Enabled. It is not recommended that Hysteresis be disabled.	EEPROM
12	8	PRI_TERMSEL	Input Buffers	If Set to “0” Primary Input Buffer Internal Termination Enabled If set to “1” Primary Internal Termination circuitry Disabled	EEPROM
13	9	PRIINVBB	Input Buffers	If Set to “1” Primary Input Negative Pin Biased with Internal VBB Voltage.	EEPROM
14	10	SECINVBB	Input Buffers	If Set to “1” Secondary Input Negative Pin Biased with Internal VBB Voltage	EEPROM
15	11	FAILSAFE	Input Buffers	If Set to “1” Fail Safe is Enabled for all Input Buffers configured as LVDS, DC Coupling only.	EEPROM
16	12	RESERVED		Must be set to “0”	EEPROM
17	13	RESERVED	--------	Must be set to “0”	EEPROM
18	14	SELINDIV0	VCO Core	INPUT DIVIDER Settings	EEPROM
19	15	SELINDIV1	VCO Core		EEPROM
20	16	SELINDIV2	VCO Core		EEPROM
21	17	SELINDIV3	VCO Core		EEPROM
22	18	SELINDIV4	VCO Core		EEPROM
23	19	SELINDIV5	VCO Core		EEPROM
24	20	SELINDIV6	VCO Core		EEPROM
25	21	SELINDIV7	VCO Core		EEPROM
26	22	LOCKW(0)	PLL Lock	LOCKW(3:0): Lock-detect Window Width = 0000 (narrow window), = 0001,0010,0100,0101 ….. = 1110 (widest window) = XX11 (RESERVED)	EEPROM
27	23	LOCKW(1)			EEPROM
28	24	LOCKW(2)			EEPROM
29	25	LOCKW(3)			EEPROM
30	26	LOCKDET	PLL Lock	Number of coherent lock events. If set to “0” it triggers after the first lock detection if set to “1” it triggers lock after 64 cycles of lock detections.	EEPROM
31	27	ADLOCK	PLL Lock	Selects Digital PLL_LOCK “0” ,Selects Analog PLL_LOCK “1”	EEPROM

Device Registers: Register 6

Table 12. CDCE62005 Register 6 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	0
1		A1		Address 1	1
2		A2		Address 2	1
3		A3		Address 3	0
4	0	SELVCO	VCO Core	VCO Select, 0:VCO1(low range), 1:VCO2(high range)	EEPROM
5	1	SELPRESCA	VCO Core	PRESCALER Setting.	EEPROM
6	2	SELPRESCB	VCO Core		EEPROM
7	3	SELFBDIV0	VCO Core	FEEDBACK DIVIDER Setting	EEPROM
8	4	SELFBDIV1	VCO Core		EEPROM
9	5	SELFBDIV2	VCO Core		EEPROM
10	6	SELFBDIV3	VCO Core		EEPROM
11	7	SELFBDIV4	VCO Core		EEPROM
12	8	SELFBDIV5	VCO Core		EEPROM
13	9	SELFBDIV6	VCO Core		EEPROM
14	10	SELFBDIV7	VCO Core		EEPROM
15	11	RESERVED	—	Must be set to "0"	EEPROM
16	12	SEC_TERMSEL	Input Buffers	If Set to "0" Secondary Input Buffer Internal Termination Enabled If set to "1" Secondary Internal Termination circuitry Disabled	EEPROM
17	13	SELBPDIV0	VCO Core	BYPASS DIVIDER Setting (6 settings + Disable + Enable)	EEPROM
18	14	SELBPDIV1	VCO Core		EEPROM
19	15	SELBPDIV2	VCO Core		EEPROM
20	16	ICPSEL0	VCO Core	CHARGE PUMP Current Select	EEPROM
21	17	ICPSEL1	VCO Core		EEPROM
22	18	ICPSEL2	VCO Core		EEPROM
23	19	ICPSEL3	VCO Core		EEPROM
24	20	RESERVED	VCO Core	When set to "0", outputs are synchronized to the reference input on the low-to-high pulse on SYNC pin or bit. When set to "1", outputs are synchronized to the SYNC low-to-high pulse	EEPROM
25	21	CPPULSEWIDTH	VCO Core	If set to 1=wide pulse, 0=narrow pulse	EEPROM
26	22	ENCAL	VCO Core	Enable VCO Calibration Command. To execute this command a rising edge must be generated (i.e. Write a LOW followed by a high to this bit location). This will initiate a VCO calibration sequence only if Calibration Mode = Manual Mode (i.e. Register 6 bit 27 is HIGH).	EEPROM
27	23	RESERVED	—	Must be set to "0"	EEPROM
28	24	AUXOUTEN	Output AUX	Enable Auxiliary Output when set to "1".	EEPROM
29	25	AUXFEEDSEL	Output AUX	Select the Output that will driving the AUX Output; Low for Selecting Output Divider "2" and High for Selecting Output Divider "3"	EEPROM
30	26	EXLFSEL	VCO Core	When Set to "1" External Loop filter is used. When Set to "0" Internal Loop Filter is used.	EEPROM
31	27	ENCAL_MODE	PLL Calibration	1: Calibration Mode = Manual Mode. In this mode, a calibration will be initiated if a rising edge is asserted on ENCAL (Register 6 Bit 22). 0: Calibration Mode = Startup Mode.	EEPROM

Device Registers: Register 7

Table 13. CDCE62005 Register 7 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	1
1		A1		Address 1	1
2		A2		Address 2	1
3		A3		Address 3	0
4	0	LFRCSEL0	VCO Core	Loop Filter Control Setting	EEPROM
5	1	LFRCSEL1	VCO Core	Loop Filter Control Setting	EEPROM
6	2	LFRCSEL2	VCO Core	Loop Filter Control Setting	EEPROM
7	3	LFRCSEL3	VCO Core	Loop Filter Control Setting	EEPROM
8	4	LFRCSEL4	VCO Core	Loop Filter Control Setting	EEPROM
9	5	LFRCSEL5	VCO Core	Loop Filter Control Setting	EEPROM
10	6	LFRCSEL6	VCO Core	Loop Filter Control Setting	EEPROM
11	7	LFRCSEL7	VCO Core	Loop Filter Control Setting	EEPROM
12	8	LFRCSEL8	VCO Core	Loop Filter Control Setting	EEPROM
13	9	LFRCSEL9	VCO Core	Loop Filter Control Setting	EEPROM
14	10	LFRCSEL10	VCO Core	Loop Filter Control Setting	EEPROM
15	11	LFRCSEL11	VCO Core	Loop Filter Control Setting	EEPROM
16	12	LFRCSEL12	VCO Core	Loop Filter Control Setting	EEPROM
17	13	LFRCSEL13	VCO Core	Loop Filter Control Setting	EEPROM
18	14	LFRCSEL14	VCO Core	Loop Filter Control Setting	EEPROM
19	15	LFRCSEL15	VCO Core	Loop Filter Control Setting	EEPROM
20	16	LFRCSEL16	VCO Core	Loop Filter Control Setting	EEPROM
21	17	LFRCSEL17	VCO Core	Loop Filter Control Setting	EEPROM
22	18	LFRCSEL18	VCO Core	Loop Filter Control Setting	EEPROM
23	19	LFRCSEL19	VCO Core	Loop Filter Control Setting	EEPROM
24	20	LFRCSEL20	VCO Core	Loop Filter Control Setting	EEPROM
25	21	RESERVED	—	Must be set to "0"	EEPROM
26	22	TESTMUX1	Diagnostics	Set to “1”	EEPROM
27	23	SEL_DEL2	Smart Mux	If set to “0” it enables short delay for fast operation If Set to “1” Long Delay recommended for Input References below 150MHz.	EEPROM
28	24	TEXTMUX2	Diagnostics	Set to “1”	EEPROM
29	25	SEL_DEL1	Smart Mux	If set to “0” it enables short delay for fast operation If Set to “1” Long Delay recommended for Input References below 150MHz.	EEPROM
30	26	EPLOCK	Status	Read Only If EPLOCK reads “0” EEPROM is unlocked. If EPLOCK reads “1”, then the EEPROM is locked (see Table 5 for how to lock the EEPROM – this can only be executed once after which the EEPROM is locked **permanently**).	EEPROM
31	27	RESERVED	Status	Read Only Always reads “1”	EEPROM

Device Registers: Register 8

Table 14. CDCE62005 Register 8 Bit Definitions

SPI BIT	RAM BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION	
0		A0		Address 0	0
1		A1		Address 1	0
2		A2		Address 2	0
3		A3		Address 3	1
4	0	CALWORD0	Status	"VCO Calibration Word" read back from device	RAM
5	1	CALWORD1	Status		RAM
6	2	CALWORD2	Status		RAM
7	3	CALWORD3	Status		RAM
8	4	CALWORD4	Status		RAM
9	5	CALWORD5	Status		RAM
10	6	PLLLOCKPIN	Status	Read Only: Status of the PLL Lock Pin Driven by the device.	RAM
11	7	/SLEEP	Status	Set Device Sleep mode On when set to "0", Normal Mode when set to "1"	RAM
12	8	/SYNC	Status	If set to "0" this bit forces "/SYNC ; Set to "1" to exit the Synchronization State.	RAM
13	9	RESERVED			RAM
14	10	VERSION0		Silicon Revision	RAM
15	11	VERSION1		Silicon Revision	RAM
16	12	VERSION2		Silicon Revision	RAM
17	13	RESERVED	—	Must be set to "0"	RAM
18	14	CALWORD_IN0	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
19	15	CALWORD_IN1	Diagnostics		RAM
20	16	CALWORD_IN2	Diagnostics		RAM
21	17	CALWORD_IN3	Diagnostics		RAM
22	18	CALWORD_IN4	Diagnostics		RAM
23	19	CALWORD_IN5	Diagnostics		RAM
24	20	RESERVED	—	Must be set to "0"	RAM
25	21	*TITSTCFG0*	Diagnostics	*TI Test Registers. For TI Use Only*	RAM
26	22	*TITSTCFG1*	Diagnostics		RAM
27	23	*TITSTCFG2*	Diagnostics		RAM
28	24	*TITSTCFG3*	Diagnostics		RAM
29	25	PRIACTIVITY	Status	Synthesizer Source Indicator (27:25) 0 0 1 Primary Input 0 1 0 Secondary Input 1 0 0 Auxiliary Input	RAM
30	26	SECACTIVITY	Status		RAM
31	27	AUXACTIVITY	Status		RAM

Device Control

Figure 22 provides a conceptual explanation of the CDCE62005 Device operation. Table 15 defines how the device behaves in each of the operational states.

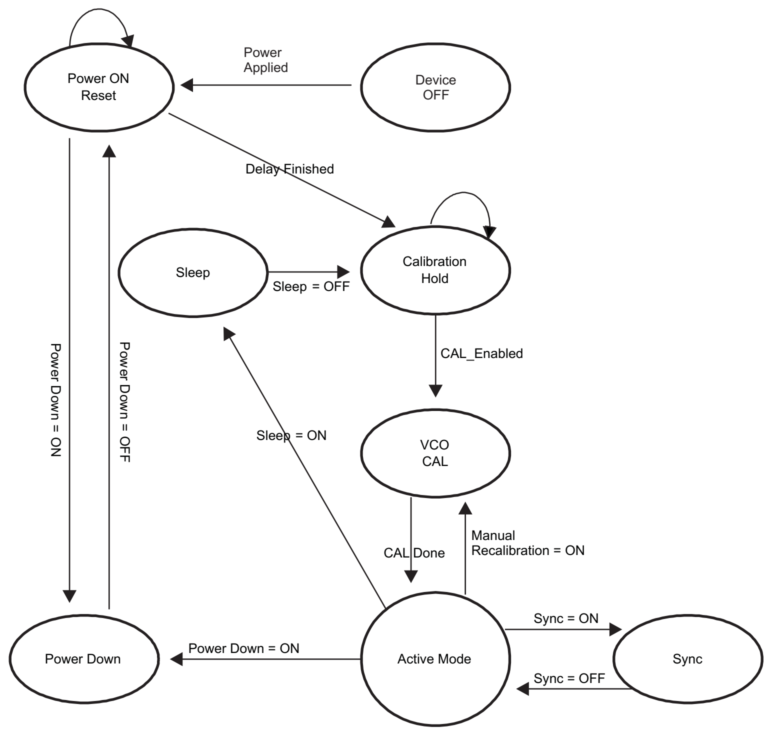


Figure 22. CDCE62005 Device State Control Diagram

Table 15. CDCE62005 Device State Definitions

State	Device Behavior	Entered Via	Exited Via	Status			
				SPI Port	PLL	Output Divider	Output Buffer
Power-On Reset	After device power supply reaches approximately 2.35 V, the contents of EEPROM are copied into the Device Registers, thereby initializing the device hardware.	Power applied to the device or upon exit from Power Down State via the Power_Down pin set HIGH.	Power On Reset and EEPROM loading delays are finished OR the Power_Down pin is set LOW.	OFF	Disabled	Disabled	OFF
Calibration Hold	The device waits until either ENCAL_MODE (Device Register 6 bit 27) is low (Start up calibration enabled) or both ENCAL_MODE is high (Manual Calibration Enabled) AND ENCAL (Device Register 6 bit 22) transitions from a low to a high signaling the device.	Delay process in the Power-On Reset State is finished or Sleep Mode (Sleep bit is in Register 8 bit 7) is turned OFF while in the Sleep State. Power Down must be OFF to enter the Calibration Hold State.	The device waits until either ENCAL_MODE (Device Register 6 bit 27) is low (Start up calibration enabled) or both ENCAL_MODE is high (Manual Calibration Enabled) AND ENCAL (Device Register 6 bit 22) transitions from a low to a high signaling the device	ON	Enabled	Disabled	OFF
VCO CAL	The voltage controlled oscillator is calibrated based on the PLL settings and the incoming reference clock. After the VCO has been calibrated, the device enters Active Mode automatically.	**Calibration Hold:** CAL Enabled becomes true when either ENCAL_MODE (Device Register 6 bit 27) is low or both ENCAL_MODE is high AND ENCAL (Device Register 6 bit 22) transitions from a low to a high. **Active Mode:** A Manual Recalibration is requested. This is initiated by setting ENCAL_MODE to HIGH (Manual Calibration Enabled) AND initiating a calibration sequence by applying a LOW to HIGH transition on ENCAL.	Calibration Process in completed	ON	Enabled	Disabled	OFF
Active Mode	Normal Operation	CAL Done (VCO calibration process finished) or Sync = OFF (from Sync State).	Sync, Power Down, Sleep, or Manual Recalibration activated.	ON	Enabled	Disabled or Enabled	Disabled or Enabled

Table 15. CDCE62005 Device State Definitions (continued)

State	Device Behavior	Entered Via	Exited Via	Status			
				SPI Port	PLL	Output Divider	Output Buffer
Power Down	Used to shut down all hardware and Resets the device after exiting the Power Down State. Therefore, the EEPROM contents will eventually be copied into RAM after the Power Down State is exited.	Power_Down pin is pulled LOW.	Power_Down pin is pulled HIGH.	ON	Disabled	Disabled	Disabled
Sleep	Identical to the Power Down State except the EEPROM contents are not copied into RAM.	Sleep bit in device register 8 bit 7 is set LOW.	Sleep bit in device register 8 bit 7 is set HIGH.	ON	Disabled	Disabled	Disabled
Sync	Sync synchronizes all output dividers so that they begin counting at the same time. Note: this operation is performed automatically each time a divider register is accessed.	Sync Bit in device register 8 bit 8 is set LOW or Sync pin is pulled LOW	Sync Bit in device register 8 bit 8 is set HIGH or Sync pin is pulled HIGH	ON	Enabled	Disabled	Disabled

External Control Pins

REF_SEL

REF_SEL provides a way to switch between the primary and secondary reference inputs (PRI_IN and SEC_IN) via an external signal. It works in conjunction with the smart multiplexer discussed in the Input Block section.

Power_Down

The Power_Down pin places the CDCE62005 into the power down state . Additionally, the CDCE62005 loads the contents of the EEPROM into RAM after the Power_Down pin is de-asserted; therefore, it is used to initialize the device after power is applied. SPI_LE signal has to be HIGH in order for EEPROM to load correctly during the rising edge of Power_Down.

SYNC

The SYNC pin (Active LOW) has a complementary register location located in Device Register 8 bit 8. When enabled, Sync synchronizes all output dividers so that they begin counting simultaneously. Further, SYNC disables all outputs when in the active state. NOTE: The output synchronization does not work for reference input frequencies less than 1 MHz.

INPUT BLOCK

The Input Block includes two Universal Input Buffers, an Auxiliary Input, and a Smart Multiplexer. The Input Block drives three different clock signals onto the Internal Clock Distribution Bus: buffered versions of both the primary and secondary inputs (PRI_IN and SEC_IN) and the output of the Smart Multiplexer.

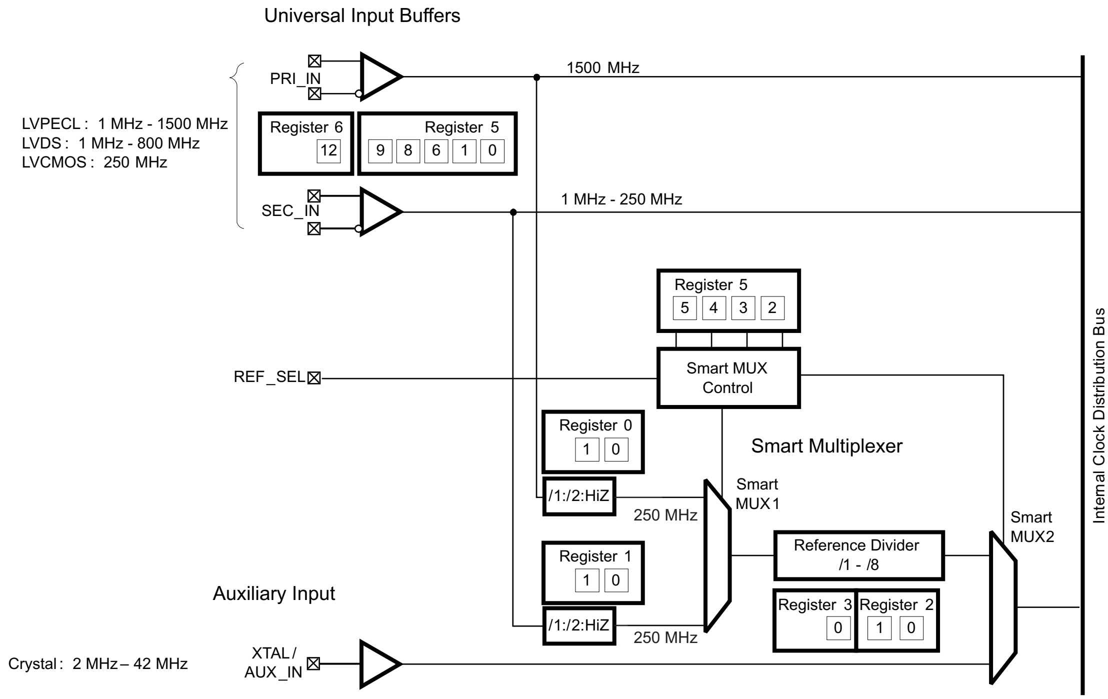
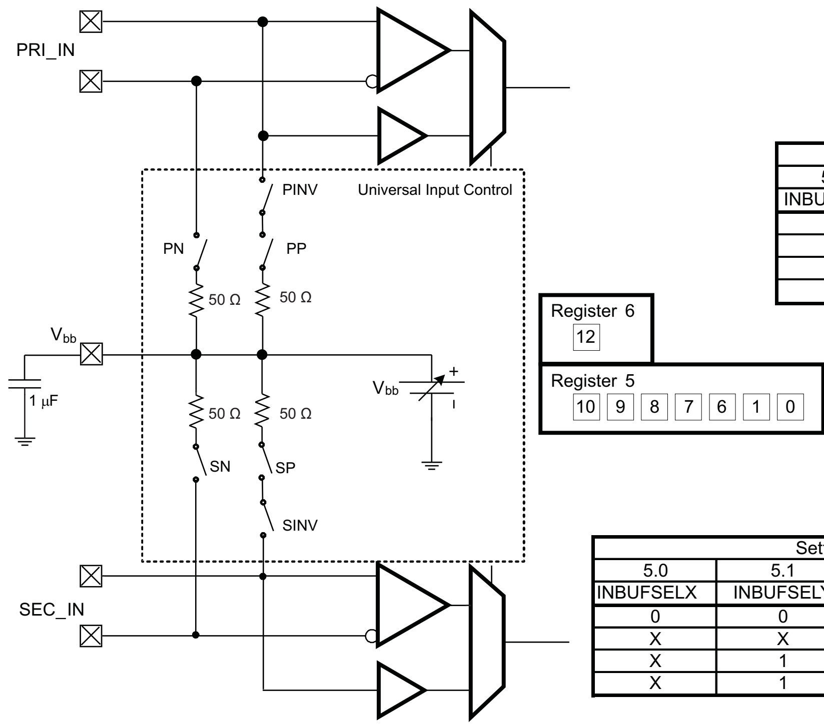


Figure 23. CDCE62005 Input Block With References to Registers

Universal Input Buffers (UIB)

Figure 24 shows the key elements of a universal input buffer. A UIB supports multiple formats along with different termination and coupling schemes. The CDCE62005 implements the UIB by including on board switched termination, a programmable bias voltage generator, and an output multiplexer. The CDCE62005 provides a high degree of configurability on the UIB to facilitate most existing clock input formats.



Settings			Nominal Vbb
5.1	5.0	5.6	
INBUFSELY	INBUFSELX	ACDCSEL	
1	0	0	1.9V
1	0	1	1.2V
1	1	0	1.2V
1	1	1	1.2V

Settings				SWITCH Status		
5.0	5.1	5.8, 6.12	5.9,5.10			
INBUFSELX	INBUFSELY	TERMSEL	INVBB	P	N	INV
0	0	X	X	OFF	OFF	OFF
X	X	1	X	OFF	OFF	OFF
X	1	0	0	ON	ON	ON
X	1	0	1	ON	ON	OFF

Figure 24. CDCE62005 Universal Input Buffer

Table 16 lists several settings for many possible clock input scenarios. Note that the two universal input buffers share the Vbb generator. Therefore, if both inputs use internal termination, they must use the same configuration mode (LVDS, LVPECL, or LVCMOS). If the application requires different modes (e.g. LVDS and LVPECL) then one of the two inputs must implement external termination.

Table 16. CDCE62005 Universal Input Buffer Configuration Matrix

PRI_IN CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	5.8	5.9	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	PRI_TERMSEL	PRIINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
	1	0	0	X	X	X	ENABLED	LVCMOS	DC	N/A	—
	1	1	0	0	0	0	ENABLED	LVPECL	AC	Internal	1.9V
	1	1	0	0	0	1	ENABLED	LVPECL	DC	Internal	1.2V
	1	1	0	1	X	X	ENABLED	LVPECL	—	External	—
	1	1	1	0	0	0	ENABLED	LVDS	AC	Internal	1.2V
	1	1	1	0	0	1	ENABLED	LVDS	DC	Internal	1.2V
	1	1	1	1	X	X	ENABLED	LVDS	—	External	—
	0	X	X	X	X	X	OFF	—	—	—	—
	1	X	X	X	X	X	ENABLED	—	—	—	—
SEC_IN CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	6.12	5.10	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	SEC_TERMSEL	SECINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
	1	0	0	X	X	X	ENABLED	LVCMOS	DC	N/A	—

Table 16. CDCE62005 Universal Input Buffer Configuration Matrix (continued)

PRI_IN CONFIGURATION MATRIX											
	SETTINGS						CONFIGURATION				
Register.Bit →	5.7	5.1	5.0	5.8	5.9	5.6					
Bit Name →	HYSTEN	INBUFSELY	INBUFSELX	PRI_TERMSEL	PRIINVBB	ACDCSEL	Hysteresis	Mode	Coupling	Termination	Vbb
	1	1	0	0	0	0	ENABLED	LVPECL	AC	Internal	1.9V
	1	1	0	0	0	1	ENABLED	LVPECL	DC	Internal	1.2V
	1	1	0	1	X	X	ENABLED	LVPECL	—	External	—
	1	1	1	0	0	0	ENABLED	LVDS	AC	Internal	1.2V
	1	1	1	0	0	1	ENABLED	LVDS	DC	Internal	1.2V
	1	1	1	1	X	X	ENABLED	LVDS	—	External	—
	0	X	X	X	X	X	OFF	—	—	—	—
	1	X	X	X	X	X	ENABLED	—	—	—	—

LVDS Fail Safe Mode

Differential data line receivers can switch on noise in the absence of an input signal. This occurs when the bus driver is turned off or the interconnect is damaged or missing. Traditionally the solution to this problem involves incorporating an external resistor network on the receiver input. This network applies a steady-state bias voltage to the input pins. The additional cost of the external components notwithstanding, the use of such a network lowers input signal magnitude and thus reduces the differential noise margin. The CDCE62005 provides internal failsafe circuitry on all LVDS inputs if enabled as shown in Table 17 for DC termination only.

Table 17. LVDS Failsafe Settings

Bit Name → Register.Bit →	FAILSAFE 5.11	LVDS Failsafe
	0	Disabled for all inputs
	1	Enabled for all inputs

Smart Multiplexer Controls

The smart multiplexer implements a configurable switching mechanism suitable for many applications in which fault tolerance is a design consideration. It includes the multiplexer itself along with three dividers. With respect to the multiplexer control, Table 18 provides an overview of the configurations supported by the CDCE62005.

Table 18. CDCE62005 Smart Multiplexer Settings

REGISTER 5 SETTINGS				SMART MULTIPLEXER MODE
EECLKSEL	AUXSEL	SECSEL	PRISEL	
5.5	5.4	5.3	5.2	
1	0	0	1	Manual Mode: PRI_IN selected
1	0	1	0	Manual Mode: SEC_IN selected
1	1	0	0	Manual Mode: AUX_IN selected
1	0	1	1	Auto MOde: PRI_IN then SEC_IN
1	1	1	1	Auto Mode: PRI_IN then SEC_IN then AUX_IN
0	X	1	1	REF_SEL pin selects PRI_IN or SEC_IN

Smart Multiplexer Auto Mode

Smart Multiplexer Auto Mode switches automatically between clock inputs based on a prioritization scheme shown in Table 18. If using the Smart Multiplexer Auto Mode, the frequencies of the clock inputs may differ by up to 20%. The phase relationship between clock inputs has no restriction.

Upon the detection of a loss of signal on the highest priority clock, the smart multiplex switches its output to the next highest priority clock on the first incoming rising edge of the next highest priority clock. During this switching operation, the output of the smart multiplexer is low. Upon restoration of the higher priority clock, the smart multiplexer waits until it detects four complete cycles from the higher priority clock prior to switching the output of the smart multiplexer back to the higher priority clock. During this switching operation, the output of the smart multiplexer remains high until the next falling edge as shown in Figure 25.

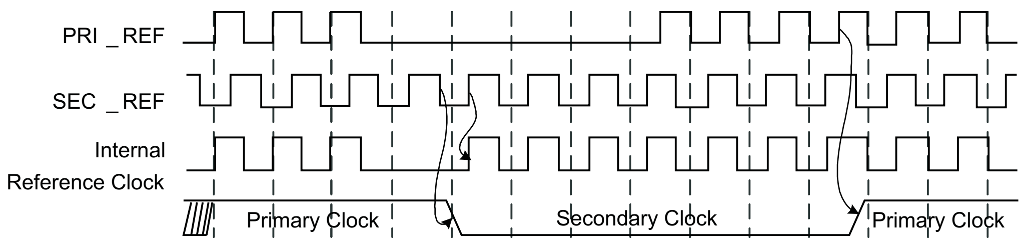


Figure 25. CDCE62005 Smart Multiplexer Timing Diagram

Smart Multiplexer Dividers

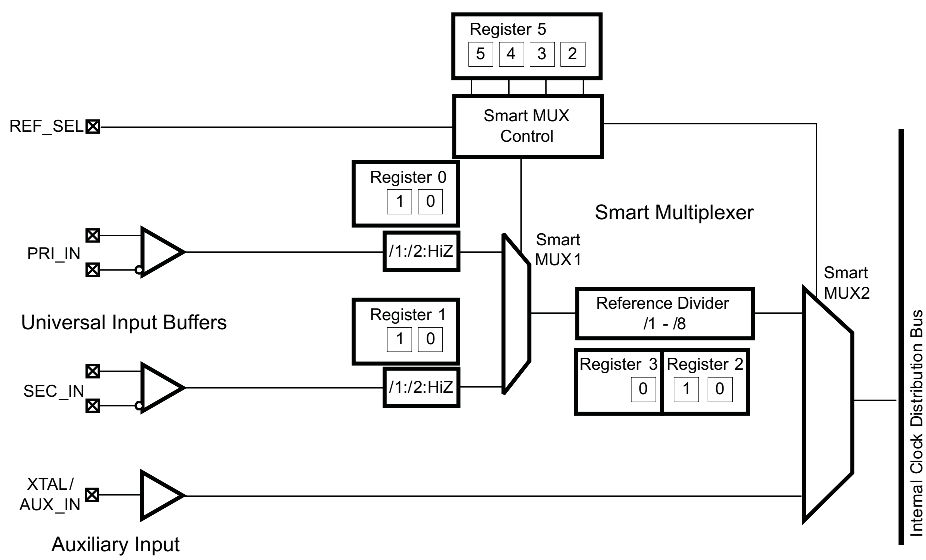


Figure 26. CDCE62005 Smart Multiplexer

The CDCE62005 Smart Multiplexer Block provides the ability to divide the primary and secondary UIB or to disconnect a UIB from the first state of the smart multiplexer altogether.

Table 19. CDCE62005 Pre-Divider Settings

	Primary Pre-Divider					Secondary Pre-Divider		
Bit Name → Register.Bit →	DIV2PRIY 0.1	DIV2PRIX 0.0	Divide Ratio		Bit Name → Register.Bit →	DIV2SECY 1.1	DIV2SECX 1.0	Divide Ratio
	0	0	Hi-Z			0	0	Hi-Z
	0	1	/2			0	1	/2
	1	0	/1			1	0	/1
	1	1	Reserved			1	1	Reserved

The CDCE62005 provides a Reference Divider that divides the clock exiting the first multiplexer stage; thus dividing the primary (PRI_IN) or the secondary input (SEC_IN).

Table 20. CDCE62005 Reference Divider Settings

	Reference Divider			
Bit Name → Register.Bit →	REFDIV2 3.0	REFDIV1 2.1	REFDIV0 2.0	Divide Ratio
	0	0	0	/1
	0	0	1	/2
	0	1	0	/3
	0	1	1	/4
	1	0	0	/5
	1	0	1	/6
	1	1	0	/7
	1	1	1	/8

Auxiliary Input Port

The auxiliary input on the CDCE62005 is designed to connect to an AT-Cut Crystal with a load capacitance of 8 to 10pF. One side of the crystal connects to Ground while the other side connects to the Auxiliary input of the device. The circuit works optimally between 20 to 40MHz but it can accept crystals from 2 to 42MHz.

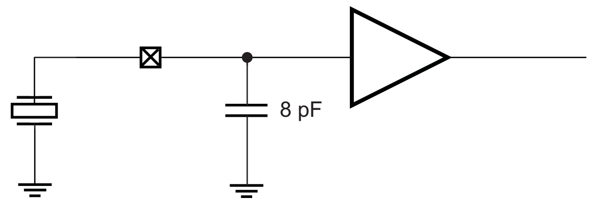


Figure 27. CDCE62005 Auxiliary Input Port

OUTPUT BLOCK

The output block includes five identical output channels. Each output channel comprises an output multiplexer, a clock divider module, and a universal output buffer as shown in Figure 28.

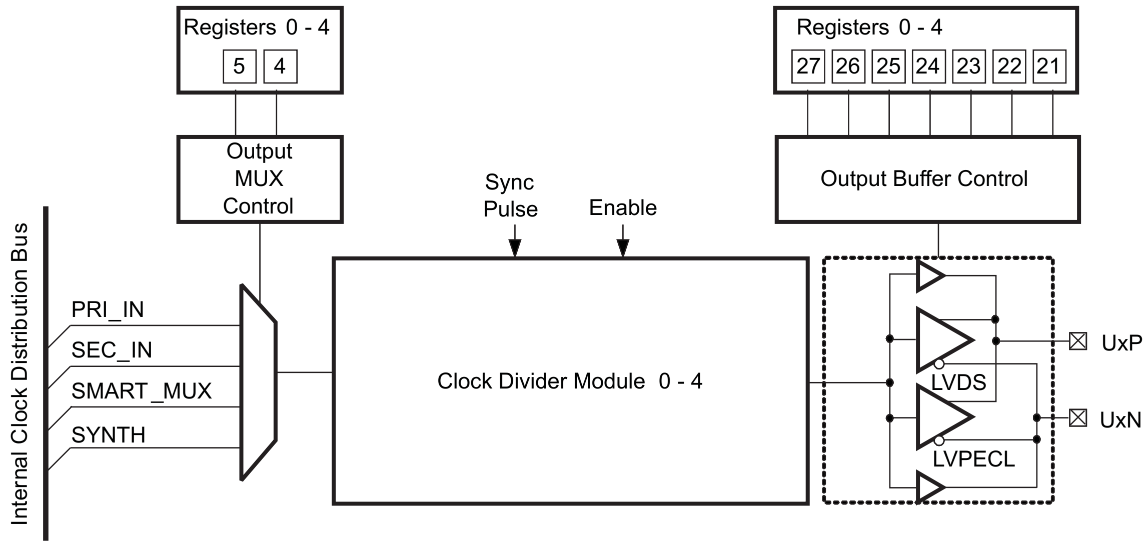


Figure 28. CDCE62005 Output Channel

Output Multiplexer Control

The Clock Divider Module receives the clock selected by the output multiplexer. The output multiplexer selects from one of four clock sources available on the Internal Clock Distribution. For a description of PRI_IN, SEC_IN, and SMART_MUX, see Figure 23. For a description of SYNTH, see Figure 34.

Table 21. CDCE62005 Output Multiplexer Control Settings

OUTPUT MULTIPLEXER CONTROL		
Register n (n = 0,1,2,3,4)		
OUTMUXnSELX n.4	OUTMUXnSELY n.5	CLOCK SOURCE SELECTED
0	0	PRI_IN
0	1	SEC_IN
1	0	SMART_MUX
1	1	SYNTH

Output Buffer Control

Each of the five output channels includes a programmable output buffer; supporting LVPECL, LVDS, and LVCMOS modes. Table 22 lists the settings required to configure the CDCE62005 for each output type. Registers 0 through 4 correspond to Output Channels 0 through 4 respectively.

Table 22. CDCE62005 Output Buffer Control Settings

OUTPUT BUFFER CONTROL						OUTPUT TYPE
Register n (n = 0,1,2,3,4)						
CMOSMODEnPX	CMOSMODEnPY	CMOSMODEnNX	CMOSMODEnNY	OUTBUFSELnX	OUTBUFSELnY	
n.22	n.23	n.24	n.25	n.26	n.27	
0	0	0	0	0	1	LVPECL
0	1	0	1	1	1	LVDS
See LVCMOS Output Buffer Configuration Settings				0	0	LVCMOS
0	1	0	1	1	0	OFF

Output Buffer Control – LVCMOS Configurations

A LVCMOS output configuration requires additional configuration data. In the single ended configuration, each Output Channel provides a pair of outputs. The CDCE62005 supports four modes of operation for single ended outputs as listed in Table 23.

Table 23. LVCMOS Output Buffer Configuration Settings

OUTPUT BUFFER CONTROL – LVCMOS CONFIGURATION						Output Type	Pin	Output Mode
Register n (n = 0,1,2,3,4)								
CMOSMODEnPX	CMOSMODEnPY	CMOSMODEnNX	CMOSMODEnNY	OUTBUFSELnX	OUTBUFSELnY			
n.22	n.23	n.24	n.25	n.26	n.27			
X	X	0	0	0	0	LVCMOS	Negative	Active – Non-inverted
X	X	0	1	0	0	LVCMOS	Negative	Hi-Z
X	X	1	0	0	0	LVCMOS	Negative	Active – Non-inverted
X	X	1	1	0	0	LVCMOS	Negative	Low
0	0	X	X	0	0	LVCMOS	Positive	Active – Non-inverted
0	1	X	X	0	0	LVCMOS	Positive	Hi-Z
1	0	X	X	0	0	LVCMOS	Positive	Active – Non-inverted
1	1	X	X	0	0	LVCMOS	Positive	Low

Output Dividers

Figure 29 shows that each output channel provides a 7-bit divider and digital phase adjust block. The Output Divider Settings lists the divide ratios supported by the output divider for each output channel. Figure 30 illustrates the output divider architecture in detail. The Prescaler provides an array of low noise dividers with duty cycle correction. The Integer Divider includes a final divide by two stage which is used to correct the duty cycle of the /1–/8 stage. The output divider's maximum input frequency is limited to 1.175GHz. If the divider is bypassed (divide ratio = 1) then the maximum frequency of the output channel is 1.5GHz.

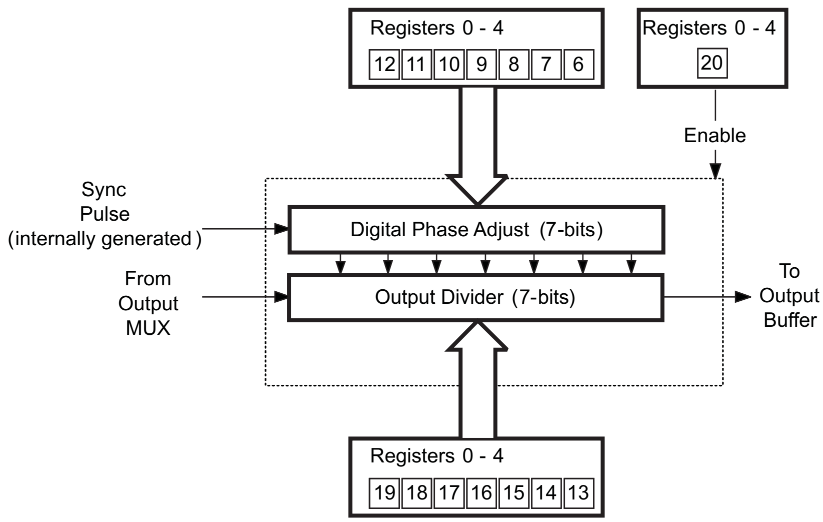


Figure 29. CDCE62005 Output Divider and Phase Adjust

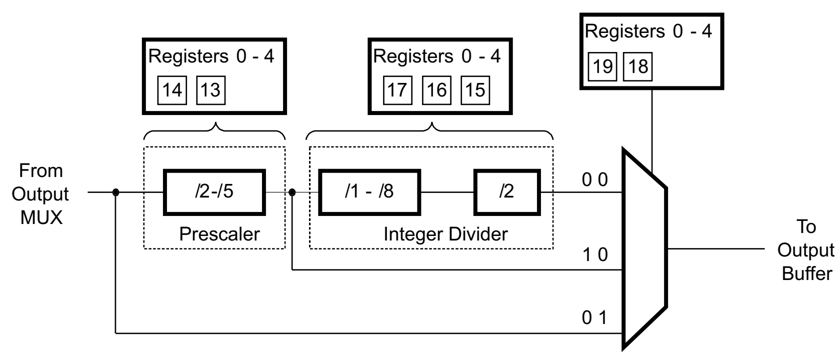


Figure 30. CDCE62005 Output Divider Architecture

CDCE62005 Output Divider Settings

OUTPUT DIVIDER n SETTINGSRegister n (n = 0,1,2,3,4)										Output Phase*		Output Divide Ratio	
Multiplexer		Integer Divider			Prescaler								
OUTnDIVSEL6	OUTnDIVSEL5	OUTnDIVSEL4	OUTnDIVSEL3	OUTnDIVSEL2	OUTnDIVSEL1	OutnDIVSEL0	OUTnDIVSEL	Prescaler Setting	Integer Divider Setting				
n.19	n.18	n.17	n.16	n.15	n.14	n.13	n.20			Cycles	Degree	Output Channels 0-4	Auxiliary Output
X	X	X	X	X	X	X	0			OFF	OFF	OFF	OFF
0	1	0	0	0	0	0	1	–	–	0	0	1	OFF
1	0	0	0	0	0	0	1	2	–	0.5	180	2**	4
1	0	0	0	0	0	1	1	3	–	0	0	3**	6
1	0	0	0	0	1	0	1	4	–	0.5	180	4	8
1	0	0	0	0	1	1	1	5	–	0	0	5	10
0	0	0	0	0	0	1	1	3	2	21	7560	6	6
0	0	0	0	0	1	0	1	4	2	28.5	10260	8	8
0	0	0	0	0	1	1	1	5	2	35	12500	10	10
0	0	0	0	1	0	1	1	3	4	24	8640	12	12
0	0	0	0	1	1	0	1	4	4	32.5	11700	16	16
0	0	0	0	1	1	1	1	5	4	40	14400	20	20
0	0	0	1	0	0	1	1	3	6	27	9720	18	18
0	0	0	1	0	1	0	1	4	6	36.5	13140	24	24
0	0	0	1	0	1	1	1	5	6	45	16200	30	30
0	0	0	1	1	1	0	1	4	8	40.5	14580	32	32
0	0	0	1	1	1	1	1	5	8	50	18000	40	40
0	0	1	0	0	1	1	1	5	10	55	19800	50	50
0	0	1	0	1	0	1	1	3	12	36	12960	36	36
0	0	1	0	1	1	0	1	4	12	48.5	17460	48	48
0	0	1	0	1	1	1	1	5	12	60	21600	60	60
0	0	1	1	0	0	0	1	2	14	25.5	9540	28	28
0	0	1	1	0	0	1	1	3	14	39	14040	42	42
0	0	1	1	0	1	0	1	4	14	52.5	18900	56	56
0	0	1	1	0	1	1	1	5	14	65	23400	70	70
0	0	1	1	1	1	0	1	4	16	56.5	20340	64	64
0	0	1	1	1	1	1	1	5	16	70	25200	80	80

*These columns show that the output divider generates a unique phase lag in the output clock (relative to the clock from the output multiplexer) determined by the divide ratio used.

**Output channel 2 or 3 determine the auxiliary output divide ratio. For example, if the auxiliary output is programmed to drive via output 2 and output 2 divider is programmed to divide by 3, then the divide ratio for the auxiliary output will be 6.

Digital Phase Adjust

Figure 31 provides an overview of the Digital Phase Adjust feature. The output divider includes a coarse phase adjust that shifts the divided clock signal that drives the output buffer. Essentially, the Digital Phase Adjust timer delays when the output divider starts dividing; thereby shifting the phase of the output clock. The phase adjust resolution is a function of the divide function. Coarse phase adjust parameters include:

- Number of Phase Delay Steps – the number of phase delay steps available is equal to the divide ratio selected. For example, if a Divide by 4 is selected, then the Digital Phase Adjust can be programmed to select when the output divider changes state based upon selecting one of the four counts on the input. Figure 31 shows an example of divide by 16 in which there are 16 rising edges of Clock IN at which the output divider changes state (this particular example shows the fourth edge shifting the output by one fourth of the period of the output).
- Phase Delay Step Size – the step size is determined by the number of phase delay steps according to the following equations:

$$\text{Stepsize(deg)} = \frac{360\ \text{degrees}}{\text{OutputDivideRatio}} \tag{4}$$

$$\text{Stepsize(sec)} = \frac{\frac{1}{f_{\text{ClockIN}}}}{\text{OutputDivideRatio}} \tag{5}$$

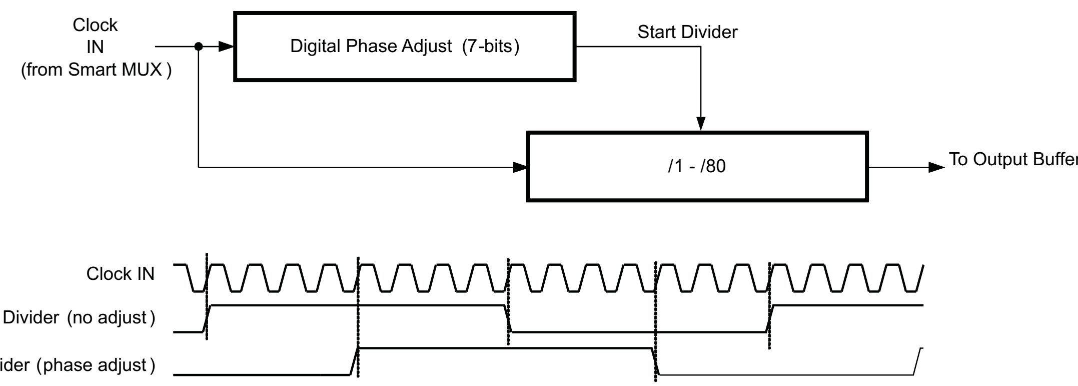


Figure 31. CDCE62005 Phase Adjust

Phase Adjust example

Given:

Output Frequency: 30.72 MHz

VCO Operating Frequency: 1966.08 MHz

Prescaler Divider Setting: 2

Output Divider Setting: 32

$$\text{Stepsize(deg)} = \frac{360}{32} = 11.25° / \text{Step} \tag{6}$$

The tables that follow provide a list of valid register settings for the digital phase adjust blocks.

Table 24. CDCE62005 Output Coarse Phase Adjust Settings (1)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/2)
3	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/3)
	0	0	0	0	0	1	0	2(2π/3)
4	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/4)
	0	0	0	0	0	1	0	2(2π/4)
	0	0	0	0	0	1	1	3(2π/4)
5	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/5)
	0	0	0	0	0	1	0	2(2π/5)
	0	0	0	0	0	1	1	3(2π/5)
	0	0	0	0	1	0	0	4(2π/5)
6	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/6)
	0	0	0	0	0	1	0	2(2π/6)
	1	0	0	0	0	0	0	3(2π/6)
	1	0	0	0	0	0	1	4(2π/6)
	1	0	0	0	0	1	0	5(2π/6)
8	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/8)
	0	0	0	0	0	1	0	2(2π/8)
	0	0	0	0	0	1	1	3(2π/8)
	1	0	0	0	0	0	0	4(2π/8)
	1	0	0	0	0	0	1	5(2π/8)
	1	0	0	0	0	1	0	6(2π/8)
	1	0	0	0	0	1	1	7(2π/8)
10	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/10)
	0	0	0	0	0	1	0	2(2π/10)
	0	0	0	0	0	1	1	3(2π/10)
	0	0	0	0	1	0	0	4(2π/10)
	1	0	0	0	0	0	0	5(2π/10)
	1	0	0	0	0	0	1	6(2π/10)
	1	0	0	0	0	1	0	7(2π/10)
	1	0	0	0	0	1	1	8(2π/10)
	1	0	0	0	1	0	0	9(2π/10)
12	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/12)
	0	0	0	0	0	1	0	2(2π/12)
	0	0	0	1	0	0	0	3(2π/12)
	0	0	0	1	0	0	1	4(2π/12)
	0	0	0	1	0	1	0	5(2π/12)
	0	0	1	0	0	0	0	6(2π/12)
	0	0	1	0	0	0	1	7(2π/12)
	0	0	1	0	0	1	0	8(2π/12)
	0	0	1	1	0	0	0	9(2π/12)
	0	0	1	1	0	0	1	10(2π/12)
	0	0	1	1	0	1	0	11(2π/12)
16	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/16)
	0	0	0	0	0	1	0	2(2π/16)
	0	0	0	0	0	1	1	3(2π/16)
	0	0	0	1	0	0	0	4(2π/16)
	0	0	0	1	0	0	1	5(2π/16)
	0	0	0	1	0	1	0	6(2π/16)
	0	0	0	1	0	1	1	7(2π/16)
	0	0	1	0	0	0	0	8(2π/16)
	0	0	1	0	0	0	1	9(2π/16)
	0	0	1	0	0	1	0	10(2π/16)
	0	0	1	0	0	1	1	11(2π/16)
	0	0	1	1	0	0	0	12(2π/16)
	0	0	1	1	0	0	1	13(2π/16)
	0	0	1	1	0	1	0	14(2π/16)
	0	0	1	1	0	1	1	15(2π/16)
18	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/18)
	0	0	0	0	0	1	0	2(2π/18)
	0	0	0	1	0	0	0	3(2π/18)
	0	0	0	1	0	0	1	4(2π/18)
	0	0	0	1	0	1	0	5(2π/18)
	0	0	1	0	0	0	0	6(2π/18)
	0	0	1	0	0	0	1	7(2π/18)
	0	0	1	0	0	1	0	8(2π/18)
	0	0	1	1	0	0	0	9(2π/18)
	0	0	1	1	0	0	1	10(2π/18)
	0	0	1	1	0	1	0	11(2π/18)
	0	1	0	0	0	0	0	12(2π/18)
	0	1	0	0	0	0	1	13(2π/18)
	0	1	0	0	0	1	0	14(2π/18)
	0	1	0	1	0	0	0	15(2π/18)
	0	1	0	1	0	0	1	16(2π/18)
	0	1	0	1	0	1	0	17(2π/18)
20	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/20)
	0	0	0	0	0	1	0	2(2π/20)
	0	0	0	0	0	1	1	3(2π/20)
	0	0	0	0	1	0	0	4(2π/20)
	0	0	0	1	0	0	0	5(2π/20)
	0	0	0	1	0	0	1	6(2π/20)
	0	0	0	1	0	1	0	7(2π/20)
	0	0	0	1	0	1	1	8(2π/20)
	0	0	0	1	1	0	0	9(2π/20)
	0	0	1	0	0	0	0	10(2π/20)
	0	0	1	0	0	0	1	11(2π/20)
	0	0	1	0	0	1	0	12(2π/20)
	0	0	1	0	0	1	1	13(2π/20)
	0	0	1	0	1	0	0	14(2π/20)
	0	0	1	1	0	0	0	15(2π/20)
	0	0	1	1	0	0	1	16(2π/20)
	0	0	1	1	0	1	0	17(2π/20)
	0	0	1	1	0	1	1	18(2π/20)
	0	0	1	1	1	0	0	19(2π/20)
24	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/24)
	0	0	0	0	0	1	0	2(2π/24)
	0	0	0	0	0	1	1	3(2π/24)
	0	0	0	1	0	0	0	4(2π/24)
	0	0	0	1	0	0	1	5(2π/24)
	0	0	0	1	0	1	0	6(2π/24)
	0	0	0	1	0	1	1	7(2π/24)
	0	0	1	0	0	0	0	8(2π/24)
	0	0	1	0	0	0	1	9(2π/24)
	0	0	1	0	0	1	0	10(2π/24)
	0	0	1	0	0	1	1	11(2π/24)
	0	0	1	1	0	0	0	12(2π/24)
	0	0	1	1	0	0	1	13(2π/24)
	0	0	1	1	0	1	0	14(2π/24)
	0	0	1	1	0	1	1	15(2π/24)
	0	1	0	0	0	0	0	16(2π/24)
	0	1	0	0	0	0	1	17(2π/24)
	0	1	0	0	0	1	0	18(2π/24)
	0	1	0	0	0	1	1	19(2π/24)
	0	1	0	1	0	0	0	20(2π/24)
	0	1	0	1	0	0	1	21(2π/24)
	0	1	0	1	0	1	0	22(2π/24)
	0	1	0	1	0	1	1	23(2π/24)

Table 25. CDCE62005 Output Coarse Phase Adjust Settings (2)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
28	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/28)
	0	0	0	1	0	0	0	2(2π/28)
	0	0	0	1	0	0	1	3(2π/28)
	0	0	1	0	0	0	0	4(2π/28)
	0	0	1	0	0	0	1	5(2π/28)
	0	0	1	1	0	0	0	6(2π/28)
	0	0	1	1	0	0	1	7(2π/28)
	0	1	0	0	0	0	0	8(2π/28)
	0	1	0	0	0	0	1	9(2π/28)
	0	1	0	1	0	0	0	10(2π/28)
	0	1	0	1	0	0	1	11(2π/28)
	0	1	1	0	0	0	0	12(2π/28)
	0	1	1	0	0	0	1	13(2π/28)
	1	0	0	0	0	0	0	14(2π/28)
	1	0	0	0	0	0	1	15(2π/28)
	1	0	0	1	0	0	0	16(2π/28)
	1	0	0	1	0	0	1	17(2π/28)
	1	0	1	0	0	0	0	18(2π/28)
	1	0	1	0	0	0	1	19(2π/28)
	1	0	1	1	0	0	0	20(2π/28)
	1	0	1	1	0	0	1	21(2π/28)
	1	1	0	0	0	0	0	22(2π/28)
	1	1	0	0	0	0	1	23(2π/28)
	1	1	0	1	0	0	0	24(2π/28)
	1	1	0	1	0	0	1	25(2π/28)
	1	1	1	0	0	0	0	26(2π/28)
	1	1	1	0	0	0	1	27(2π/28)
30	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/30)
	0	0	0	0	0	1	0	2(2π/30)
	0	0	0	0	0	1	1	3(2π/30)
	0	0	0	0	1	0	0	4(2π/30)
	0	0	0	1	0	0	0	5(2π/30)
	0	0	0	1	0	0	1	6(2π/30)
	0	0	0	1	0	1	0	7(2π/30)
	0	0	0	1	0	1	1	8(2π/30)
	0	0	0	1	1	0	0	9(2π/30)
	0	0	1	0	0	0	0	10(2π/30)
	0	0	1	0	0	0	1	11(2π/30)
	0	0	1	0	0	1	0	12(2π/30)
	0	0	1	0	0	1	1	13(2π/30)
	0	0	1	0	1	0	0	14(2π/30)
	0	0	1	1	0	0	0	15(2π/30)
	0	0	1	1	0	0	1	16(2π/30)
	0	0	1	1	0	1	0	17(2π/30)
	0	0	1	1	0	1	1	18(2π/30)
	0	0	1	1	1	0	0	19(2π/30)
	0	1	0	0	0	0	0	20(2π/30)
	0	1	0	0	0	0	1	21(2π/30)
	0	1	0	0	0	1	0	22(2π/30)
	0	1	0	0	0	1	1	23(2π/30)
	0	1	0	0	1	0	0	24(2π/30)
	0	1	0	1	0	0	0	25(2π/30)
	0	1	0	1	0	0	1	26(2π/30)
	0	1	0	1	0	1	0	27(2π/30)
	0	1	0	1	0	1	1	28(2π/30)
	0	1	0	1	1	0	0	29(2π/30)
32	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/32)
	0	0	0	0	0	1	0	2(2π/32)
	0	0	0	0	0	1	1	3(2π/32)
	0	0	0	1	0	0	0	4(2π/32)
	0	0	0	1	0	0	1	5(2π/32)
	0	0	0	1	0	1	0	6(2π/32)
	0	0	0	1	0	1	1	7(2π/32)
	0	0	1	0	0	0	0	8(2π/32)
	0	0	1	0	0	0	1	9(2π/32)
	0	0	1	0	0	1	0	10(2π/32)
	0	0	1	0	0	1	1	11(2π/32)
	0	0	1	1	0	0	0	12(2π/32)
	0	0	1	1	0	0	1	13(2π/32)
	0	0	1	1	0	1	0	14(2π/32)
	0	0	1	1	0	1	1	15(2π/32)
	0	1	0	0	0	0	0	16(2π/32)
	0	1	0	0	0	0	1	17(2π/32)
	0	1	0	0	0	1	0	18(2π/32)
	0	1	0	0	0	1	1	19(2π/32)
	0	1	0	1	0	0	0	20(2π/32)
	0	1	0	1	0	0	1	21(2π/32)
	0	1	0	1	0	1	0	22(2π/32)
	0	1	0	1	0	1	1	23(2π/32)
	0	1	1	0	0	0	0	24(2π/32)
	0	1	1	0	0	0	1	25(2π/32)
	0	1	1	0	0	1	0	26(2π/32)
	0	1	1	0	0	1	1	27(2π/32)
	0	1	1	1	0	0	0	28(2π/32)
	0	1	1	1	0	0	1	29(2π/32)
	0	1	1	1	0	1	0	30(2π/32)
	0	1	1	1	0	1	1	31(2π/32)
36	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/36)
	0	0	0	0	0	1	0	2(2π/36)
	0	0	0	1	0	0	0	3(2π/36)
	0	0	0	1	0	0	1	4(2π/36)
	0	0	0	1	0	1	0	5(2π/36)
	0	0	1	0	0	0	0	6(2π/36)
	0	0	1	0	0	0	1	7(2π/36)
	0	0	1	0	0	1	0	8(2π/36)
	0	0	1	1	0	0	0	9(2π/36)
	0	0	1	1	0	0	1	10(2π/36)
	0	0	1	1	0	1	0	11(2π/36)
	0	1	0	0	0	0	0	12(2π/36)
	0	1	0	0	0	0	1	13(2π/36)
	0	1	0	0	0	1	0	14(2π/36)
	0	1	0	1	0	0	0	15(2π/36)
	0	1	0	1	0	0	1	16(2π/36)
	0	1	0	1	0	1	0	17(2π/36)
	1	0	0	0	0	0	0	18(2π/36)
	1	0	0	0	0	0	1	19(2π/36)
	1	0	0	0	0	1	0	20(2π/36)
	1	0	0	1	0	0	0	21(2π/36)
	1	0	0	1	0	0	1	22(2π/36)
	1	0	0	1	0	1	0	23(2π/36)
	1	0	1	0	0	0	0	24(2π/36)
	1	0	1	0	0	0	1	25(2π/36)
	1	0	1	0	0	1	0	26(2π/36)
	1	0	1	1	0	0	0	27(2π/36)
	1	0	1	1	0	0	1	28(2π/36)
	1	0	1	1	0	1	0	29(2π/36)
	1	1	0	0	0	0	0	30(2π/36)
	1	1	0	0	0	0	1	31(2π/36)
	1	1	0	0	0	1	0	32(2π/36)
	1	1	0	1	0	0	0	33(2π/36)
	1	1	0	1	0	0	1	34(2π/36)
	1	1	0	1	0	1	0	35(2π/36)

Table 26. CDCE62005 Output Coarse Phase Adjust Settings (3)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
40	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/40)
	0	0	0	0	0	1	0	2(2π/40)
	0	0	0	0	0	1	1	3(2π/40)
	0	0	0	0	1	0	0	4(2π/40)
	0	0	0	1	0	0	0	5(2π/40)
	0	0	0	1	0	0	1	6(2π/40)
	0	0	0	1	0	1	0	7(2π/40)
	0	0	0	1	0	1	1	8(2π/40)
	0	0	0	1	1	0	0	9(2π/40)
	0	0	1	0	0	0	0	10(2π/40)
	0	0	1	0	0	0	1	11(2π/40)
	0	0	1	0	0	1	0	12(2π/40)
	0	0	1	0	0	1	1	13(2π/40)
	0	0	1	0	1	0	0	14(2π/40)
	0	0	1	1	0	0	0	15(2π/40)
	0	0	1	1	0	0	1	16(2π/40)
	0	0	1	1	0	1	0	17(2π/40)
	0	0	1	1	0	1	1	18(2π/40)
	0	0	1	1	1	0	0	19(2π/40)
	0	1	0	0	0	0	0	20(2π/40)
	0	1	0	0	0	0	1	21(2π/40)
	0	1	0	0	0	1	0	22(2π/40)
	0	1	0	0	0	1	1	23(2π/40)
	0	1	0	0	1	0	0	24(2π/40)
	0	1	0	1	0	0	0	25(2π/40)
	0	1	0	1	0	0	1	26(2π/40)
	0	1	0	1	0	1	0	27(2π/40)
	0	1	0	1	0	1	1	28(2π/40)
	0	1	0	1	1	0	0	29(2π/40)
	0	1	1	0	0	0	0	30(2π/40)
	0	1	1	0	0	0	1	31(2π/40)
	0	1	1	0	0	1	0	32(2π/40)
	0	1	1	0	0	1	1	33(2π/40)
	0	1	1	0	1	0	0	34(2π/40)
	0	1	1	1	0	0	0	35(2π/40)
	0	1	1	1	0	0	1	36(2π/40)
	0	1	1	1	0	1	0	37(2π/40)
	0	1	1	1	0	1	1	38(2π/40)
	0	1	1	1	1	0	0	39(2π/40)
42	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/42)
	0	0	0	0	0	1	0	2(2π/42)
	0	0	0	1	0	0	0	3(2π/42)
	0	0	0	1	0	0	1	4(2π/42)
	0	0	0	1	0	1	0	5(2π/42)
	0	0	1	0	0	0	0	6(2π/42)
	0	0	1	0	0	0	1	7(2π/42)
	0	0	1	0	0	1	0	8(2π/42)
	0	0	1	1	0	0	0	9(2π/42)
	0	0	1	1	0	0	1	10(2π/42)
	0	0	1	1	0	1	0	11(2π/42)
	0	1	0	0	0	0	0	12(2π/42)
	0	1	0	0	0	0	1	13(2π/42)
	0	1	0	0	0	1	0	14(2π/42)
	0	1	0	1	0	0	0	15(2π/42)
	0	1	0	1	0	0	1	16(2π/42)
	0	1	0	1	0	1	0	17(2π/42)
	0	1	1	0	0	0	0	18(2π/42)
	0	1	1	0	0	0	1	19(2π/42)
	0	1	1	0	0	1	0	20(2π/42)
	1	0	0	0	0	0	0	21(2π/42)
	1	0	0	0	0	0	1	22(2π/42)
	1	0	0	0	0	1	0	23(2π/42)
	1	0	0	1	0	0	0	24(2π/42)
	1	0	0	1	0	0	1	25(2π/42)
	1	0	0	1	0	1	0	26(2π/42)
	1	0	1	0	0	0	0	27(2π/42)
	1	0	1	0	0	0	1	28(2π/42)
	1	0	1	0	0	1	0	29(2π/42)
	1	0	1	1	0	0	0	30(2π/42)
	1	0	1	1	0	0	1	31(2π/42)
	1	0	1	1	0	1	0	32(2π/42)
	1	1	0	0	0	0	0	33(2π/42)
	1	1	0	0	0	0	1	34(2π/42)
	1	1	0	0	0	1	0	35(2π/42)
	1	1	0	1	0	0	0	36(2π/42)
	1	1	0	1	0	0	1	37(2π/42)
	1	1	0	1	0	1	0	38(2π/42)
	1	1	1	0	0	0	0	39(2π/42)
	1	1	1	0	0	0	1	40(2π/42)
	1	1	1	0	0	1	0	41(2π/42)

Divide Ratio	PHnADGC6	PHnADGC5	PHnADGC4	PHnADGC3	PHnADGC2	PHnADGC1	PHnADGC0	Phase Delay
	n.12	n.11	n.10	n.9	n.8	n.7	n.6	(radian)
48	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/48)
	0	0	0	0	0	1	0	2(2π/48)
	0	0	0	0	0	1	1	3(2π/48)
	0	0	0	1	0	0	0	4(2π/48)
	0	0	0	1	0	0	1	5(2π/48)
	0	0	0	1	0	1	0	6(2π/48)
	0	0	0	1	0	1	1	7(2π/48)
	0	0	1	0	0	0	0	8(2π/48)
	0	0	1	0	0	0	1	9(2π/48)
	0	0	1	0	0	1	0	10(2π/48)
	0	0	1	0	0	1	1	11(2π/48)
	0	0	1	1	0	0	0	12(2π/48)
	0	0	1	1	0	0	1	13(2π/48)
	0	0	1	1	0	1	0	14(2π/48)
	0	0	1	1	0	1	1	15(2π/48)
	0	1	0	0	0	0	0	16(2π/48)
	0	1	0	0	0	0	1	17(2π/48)
	0	1	0	0	0	1	0	18(2π/48)
	0	1	0	0	0	1	1	19(2π/48)
	0	1	0	1	0	0	0	20(2π/48)
	0	1	0	1	0	0	1	21(2π/48)
	0	1	0	1	0	1	0	22(2π/48)
	0	1	0	1	0	1	1	23(2π/48)
	1	0	0	0	0	0	0	24(2π/48)
	1	0	0	0	0	0	1	25(2π/48)
	1	0	0	0	0	1	0	26(2π/48)
	1	0	0	0	0	1	1	27(2π/48)
	1	0	0	1	0	0	0	28(2π/48)
	1	0	0	1	0	0	1	29(2π/48)
	1	0	0	1	0	1	0	30(2π/48)
	1	0	0	1	0	1	1	31(2π/48)
	1	0	1	0	0	0	0	32(2π/48)
	1	0	1	0	0	0	1	33(2π/48)
	1	0	1	0	0	1	0	34(2π/48)
	1	0	1	0	0	1	1	35(2π/48)
	1	0	1	1	0	0	0	36(2π/48)
	1	0	1	1	0	0	1	37(2π/48)
	1	0	1	1	0	1	0	38(2π/48)
	1	0	1	1	0	1	1	39(2π/48)
	1	1	0	0	0	0	0	40(2π/48)
	1	1	0	0	0	0	1	41(2π/48)
	1	1	0	0	0	1	0	42(2π/48)
	1	1	0	0	0	1	1	43(2π/48)
	1	1	0	1	0	0	0	44(2π/48)
	1	1	0	1	0	0	1	45(2π/48)
	1	1	0	1	0	1	0	46(2π/48)
	1	1	0	1	0	1	1	47(2π/48)

Table 27. CDCE62005 Output Coarse Phase Adjust Settings (4)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
50	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/50)
	0	0	0	0	0	1	0	2(2π/50)
	0	0	0	0	0	1	1	3(2π/50)
	0	0	0	0	1	0	0	4(2π/50)
	0	0	0	1	0	0	0	5(2π/50)
	0	0	0	1	0	0	1	6(2π/50)
	0	0	0	1	0	1	0	7(2π/50)
	0	0	0	1	0	1	1	8(2π/50)
	0	0	0	1	1	0	0	9(2π/50)
	0	0	1	0	0	0	0	10(2π/50)
	0	0	1	0	0	0	1	11(2π/50)
	0	0	1	0	0	1	0	12(2π/50)
	0	0	1	0	0	1	1	13(2π/50)
	0	0	1	0	1	0	0	14(2π/50)
	0	0	1	1	0	0	0	15(2π/50)
	0	0	1	1	0	0	1	16(2π/50)
	0	0	1	1	0	1	0	17(2π/50)
	0	0	1	1	0	1	1	18(2π/50)
	0	0	1	1	1	0	0	19(2π/50)
	0	1	0	0	0	0	0	20(2π/50)
	0	1	0	0	0	0	1	21(2π/50)
	0	1	0	0	0	1	0	22(2π/50)
	0	1	0	0	0	1	1	23(2π/50)
	0	1	0	0	1	0	0	24(2π/50)
	1	0	0	0	0	0	0	25(2π/50)
	1	0	0	0	0	0	1	26(2π/50)
	1	0	0	0	0	1	0	27(2π/50)
	1	0	0	0	0	1	1	28(2π/50)
	1	0	0	0	1	0	0	29(2π/50)
	1	0	0	1	0	0	0	30(2π/50)
	1	0	0	1	0	0	1	31(2π/50)
	1	0	0	1	0	1	0	32(2π/50)
	1	0	0	1	0	1	1	33(2π/50)
	1	0	0	1	1	0	0	34(2π/50)
	1	0	1	0	0	0	0	35(2π/50)
	1	0	1	0	0	0	1	36(2π/50)
	1	0	1	0	0	1	0	37(2π/50)
	1	0	1	0	0	1	1	38(2π/50)
	1	0	1	0	1	0	0	39(2π/50)
	1	0	1	1	0	0	0	40(2π/50)
	1	0	1	1	0	0	1	41(2π/50)
	1	0	1	1	0	1	0	42(2π/50)
	1	0	1	1	0	1	1	43(2π/50)
	1	0	1	1	1	0	0	44(2π/50)
	1	1	0	0	0	0	0	45(2π/50)
	1	1	0	0	0	0	1	46(2π/50)
	1	1	0	0	0	1	0	47(2π/50)
	1	1	0	0	0	1	1	48(2π/50)
	1	1	0	0	1	0	0	49(2π/50)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
56	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/56)
	0	0	0	0	0	1	0	2(2π/56)
	0	0	0	0	0	1	1	3(2π/56)
	0	0	0	1	0	0	0	4(2π/56)
	0	0	0	1	0	0	1	5(2π/56)
	0	0	0	1	0	1	0	6(2π/56)
	0	0	0	1	0	1	1	7(2π/56)
	0	0	1	0	0	0	0	8(2π/56)
	0	0	1	0	0	0	1	9(2π/56)
	0	0	1	0	0	1	0	10(2π/56)
	0	0	1	0	0	1	1	11(2π/56)
	0	0	1	1	0	0	0	12(2π/56)
	0	0	1	1	0	0	1	13(2π/56)
	0	0	1	1	0	1	0	14(2π/56)
	0	0	1	1	0	1	1	15(2π/56)
	0	1	0	0	0	0	0	16(2π/56)
	0	1	0	0	0	0	1	17(2π/56)
	0	1	0	0	0	1	0	18(2π/56)
	0	1	0	0	0	1	1	19(2π/56)
	0	1	0	1	0	0	0	20(2π/56)
	0	1	0	1	0	0	1	21(2π/56)
	0	1	0	1	0	1	0	22(2π/56)
	0	1	0	1	0	1	1	23(2π/56)
	0	1	1	0	0	0	0	24(2π/56)
	0	1	1	0	0	0	1	25(2π/56)
	0	1	1	0	0	1	0	26(2π/56)
	0	1	1	0	0	1	1	27(2π/56)
	1	0	0	0	0	0	0	28(2π/56)
	1	0	0	0	0	0	1	29(2π/56)
	1	0	0	0	0	1	0	30(2π/56)
	1	0	0	0	0	1	1	31(2π/56)
	1	0	0	1	0	0	0	32(2π/56)
	1	0	0	1	0	0	1	33(2π/56)
	1	0	0	1	0	1	0	34(2π/56)
	1	0	0	1	0	1	1	35(2π/56)
	1	0	1	0	0	0	0	36(2π/56)
	1	0	1	0	0	0	1	37(2π/56)
	1	0	1	0	0	1	0	38(2π/56)
	1	0	1	0	0	1	1	39(2π/56)
	1	0	1	1	0	0	0	40(2π/56)
	1	0	1	1	0	0	1	41(2π/56)
	1	0	1	1	0	1	0	42(2π/56)
	1	0	1	1	0	1	1	43(2π/56)
	1	1	0	0	0	0	0	44(2π/56)
	1	1	0	0	0	0	1	45(2π/56)
	1	1	0	0	0	1	0	46(2π/56)
	1	1	0	0	0	1	1	47(2π/56)
	1	1	0	1	0	0	0	48(2π/56)
	1	1	0	1	0	0	1	49(2π/56)
	1	1	0	1	0	1	0	50(2π/56)
	1	1	0	1	0	1	1	51(2π/56)
	1	1	1	0	0	0	0	52(2π/56)
	1	1	1	0	0	0	1	53(2π/56)
	1	1	1	0	0	1	0	54(2π/56)
	1	1	1	0	0	1	1	55(2π/56)

Table 28. CDCE62005 Output Coarse Phase Adjust Settings (5)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
60	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/60)
	0	0	0	0	0	1	0	2(2π/60)
	0	0	0	0	0	1	1	3(2π/60)
	0	0	0	0	1	0	0	4(2π/60)
	0	0	0	1	0	0	0	5(2π/60)
	0	0	0	1	0	0	1	6(2π/60)
	0	0	0	1	0	1	0	7(2π/60)
	0	0	0	1	0	1	1	8(2π/60)
	0	0	0	1	1	0	0	9(2π/60)
	0	0	1	0	0	0	0	10(2π/60)
	0	0	1	0	0	0	1	11(2π/60)
	0	0	1	0	0	1	0	12(2π/60)
	0	0	1	0	0	1	1	13(2π/60)
	0	0	1	0	1	0	0	14(2π/60)
	0	0	1	1	0	0	0	15(2π/60)
	0	0	1	1	0	0	1	16(2π/60)
	0	0	1	1	0	1	0	17(2π/60)
	0	0	1	1	0	1	1	18(2π/60)
	0	0	1	1	1	0	0	19(2π/60)
	0	1	0	0	0	0	0	20(2π/60)
	0	1	0	0	0	0	1	21(2π/60)
	0	1	0	0	0	1	0	22(2π/60)
	0	1	0	0	0	1	1	23(2π/60)
	0	1	0	0	1	0	0	24(2π/60)
	0	1	0	1	0	0	0	25(2π/60)
	0	1	0	1	0	0	1	26(2π/60)
	0	1	0	1	0	1	0	27(2π/60)
	0	1	0	1	0	1	1	28(2π/60)
	0	1	0	1	1	0	0	29(2π/60)
	1	0	0	0	0	0	0	30(2π/60)
	1	0	0	0	0	0	1	31(2π/60)
	1	0	0	0	0	1	0	32(2π/60)
	1	0	0	0	0	1	1	33(2π/60)
	1	0	0	0	1	0	0	34(2π/60)
	1	0	0	1	0	0	0	35(2π/60)
	1	0	0	1	0	0	1	36(2π/60)
	1	0	0	1	0	1	0	37(2π/60)
	1	0	0	1	0	1	1	38(2π/60)
	1	0	0	1	1	0	0	39(2π/60)
	1	0	1	0	0	0	0	40(2π/60)
	1	0	1	0	0	0	1	41(2π/60)
	1	0	1	0	0	1	0	42(2π/60)
	1	0	1	0	0	1	1	43(2π/60)
	1	0	1	0	1	0	0	44(2π/60)
	1	0	1	1	0	0	0	45(2π/60)
	1	0	1	1	0	0	1	46(2π/60)
	1	0	1	1	0	1	0	47(2π/60)
	1	0	1	1	0	1	1	48(2π/60)
	1	0	1	1	1	0	0	49(2π/60)
	1	1	0	0	0	0	0	50(2π/60)
	1	1	0	0	0	0	1	51(2π/60)
	1	1	0	0	0	1	0	52(2π/60)
	1	1	0	0	0	1	1	53(2π/60)
	1	1	0	0	1	0	0	54(2π/60)
	1	1	0	1	0	0	0	55(2π/60)
	1	1	0	1	0	0	1	56(2π/60)
	1	1	0	1	0	1	0	57(2π/60)
	1	1	0	1	0	1	1	58(2π/60)
	1	1	0	1	1	0	0	59(2π/60)

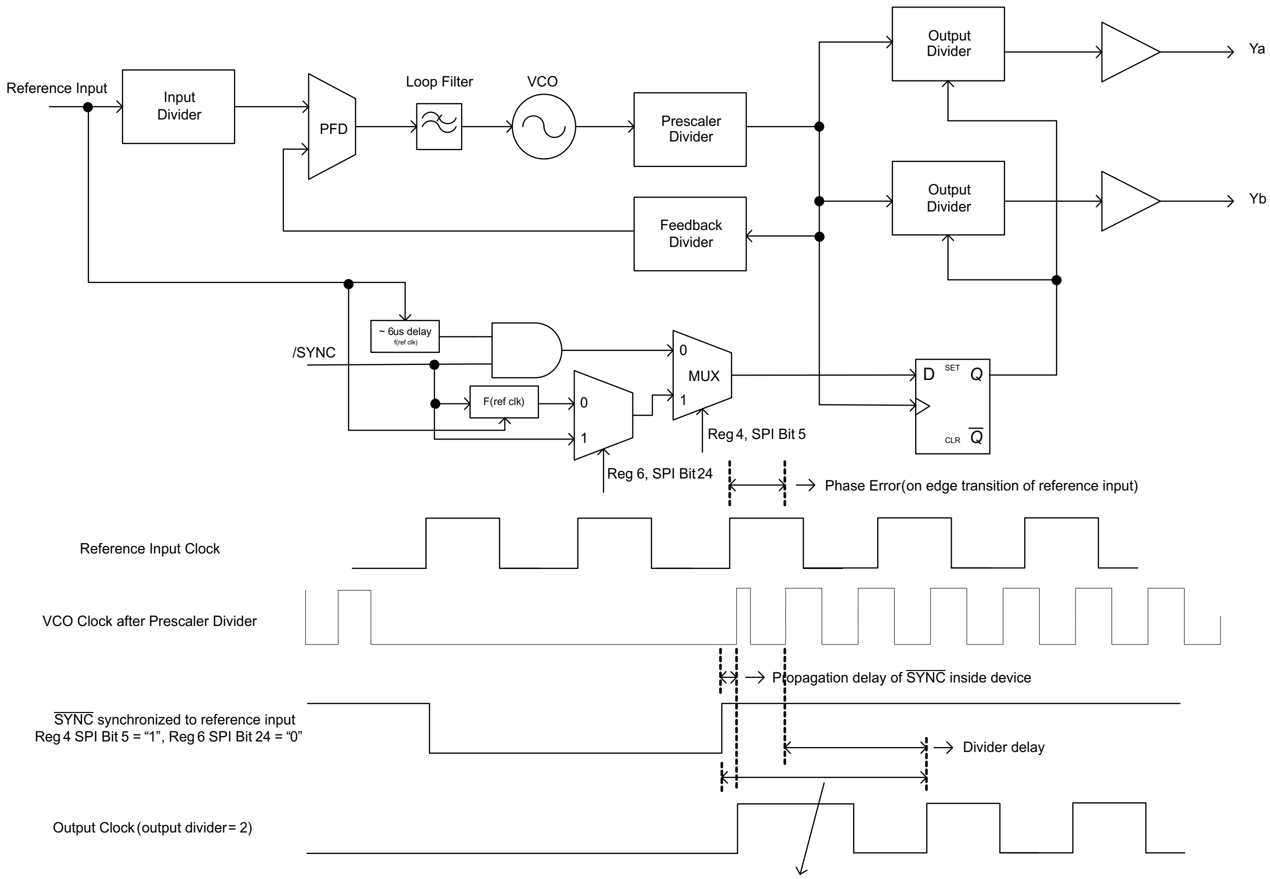
Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
64	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/64)
	0	0	0	0	0	1	0	2(2π/64)
	0	0	0	0	0	1	1	3(2π/64)
	0	0	0	1	0	0	0	4(2π/64)
	0	0	0	1	0	0	1	5(2π/64)
	0	0	0	1	0	1	0	6(2π/64)
	0	0	0	1	0	1	1	7(2π/64)
	0	0	1	0	0	0	0	8(2π/64)
	0	0	1	0	0	0	1	9(2π/64)
	0	0	1	0	0	1	0	10(2π/64)
	0	0	1	0	0	1	1	11(2π/64)
	0	0	1	1	0	0	0	12(2π/64)
	0	0	1	1	0	0	1	13(2π/64)
	0	0	1	1	0	1	0	14(2π/64)
	0	0	1	1	0	1	1	15(2π/64)
	0	1	0	0	0	0	0	16(2π/64)
	0	1	0	0	0	0	1	17(2π/64)
	0	1	0	0	0	1	0	18(2π/64)
	0	1	0	0	0	1	1	19(2π/64)
	0	1	0	1	0	0	0	20(2π/64)
	0	1	0	1	0	0	1	21(2π/64)
	0	1	0	1	0	1	0	22(2π/64)
	0	1	0	1	0	1	1	23(2π/64)
	0	1	1	0	0	0	0	24(2π/64)
	0	1	1	0	0	0	1	25(2π/64)
	0	1	1	0	0	1	0	26(2π/64)
	0	1	1	0	0	1	1	27(2π/64)
	0	1	1	1	0	0	0	28(2π/64)
	0	1	1	1	0	0	1	29(2π/64)
	0	1	1	1	0	1	0	30(2π/64)
	0	1	1	1	0	1	1	31(2π/64)
	1	0	0	0	0	0	0	32(2π/64)
	1	0	0	0	0	0	1	33(2π/64)
	1	0	0	0	0	1	0	34(2π/64)
	1	0	0	0	0	1	1	35(2π/64)
	1	0	0	1	0	0	0	36(2π/64)
	1	0	0	1	0	0	1	37(2π/64)
	1	0	0	1	0	1	0	38(2π/64)
	1	0	0	1	0	1	1	39(2π/64)
	1	0	1	0	0	0	0	40(2π/64)
	1	0	1	0	0	0	1	41(2π/64)
	1	0	1	0	0	1	0	42(2π/64)
	1	0	1	0	0	1	1	43(2π/64)
	1	0	1	1	0	0	0	44(2π/64)
	1	0	1	1	0	0	1	45(2π/64)
	1	0	1	1	0	1	0	46(2π/64)
	1	0	1	1	0	1	1	47(2π/64)
	1	1	0	0	0	0	0	48(2π/64)
	1	1	0	0	0	0	1	49(2π/64)
	1	1	0	0	0	1	0	50(2π/64)
	1	1	0	0	0	1	1	51(2π/64)
	1	1	0	1	0	0	0	52(2π/64)
	1	1	0	1	0	0	1	53(2π/64)
	1	1	0	1	0	1	0	54(2π/64)
	1	1	0	1	0	1	1	55(2π/64)
	1	1	1	0	0	0	0	56(2π/64)
	1	1	1	0	0	0	1	57(2π/64)
	1	1	1	0	0	1	0	58(2π/64)
	1	1	1	0	0	1	1	59(2π/64)
	1	1	1	1	0	0	0	60(2π/64)
	1	1	1	1	0	0	1	61(2π/64)
	1	1	1	1	0	1	0	62(2π/64)
	1	1	1	1	0	1	1	63(2π/64)

Table 29. CDCE62005 Output Coarse Phase Adjust Settings (6)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
70	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/70)
	0	0	0	0	0	1	0	2(2π/70)
	0	0	0	0	0	1	1	3(2π/70)
	0	0	0	0	1	0	0	4(2π/70)
	0	0	0	1	0	0	0	5(2π/70)
	0	0	0	1	0	0	1	6(2π/70)
	0	0	0	1	0	1	0	7(2π/70)
	0	0	0	1	0	1	1	8(2π/70)
	0	0	0	1	1	0	0	9(2π/70)
	0	0	1	0	0	0	0	10(2π/70)
	0	0	1	0	0	0	1	11(2π/70)
	0	0	1	0	0	1	0	12(2π/70)
	0	0	1	0	0	1	1	13(2π/70)
	0	0	1	0	1	0	0	14(2π/70)
	0	0	1	1	0	0	0	15(2π/70)
	0	0	1	1	0	0	1	16(2π/70)
	0	0	1	1	0	1	0	17(2π/70)
	0	0	1	1	0	1	1	18(2π/70)
	0	0	1	1	1	0	0	19(2π/70)
	0	1	0	0	0	0	0	20(2π/70)
	0	1	0	0	0	0	1	21(2π/70)
	0	1	0	0	0	1	0	22(2π/70)
	0	1	0	0	0	1	1	23(2π/70)
	0	1	0	0	1	0	0	24(2π/70)
	0	1	0	1	0	0	0	25(2π/70)
	0	1	0	1	0	0	1	26(2π/70)
	0	1	0	1	0	1	0	27(2π/70)
	0	1	0	1	0	1	1	28(2π/70)
	0	1	0	1	1	0	0	29(2π/70)
	0	1	1	0	0	0	0	30(2π/70)
	0	1	1	0	0	0	1	31(2π/70)
	0	1	1	0	0	1	0	32(2π/70)
	0	1	1	0	0	1	1	33(2π/70)
	0	1	1	0	1	0	0	34(2π/70)
	1	0	0	0	0	0	0	35(2π/70)
	1	0	0	0	0	0	1	36(2π/70)
	1	0	0	0	0	1	0	37(2π/70)
	1	0	0	0	0	1	1	38(2π/70)
	1	0	0	0	1	0	0	39(2π/70)
	1	0	0	1	0	0	0	40(2π/70)
	1	0	0	1	0	0	1	41(2π/70)
	1	0	0	1	0	1	0	42(2π/70)
	1	0	0	1	0	1	1	43(2π/70)
	1	0	0	1	1	0	0	44(2π/70)
	1	0	1	0	0	0	0	45(2π/70)
	1	0	1	0	0	0	1	46(2π/70)
	1	0	1	0	0	1	0	47(2π/70)
	1	0	1	0	0	1	1	48(2π/70)
	1	0	1	0	1	0	0	49(2π/70)
	1	0	1	1	0	0	0	50(2π/70)
	1	0	1	1	0	0	1	51(2π/70)
	1	0	1	1	0	1	0	52(2π/70)
	1	0	1	1	0	1	1	53(2π/70)
	1	0	1	1	1	0	0	54(2π/70)
	1	1	0	0	0	0	0	55(2π/70)
	1	1	0	0	0	0	1	56(2π/70)
	1	1	0	0	0	1	0	57(2π/70)
	1	1	0	0	0	1	1	58(2π/70)
	1	1	0	0	1	0	0	59(2π/70)
	1	1	0	1	0	0	0	60(2π/70)
	1	1	0	1	0	0	1	61(2π/70)
	1	1	0	1	0	1	0	62(2π/70)
	1	1	0	1	0	1	1	63(2π/70)
	1	1	0	1	1	0	0	64(2π/70)
	1	1	1	0	0	0	0	65(2π/70)
	1	1	1	0	0	0	1	66(2π/70)
	1	1	1	0	0	1	0	67(2π/70)
	1	1	1	0	0	1	1	68(2π/70)
	1	1	1	0	1	0	0	69(2π/70)

Divide Ratio	PHnADGC6 n.12	PHnADGC5 n.11	PHnADGC4 n.10	PHnADGC3 n.9	PHnADGC2 n.8	PHnADGC1 n.7	PHnADGC0 n.6	Phase Delay (radian)
80	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	(2π/80)
	0	0	0	0	0	1	0	2(2π/80)
	0	0	0	0	0	1	1	3(2π/80)
	0	0	0	0	1	0	0	4(2π/80)
	0	0	0	1	0	0	0	5(2π/80)
	0	0	0	1	0	0	1	6(2π/80)
	0	0	0	1	0	1	0	7(2π/80)
	0	0	0	1	0	1	1	8(2π/80)
	0	0	0	1	1	0	0	9(2π/80)
	0	0	1	0	0	0	0	10(2π/80)
	0	0	1	0	0	0	1	11(2π/80)
	0	0	1	0	0	1	0	12(2π/80)
	0	0	1	0	0	1	1	13(2π/80)
	0	0	1	0	1	0	0	14(2π/80)
	0	0	1	1	0	0	0	15(2π/80)
	0	0	1	1	0	0	1	16(2π/80)
	0	0	1	1	0	1	0	17(2π/80)
	0	0	1	1	0	1	1	18(2π/80)
	0	0	1	1	1	0	0	19(2π/80)
	0	1	0	0	0	0	0	20(2π/80)
	0	1	0	0	0	0	1	21(2π/80)
	0	1	0	0	0	1	0	22(2π/80)
	0	1	0	0	0	1	1	23(2π/80)
	0	1	0	0	1	0	0	24(2π/80)
	0	1	0	1	0	0	0	25(2π/80)
	0	1	0	1	0	0	1	26(2π/80)
	0	1	0	1	0	1	0	27(2π/80)
	0	1	0	1	0	1	1	28(2π/80)
	0	1	0	1	1	0	0	29(2π/80)
	0	1	1	0	0	0	0	30(2π/80)
	0	1	1	0	0	0	1	31(2π/80)
	0	1	1	0	0	1	0	32(2π/80)
	0	1	1	0	0	1	1	33(2π/80)
	0	1	1	0	1	0	0	34(2π/80)
	0	1	1	1	0	0	0	35(2π/80)
	0	1	1	1	0	0	1	36(2π/80)
	0	1	1	1	0	1	0	37(2π/80)
	0	1	1	1	0	1	1	38(2π/80)
	0	1	1	1	1	0	0	39(2π/80)
	1	0	0	0	0	0	0	40(2π/80)
	1	0	0	0	0	0	1	41(2π/80)
	1	0	0	0	0	1	0	42(2π/80)
	1	0	0	0	0	1	1	43(2π/80)
	1	0	0	0	1	0	0	44(2π/80)
	1	0	0	1	0	0	0	45(2π/80)
	1	0	0	1	0	0	1	46(2π/80)
	1	0	0	1	0	1	0	47(2π/80)
	1	0	0	1	0	1	1	48(2π/80)
	1	0	0	1	1	0	0	49(2π/80)
	1	0	1	0	0	0	0	50(2π/80)
	1	0	1	0	0	0	1	51(2π/80)
	1	0	1	0	0	1	0	52(2π/80)
	1	0	1	0	0	1	1	53(2π/80)
	1	0	1	0	1	0	0	54(2π/80)
	1	0	1	1	0	0	0	55(2π/80)
	1	0	1	1	0	0	1	56(2π/80)
	1	0	1	1	0	1	0	57(2π/80)
	1	0	1	1	0	1	1	58(2π/80)
	1	0	1	1	1	0	0	59(2π/80)
	1	1	0	0	0	0	0	60(2π/80)
	1	1	0	0	0	0	1	61(2π/80)
	1	1	0	0	0	1	0	62(2π/80)
	1	1	0	0	0	1	1	63(2π/80)
	1	1	0	0	1	0	0	64(2π/80)
	1	1	0	1	0	0	0	65(2π/80)
	1	1	0	1	0	0	1	66(2π/80)
	1	1	0	1	0	1	0	67(2π/80)
	1	1	0	1	0	1	1	68(2π/80)
	1	1	0	1	1	0	0	69(2π/80)
	1	1	1	0	0	0	0	70(2π/80)
	1	1	1	0	0	0	1	71(2π/80)
	1	1	1	0	0	1	0	72(2π/80)
	1	1	1	0	0	1	1	73(2π/80)
	1	1	1	0	1	0	0	74(2π/80)
	1	1	1	1	0	0	0	75(2π/80)
	1	1	1	1	0	0	1	76(2π/80)
	1	1	1	1	0	1	0	77(2π/80)
	1	1	1	1	0	1	1	78(2π/80)
	1	1	1	1	1	0	0	79(2π/80)

Output Synchronization



When Reg 6, SPI Bit 24 = "0", Reg 4 SPI Bit 5 = "1" and the $\overline{\text{SYNC}}$ pulse low-to-high transition is synchronized to the reference input, the delay of the $\overline{\text{SYNC}}$ low-to-high pulse to the toggling of synchronized outputs is equal to the propagation delay of $\overline{\text{SYNC}}$ signal inside device + phase error (on reference input edge transition after $\overline{\text{SYNC}}$ signal) + divider delay (2.5 clock cycles of VCO clock after prescaler) + delay between $\overline{\text{SYNC}}$ and input transition. Total uncertainty is 1 clock cycle of VCO clock after prescaler (uncertainty irrespective of output divide value)

Figure 32. CDCE62005 $\overline{\text{SYNC}}$ to Output delay variation

Output Synchronization Timing

Synchronization of the outputs is edecuted in several ways:

- The $\overline{\text{SYNC}}$ pin is forced low and then released (manual sync).
- By setting and then resetting Register 8, SPI Bit 12.
- Whenever the output dividers are changed.

The most common way to execute the output synchronization is to toggle the $\overline{\text{SYNC}}$ pin where the outputs are aligned on a low-to-high pulse on the SYNC after a delay as explained in Figure 32. For having tight control on the delay variation of the outputs synchronization after a low-to-high pulse on the SYNC pin, the Register 4, SPI Bit 5 needs to be set to "1". When Reg 6, SPI Bit 24 = "0", the outputs are synchronized to each other and to the reference input. In this case, the total delay from SYNC low-to-high pulse to toggling of synchronized outputs is given in Figure 32.

When Reg 6, SPI Bit 24 = "1", the outputs are synchronized to each other and to the $\overline{\text{SYNC}}$ low-to-high pulse. In this case, the total delay from SYNC low-to-high pulse to toggling of synchronized outputs is equal to the propagation delay of SYNC signal inside device + divider delay. Total uncertainty is 1 cycle of VCO clock after prescaler (uncertainty irrespective of output divide value).

Auxiliary Output

Figure 33 shows the auxiliary output port. Table 30 lists how the auxiliary output port is controlled. The output buffer supports a maximum output frequency of 250 MHz and drives at LVCMOS levels. Refer to for the list of divider settings that establishes the output frequency.

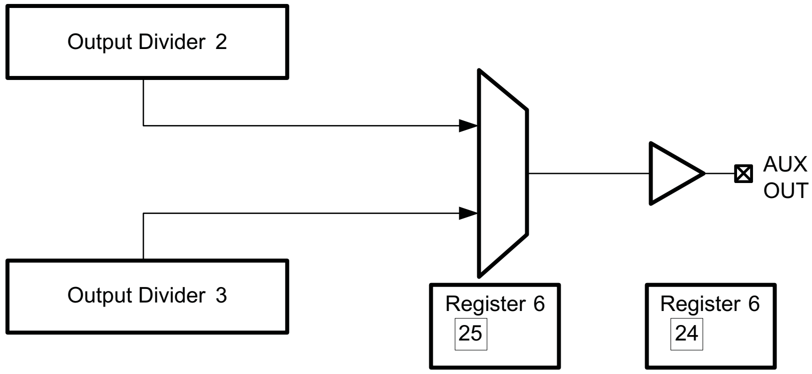


Figure 33. CDCE62005 Auxiliary Output

Table 30. CDCE62005 Auxiliary Output Settings

Bit Name →	AUXFEEDSEL	AUXOUTEN	AUX OUTPUT SOURCE
Register.Bit →	6.25	6.24	
	X	0	OFF
	0	1	Divider 2
	1	1	Divider 3

SYNTHESIZER BLOCK

Figure 34 provides an overview of the CDCE62005 synthesizer block. The Synthesizer Block provides a Phase Locked Loop, a partially integrated programmable loop filter, and two Voltage Controlled Oscillators (VCO). The synthesizer block generates an output clock called "SYNTH" and drives it onto the Internal Clock Distribution Bus.

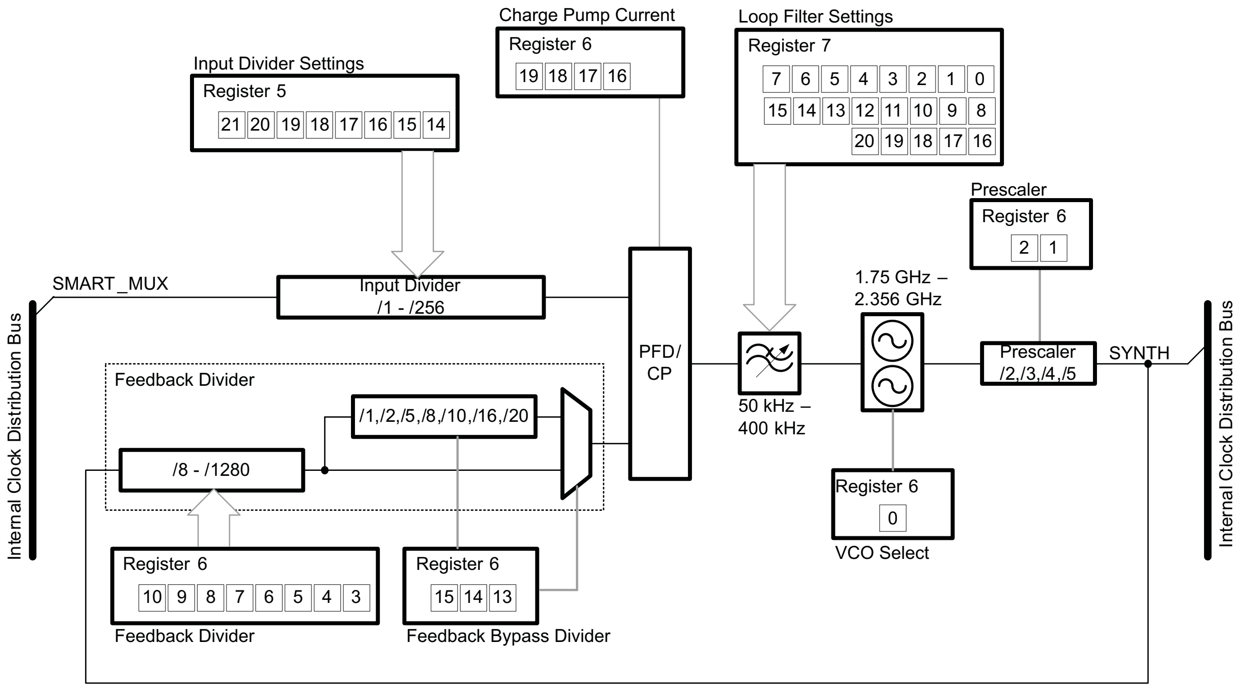


Figure 34. CDCE62005 Synthesizer Block

Input Divider

The Input Divider divides the clock signal selected by the Smart Multiplexer (see Table 18) and presents the divided signal to the Phase Frequency Detector / Charge Pump of the frequency synthesizer.

Table 31. CDCE62005 Input Divider Settings

INPUT DIVIDER SETTINGS								DIVIDE RATIO
SELINDIV7	SELINDIV6	SELINDIV5	SELINDIV4	SELINDIV3	SELINDIV2	SELINDIV1	SELINDIV0	
5.21	5.20	5.19	5.18	5.17	5.16	5.15	5.14	
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
0	0	0	0	0	1	0	1	6
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	256

Feedback and Feedback Bypass Divider

Table 32 shows how to configure the Feedback divider for various divide values

Table 32. CDCE62005 Feedback Divider Settings

FEEDBACK DIVIDER								DIVIDE RATIO
SELFBDIV7	SELFBDIV6	SELFBDIV5	SELFBDIV4	SELFBDIV3	SELFBDIV2	SELFBDIV1	SELFBDIV0	
6.10	6.9	9.8	6.7	6.6	6.5	6.4	6.3	
0	0	0	0	0	0	0	0	8
0	0	0	0	0	0	0	1	12
0	0	0	0	0	0	1	0	16
0	0	0	0	0	0	1	1	20
0	0	0	0	0	1	0	1	24
0	0	0	0	0	1	1	0	32
0	0	0	0	1	0	0	1	36
0	0	0	0	0	1	1	1	40
0	0	0	0	1	0	1	0	48
0	0	0	1	1	0	0	0	56
0	0	0	0	1	0	1	1	60
0	0	0	0	1	1	1	0	64
0	0	0	1	0	1	0	1	72
0	0	0	0	1	1	1	1	80
0	0	0	1	1	0	0	1	84
0	0	0	1	0	1	1	0	96
0	0	0	1	0	0	1	1	100
0	1	0	0	1	0	0	1	108
0	0	0	1	1	0	1	0	112
0	0	0	1	0	1	1	1	120
0	0	0	1	1	1	1	0	128
0	0	0	1	1	0	1	1	140
0	0	1	1	0	1	0	1	144
0	0	0	1	1	1	1	1	160
0	0	1	1	1	0	0	1	168
0	1	0	0	1	0	1	1	180
0	0	1	1	0	1	1	0	192
0	0	1	1	0	0	1	1	200
0	1	0	1	0	1	0	1	216
0	0	1	1	1	0	1	0	224
0	0	1	1	0	1	1	1	240
0	1	0	1	1	0	0	1	252
0	0	1	1	1	1	1	0	256
0	0	1	1	1	0	1	1	280
0	1	0	1	0	1	1	0	288
0	1	0	1	0	0	1	1	300
0	0	1	1	1	1	1	1	320
0	1	0	1	1	0	1	0	336
0	1	0	1	0	1	1	1	360
0	1	0	1	1	1	1	0	384
1	1	0	1	1	0	0	0	392
0	1	1	1	0	0	1	1	400

Table 32. CDCE62005 Feedback Divider Settings (continued)

FEEDBACK DIVIDER								DIVIDE RATIO
SELFBDIV7	SELFBDIV6	SELFBDIV5	SELFBDIV4	SELFBDIV3	SELFBDIV2	SELFBDIV1	SELFBDIV0	
6.10	6.9	9.8	6.7	6.6	6.5	6.4	6.3	
0	1	0	1	1	0	1	1	420
1	0	1	1	0	1	0	1	432
0	1	1	1	1	0	1	0	448
0	1	0	1	1	1	1	1	480
1	0	0	1	0	0	1	1	500
1	0	1	1	1	0	0	1	504
0	1	1	1	1	1	1	0	512
0	1	1	1	1	0	1	1	560
1	0	1	1	0	1	1	0	576
1	1	0	1	1	0	0	1	588
1	0	0	1	0	1	1	1	600
0	1	1	1	1	1	1	1	640
1	0	1	1	1	0	1	0	672
1	0	0	1	1	0	1	1	700
1	0	1	1	0	1	1	1	720
1	0	1	1	1	1	1	0	768
1	1	0	1	1	0	1	0	784
1	0	0	1	1	1	1	1	800
1	0	1	1	1	0	1	1	840
1	1	0	1	1	1	1	0	896
1	0	1	1	1	1	1	1	960
1	1	0	1	1	0	1	1	980
1	1	1	1	1	1	1	0	1024
1	1	0	1	1	1	1	1	1120
1	1	1	1	1	1	1	1	1280

Table 33 shows how to configure the Feedback Bypass Divider.

Table 33. CDCE62005 Feedback Bypass Divider Settings

FEEDBACK BYPASS DIVIDER			DIVIDE RATIO
SELBPDIV2	SELBPDIV1	SELBPDIV0	
6.15	6.14	6.13	
0	0	0	2
0	0	1	5
0	1	0	8
0	1	1	10
1	0	0	16
1	0	1	20
1	1	0	RESERVED
1	1	1	1(bypass)

VCO Select

Table 34 illustrates how to control the dual voltage controlled oscillators.

Table 34. CDCE62005 VCO Select

Bit Name →	VCO Select SELVCO	VCO CHARACTERISTICS		
Register.Bit →	6.0	VCO Range	Fmin (MHz)	Fmax (MHz)
	0	Low	1750	2046
	1	High	2040	2356

Prescaler

Table 35 shows how to configure the prescaler.

Table 35. CDCE62005 Prescaler Settings

SETTINGS		DIVIDE RATIO
SELPRESCB	SELPRESCA	
6.2	6.1	
0	0	5
1	0	4
0	1	3
1	1	2

Charge Pump Current Settings

Table 36 provides the settings for the charge pump:

Table 36. CDCD62005 Charge Pump Settings

Bit Name →	CHARGE PUMP SETTINGS				CHARGE PUMP CURRENT
	ICPSEL3	ICPSEL2	ICPSEL1	ICPSEL0	
Register.Bit →	6.19	6.18	6.17	6.16	
	0	0	0	0	50 μA
	0	0	0	1	100 μA
	0	0	1	0	150 μA
	0	0	1	1	200 μA
	0	1	0	0	300 μA
	0	1	0	1	400 μA
	0	1	1	0	600 μA
	0	1	1	1	750 μA
	1	0	0	0	1 mA
	1	0	0	1	1.25 mA
	1	0	1	0	1.5 mA
	1	0	1	1	2 mA
	1	1	0	0	2.5 mA
	1	1	0	1	3 mA
	1	1	1	0	3.5 mA
	1	1	1	1	3.75 mA

Loop Filter

Figure 35 depicts the loop filter topology of the CDCE62005. It facilitates both internal and external implementations providing optimal flexibility.

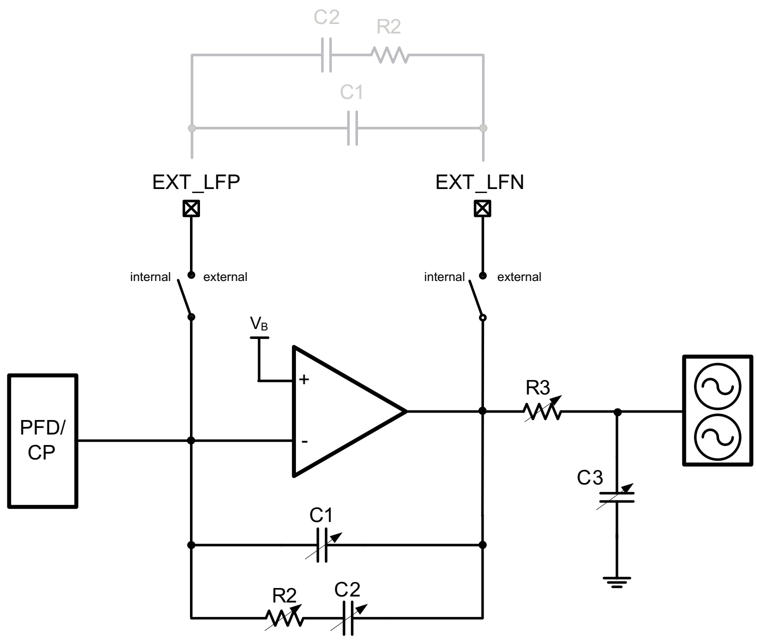


Figure 35. CDCE62005 Loop Filter Topology

Internal Loop Filter Component Configuration

Figure 35 contains five different loop filter components with programmable values: C1, C2, R2, R3, and C3. Table 37 shows that the CDCE62005 uses one of four different types of circuit implementation (shown in Figure 36) for each of the internal loop filter components.

Table 37. CDCE62005 Loop Filter Component Implementation Type

Component	Control Bits Used	Implementation Type (see Figure 36)
C1	5	a
C2	5	a
R2	5	c
R3	2	d
C3	4	b

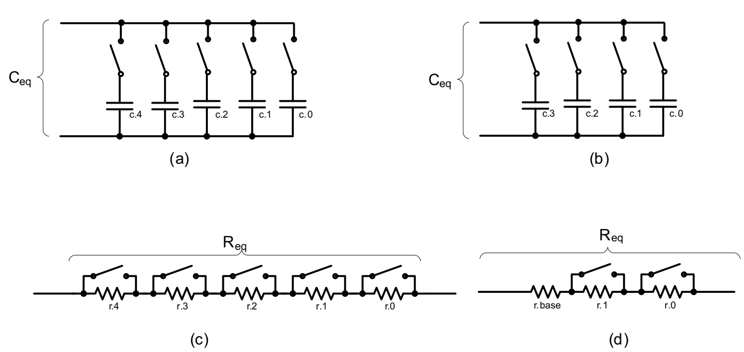


Figure 36. CDCE62005 Internal Loop Filter Component Schematics

Table 38. CDCE62005 Internal Loop Filter – C1 Settings

	C1 SETTINGS						
Bit Name →	**EXLFSEL**	**LFRCSEL14**	**LFRCSEL13**	**LFRCSEL12**	**LFRCSEL11**	**LFRCSEL10**	
Capacitor Value →	**—**	**37.5 pF**	**21.5 pF**	**10 pF**	**6.5 pF**	**1.5 pF**	
Register.Bit →	**6.26**	**7.14**	**7.13**	**7.12**	**7.11**	**7.10**	**Capacitor Value**
	1	X	X	X	X	X	External Loop Filter
	0	0	0	0	0	0	0 pF
	0	0	0	0	0	1	1.5 pF
	0	0	0	0	1	0	6.5 pF
	0	0	0	0	1	1	8 pF
	0	0	0	1	0	0	10 pF
	0	0	0	1	0	1	11.5 pF
	0	0	0	1	1	0	16.5 pF
	0	0	0	1	1	1	18 pF
	0	0	1	0	0	0	21.5 pF
	0	0	1	0	0	1	23 pF
	0	•	•	•	•	•	•
	0	1	1	1	0	0	69 pF
	0	1	1	1	0	1	70.5 pF
	0	1	1	1	1	0	75.5 pF
	0	1	1	1	1	1	77 pF

Table 39. CDCE62005 Internal Loop Filter – C2 Settings

	C2 SETTINGS						
Bit Name →1	**EXLFSEL**	**LFRCSEL4**	**LFRCSEL3**	**LFRCSEL2**	**LFRCSEL1**	**LFRCSEL0**	
Capacitor Value →	**—**	**226 pF**	**123 pF**	**87 pF**	**25 pF**	**12.5 pF**	
Register.Bit 1→	**6.26**	**7.4**	**7.3**	**7.2**	**7.1**	**7.0**	**Capacitor Value**
	1	0	0	0	0	0	External Loop Filter
	0	0	0	0	0	0	0 pF
	0	0	0	0	0	1	12.5 pF
	0	0	0	0	1	0	25 pF
	0	0	0	0	1	1	37.5 pF
	0	0	0	1	0	0	87 pF
	0	0	0	1	0	1	99.5 pF
	0	0	0	1	1	0	112 pF
	0	0	0	1	1	1	124.5 pF
	0	0	1	0	0	0	123 pF
	0	0	1	0	0	1	135.5 pF
	0	•	•	•	•	•	•
	0	1	1	1	0	0	436 pF
	0	1	1	1	0	1	448.5 pF
	0	1	1	1	1	0	461 pF
	0	1	1	1	1	1	473.5 pF

Table 40. CDCE62005 Internal Loop Filter – R2 Settings

	R2 SETTINGS						
Bit Name →	EXLFSEL	LFRCSEL9	LFRCSEL8	LFRCSEL7	LFRCSEL6	LFRCSEL5	
Resistor Value →	—	56.4 k	38.2 k	20 k	9 k	4 k	
Register.Bit →	6.26	7.9	7.8	7.7	7.6	7.5	Resistor Value (kΩ)
	1	X	X	X	X	X	External Loop Filter
	0	0	0	0	0	0	127.6
	0	0	0	0	0	1	123.6
	0	0	0	0	1	0	118.6
	0	0	0	0	1	1	114.6
	0	0	0	1	0	0	107.6
	0	0	0	1	0	1	103.6
	0	0	0	1	1	0	98.6
	0	0	0	1	1	1	94.6
	0	0	1	0	0	0	89.4
	0	0	1	0	0	1	85.4
	0	•	•	•	•	•	•
	0	1	1	1	0	0	13
	0	1	1	1	0	1	9
	0	1	1	1	1	0	4
	0	1	1	1	1	1	0

Table 41. CDCE62005 Internal Loop Filter – C3 Settings

	C3 SETTINGS					
Bit Name →	EXLFSEL	LFRCSEL18	LFRCSEL17	LFRCSEL16	LFRCSEL15	
Capacitor Value →	—	85 pF	19.5 pF	5.5 pF	2.5 pF	
Register.Bit →	6.26	7.18	7.17	7.16	7.15	Capacitor Value
	1	X	X	X	X	External Loop Filter
	0	0	0	0	0	0 pF
	0	0	0	0	1	2.5 pF
	0	0	0	1	0	5.5 pF
	0	0	0	1	1	8 pF
	0	0	1	0	0	19.5 pF
	0	0	1	0	1	22 pF
	0	0	1	1	0	25 pF
	0	0	1	1	1	27.5 pF
	0	1	0	0	0	85 pF
	0	1	0	0	1	87.5 pF
	0	•	•	•	•	•
	0	1	1	1	0	104.5 pF
	0	1	1	1	1	107 pF
	0	1	1	1	0	110 pF
	0	1	1	1	1	112.5 pF

Table 42. CDCE62005 Internal Loop Filter – R3 Settings

	R3 SETTINGS			
Bit Name →	**EXLFSEL**	**LFRCSEL20**	**LFRCSEL19**	
Resistor Value →	**—**	**10 k**	**5 k**	
Register.Bit →	**6.26**	**7.20**	**7.19**	**Resistor Value (kΩ)**
	1	X	X	External Loop Filter
	0	0	0	20
	0	0	1	15
	0	1	0	10
	0	1	1	5

External Loop Filter Component Configuration

To implement an external loop filter, set EXLFSEL bit (6.26) high. Setting all of the control switches low that control capacitors C1 and C2 (see Table 40) remove them from the loop filter circuit. This is necessary for an external loop filter implementation.

Lock Detect

Digital Lock Detect

The CDCE62005 provides both an analog and a digital lock detect circuit. With respect to lock detect, two signals whose phase difference is less than a prescribed amount are 'locked' otherwise they are 'unlocked'. The phase frequency detector / charge pump compares the clock provided by the input divider and the feedback divider; using the input divider as the phase reference. The digital lock detect circuit implements a programmable lock detect window. Table 43 shows an overview of how to configure the digital lock detect feature. When selecting the digital PLL lock option, the PLL_LOCK pin will possibly jitter several times between lock and out of lock until the PLL achieves a stable lock. If desired, choosing a wide loop bandwidth and a high number of successive clock cycles virtually eliminates this characteristic. PLL_LOCK will return to out of lock, if just one cycle is outside the lock detect window or if a cycle slip occurs.

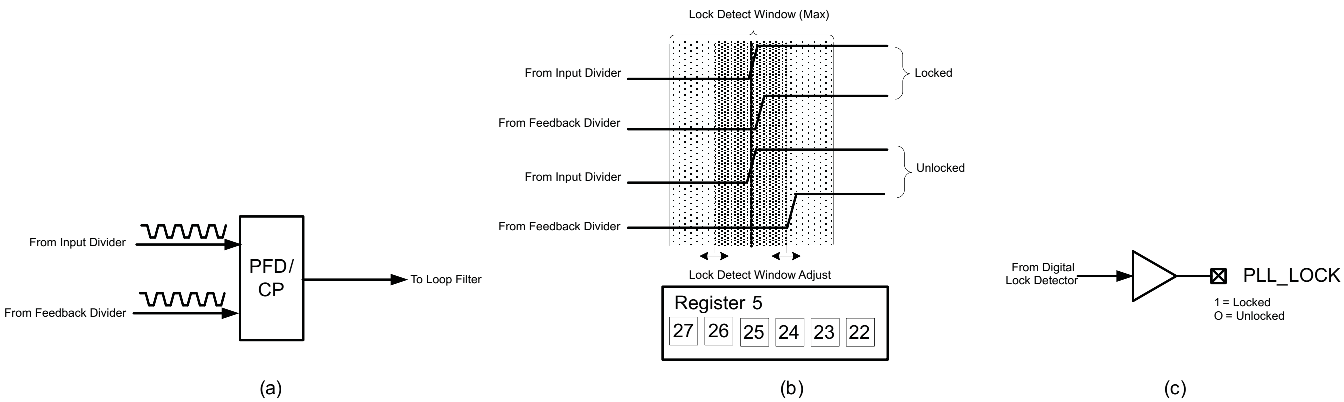


Figure 37. CDCE62005 Digital Lock Detect

Table 43. CDCE62005 Digital Lock Detect Control

	DIGITAL LOCK DETECT						
Bit Name →	ADLOCK	LOCKDET	LOCKW(3)	LOCKW(2)	LOCKW(1)	LOCKW(0)	
Register.Bit →	5.27	5.26	5.25	5.24	5.23	5.22	Lock Detect Window
	1	X	X	X	X	X	Analog Lock
	X	0	X	X	X	X	1 cycle in lock window triggers a lock
	X	1	X	X	X	X	64 continuous cycles in lock window triggers a lock
	0	X	0	0	0	0	Narrow Window
	0	X	0	0	0	1	One step wider than narrow window
	0	X	0	0	1	0	Two steps wider than narrow window
	0	X	0	1	0	0	Three steps wider than narrow window
	0	X	0	1	0	1	Four steps wider than narrow window
	•	•	•	•	•	•	•
	0	X	1	1	1	0	Widest Window
	0	X	X	X	1	1	Reserved

Analog Lock Detect

Figure 38 shows the Analog Lock Detect circuit. Depending upon the phase relationship of the two signals presented at the PFD/CP inputs, the lock detect circuit either charges (if the PLL is locked) or discharges (if PLL is unlocked) the circuit shown via 100μA current sources. An external capacitor determines the sensitivity of the lock detect circuit. The value of the capacitor determines the rate of change of the voltage presented on the output pin PLL_LOCK and hence how quickly the PLL_LOCK output toggles based on a change of PLL locked status. The PLL_LOCK pin is an analog output in analog lock detect mode.

$$Vout = \frac{1}{C} \times i \times t \tag{7}$$

Solving for t yields:

$$t = \frac{V_{out} \times C}{i} \tag{8}$$

$V_H = 0.55 \times V_{CC}$

$V_L = 0.35 \times V_{CC}$

For Example, let:

$$C = 10\ nF$$
$$V_{cc} = 3.3\ V \therefore V_H \cong 1.8\ V = V_{Out}$$
$$t = \frac{1.8 \times 10n}{110\ \mu} \cong 164\ \mu s \tag{9}$$

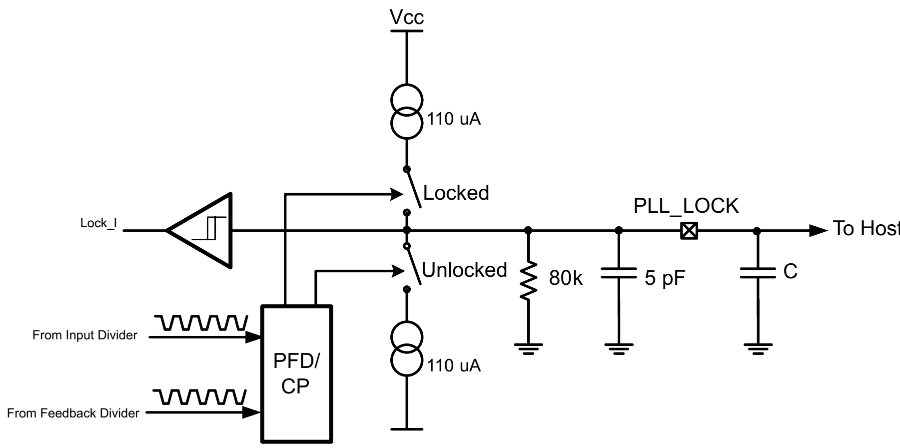


Figure 38. CDCE62005 Analog Lock Detect

DEVICE POWER CALCULATION AND THERMAL MANAGEMENT

The CDCE62005 is a high performance device, therefore careful attention must be paid to device configuration and printed circuit board layout with respect to power consumption. Table 44 provides the power consumption for the individual blocks within the CDCE62005. To estimate total power consumption, calculate the sum of the products of the number of blocks used and the power dissipated of each corresponding block.

Table 44. CDCE62005 Power Consumption

Internal Block (Power at 3.3V)	Power Dissipated per Block	Number of Blocks per Device
Input Circuit	250 mW	1
PLL and VCO Core	500 mW	1
Output Divider	185 mW	5
Output Buffer (LVPECL)	116 mW	5
Output Buffer (LVDS)	76 mW	5
Output Buffer (LVCMOS)	86 mW	10

This power estimate determines the degree of thermal management required for a specific design. Employing the thermally enhanced printed circuit board layout shown in Figure 40 insures that the thermal performance curves shown in Figure 39 apply. Observing good thermal layout practices enables the thermal pad on the backside of the QFN-48 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

Figure 40 shows a layout optimized for good thermal performance and a good power supply connection as well. The 7×7 filled via patter facilitates both considerations. Finally, the recommended layout achieves θ_{JA} = 27.3°C/W in still air and 20.3°C/W in an environment with 100 LFM airflow if implemented on a JEDEC compliant thermal test board..

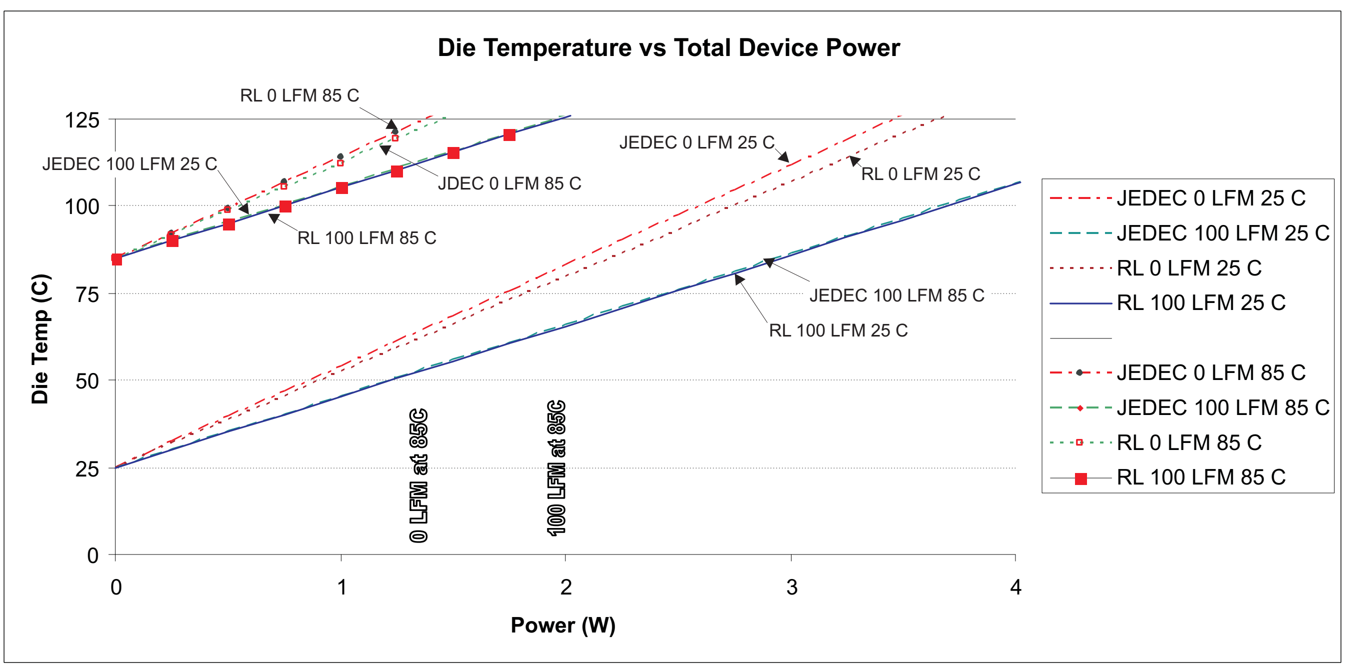


Figure 39. CDCE62005 Die Temperature vs Device Power

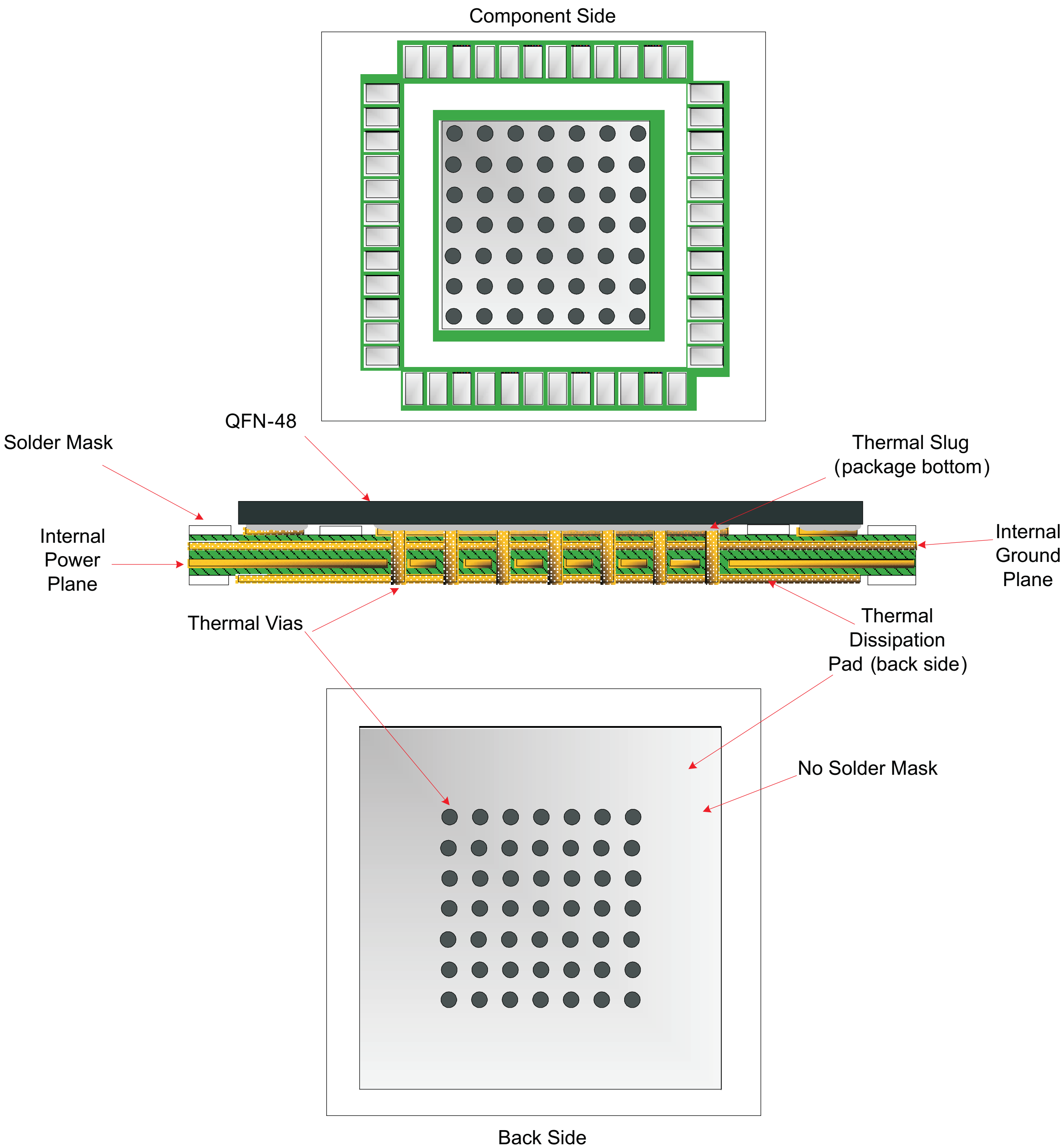
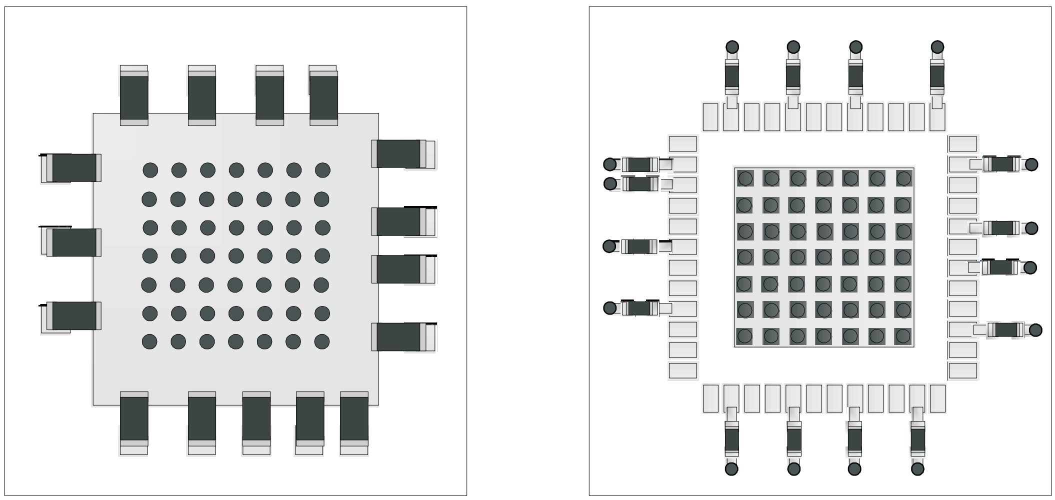


Figure 40. CDCE62005 Recommended PCB Layout

CDCE62005 Power Supply Bypassing – Recommended Layout

Figure 41 shows two conceptual layouts detailing recommended placement of power supply bypass capacitors. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. For component side mounting, use 0201 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.



Back Side

Component Side

Figure 41. CDCE62005 Power Supply Bypassing

APPLICATION INFORMATION AND GENERAL USAGE HINTS

Fan-out Buffer

Each output of the CDCE62005 can be configured as a fan-out buffer (divider bypassed) or fan-out buffer with divide and skew control functionality.

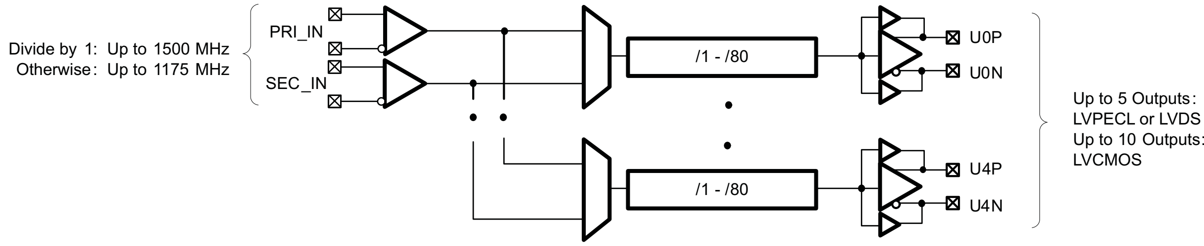


Figure 42. CDCE62005 Fan-out Buffer Mode

Clock Generator

The CDCE62005 can generate 5–10 low noise clocks from a single crystal as follows:

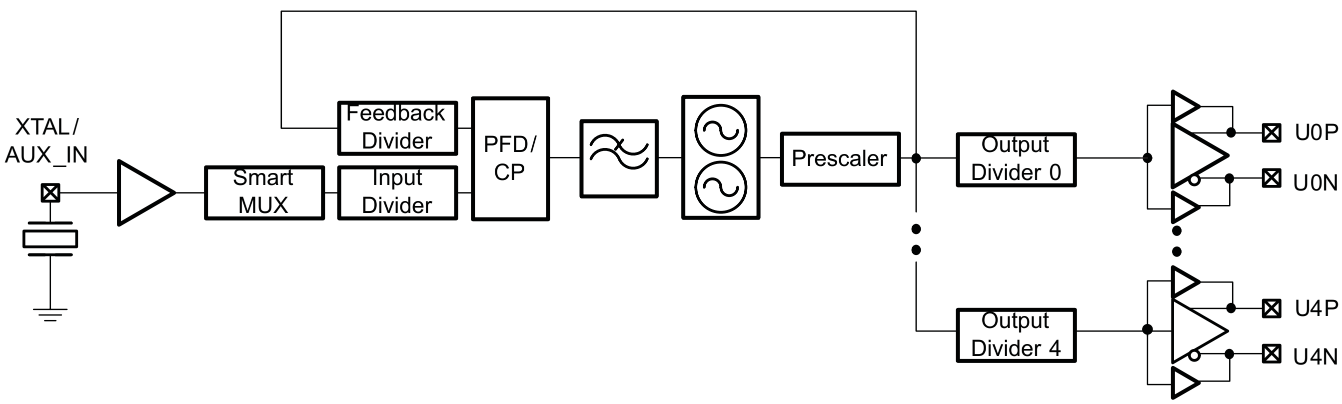


Figure 43. CDCE62005 Clock Generator Mode

Jitter Cleaner – Mixed Mode (1)

The following table presents a common scenario. The CDCE62005 must generate several integer-related clocks from a reference that has traversed a backplane. In order for jitter cleaning to take place, the phase noise of the on-board clock path must be better than that of the incoming clock. The designer must pay attention to the optimization of the loop bandwidth of the synthesizer and understand the phase noise profiles of the oscillators involved. Further, other devices on the card require clocks at frequencies not related to the backplane clock. The system requires combinations of differential and single-ended clocks in specific formats with specific phase relationships. (1)

CLOCK FREQUENCY	INPUT/OUTPUT	FORMAT	NUMBER	CDCE62005 PORT	COMMENT
10.000 MHz	Input	LVDS	1	SEC_IN	Low end crystal oscillator
30.72 MHz	Input	LVDS	1	PRI_IN	Reference from backplane
122.88 MHz	Output	LVDS	1	U0	SERDES Clock
491.52 MHz	Output	LVPECL	1	U1	ASIC
245.76 MHz	Output	LVPECL	1	U2	FPGA
30.72 MHz	Outputs	LVCMOS	2	U3	ASIC
10.000 MHz	Outputs	LVCMOS	2	U4	CPU, DSP

(1) Pay special attention when using the universal inputs with two different clock sources. Two clocks derived from the same source may use the internal bias generator and internal termination network without jitter performance degradation. However, if their origin is from different sources (e.g. two independent oscillators) then sharing the internal bias generator can degrade jitter performance significantly.

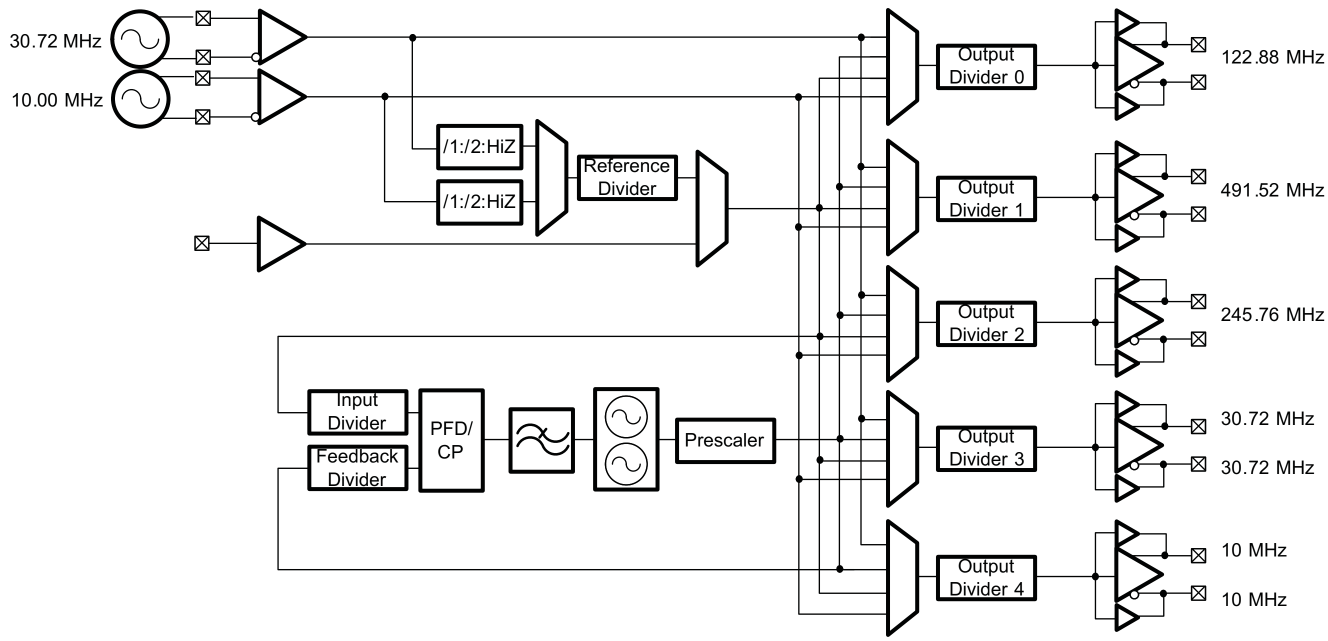


Figure 44. CDCE62005 Jitter Cleaner Example

Clocking ADCs with the CDCE62005

High-speed analog to digital converters incorporate high input bandwidth on both the analog port and the sample clock port. Often the input bandwidth far exceeds the sample rate of the converter. Engineers regularly implement receiver chains that take advantage of the characteristics of bandpass sampling. This implementation trend often causes engineers working in communications system design to encounter the term *clock limited performance*. Therefore, it is important to understand the impact of clock jitter on ADC performance. Equation 10 shows the relationship of data converter signal to noise ratio (SNR) to total jitter.

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{in}\, jitter_{total}}\right] \tag{10}$$

Total jitter comprises two components: the intrinsic aperture jitter of the converter and the jitter of the sample clock:

$$jitter_{total} = \sqrt{(jitter_{ADC})^2 + (jitter_{CLK})^2} \tag{11}$$

With respect to an ADC with N-bits of resolution, ignoring total jitter, DNL, and input noise, the following equation shows the relationship between resolution and SNR:

$$SNR_{ADC} = 6.02N + 1.76 \tag{12}$$

Figure 45 plots Equation 10 and Equation 12 for constant values of total jitter. When used in conjunction with most ADCs, the CDCE62005 supports a total jitter performance value of <1 ps.

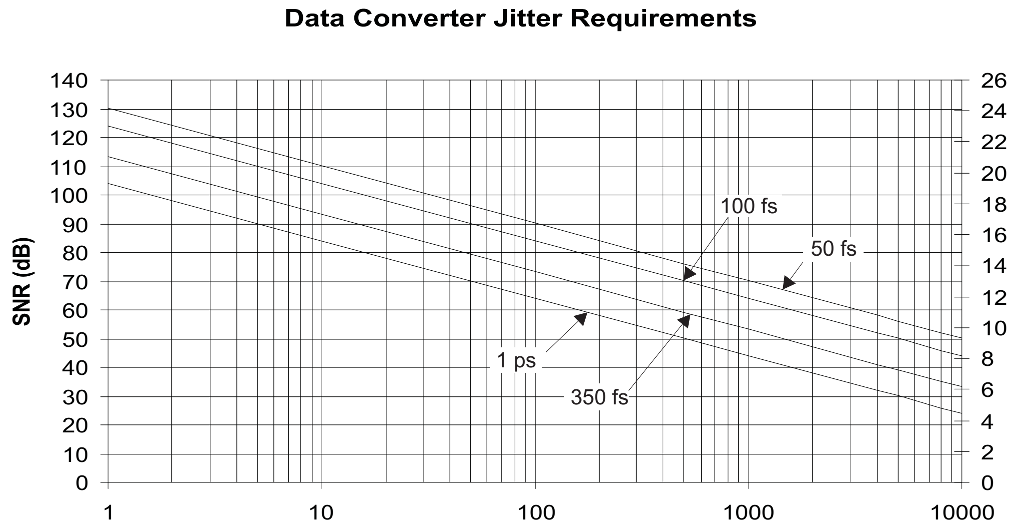


Figure 45. Data Converter Jitter Requirements

CDCE62005 SERDES Startup Mode

A common scenario involves a host communicating to a satellite system via a high-speed wired communications link. Typical communications media might be a cable, backplane, or fiber. The reference clock for the satellite system is embedded in the high speed link. This reference clock must be recovered by the SERDES, however, the recovered clock contains unacceptable levels of jitter due to a degradation of SNR associated with transmission over the media. At system startup, the satellite system must self-configure prior to the recovery and cleanup of the reference clock provided by the host. Furthermore, upon loss of the communication link with the host, the satellite system must continue to operate albeit with limited functionality. Figure 46 shows a block diagram of an optical based system with such a mechanism that takes advantage of the features of the CDCE62005:

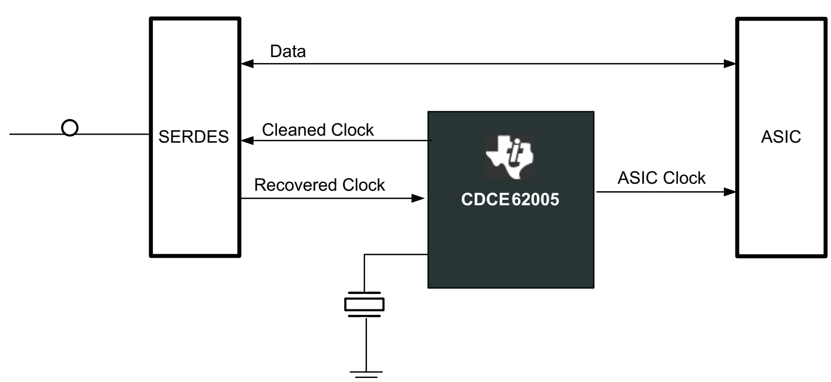


Figure 46. CDCE62005 SERDES Startup Overview

The functionality provided by the Smart Multiplexer provides a straightforward implementation of a SERDES clock link. The Auxiliary Input provides a startup clock because it connects to a crystal. The on-chip EEPROM determines the default configuration at power-up; therefore, the CDCE62005 requires no host communication to begin cleaning the recovered clock once it is available. The CDCE62005 immediately begins clocking the satellite components including the SERDES using the crystal as a clock source and a frequency reference. After the SERDES recovers the clock, the CDCE62005 removes the jitter via the on-chip synthesizer/loop filter. The recovered clock from the communications link becomes the frequency reference for the satellite system after the smart multiplexer automatically switches over to it. The CDCE62005 applies the cleaned clock to the recovered clock input on the SERDES; thereby establishing a reliable communications link between host and satellite systems.

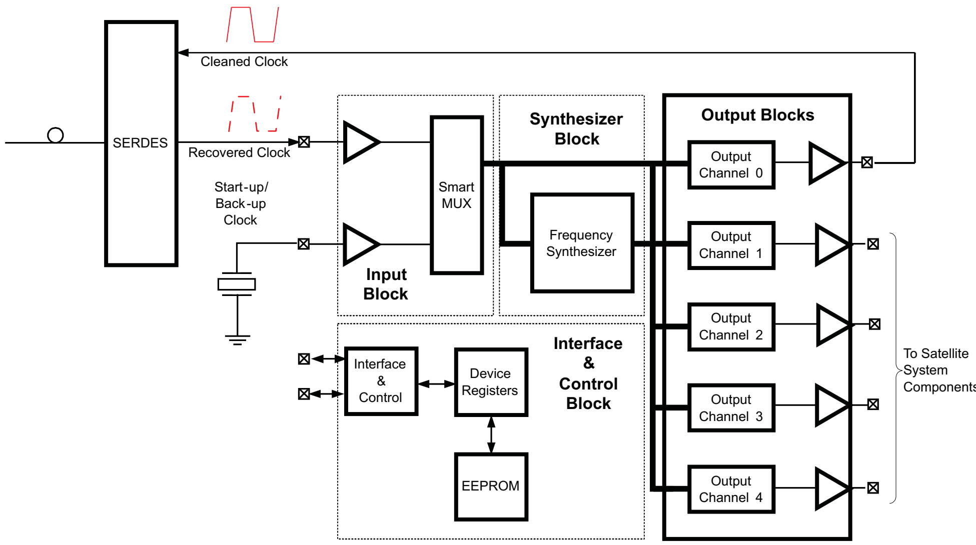


Figure 47. CDCE62005 SERDES Startup Mode

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July, 2009) to Revision C **Page**

- Deleted features involving single-ended clock sources and crystal auxiliary inputs 1
- Deleted *LVCMOS INPUT MODE (AUX_IN)* section from Electrical Characteristics table 12
- Deleted f_{REF} *Single-ended Inputs* .. from AUXILARY_IN REQUIREMENTS in the TIMING REQUIREMENTS table 18

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CDCE62005RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
CDCE62005RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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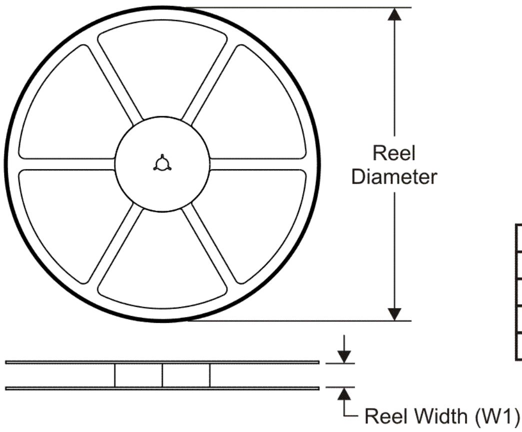
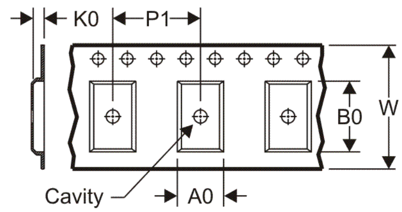
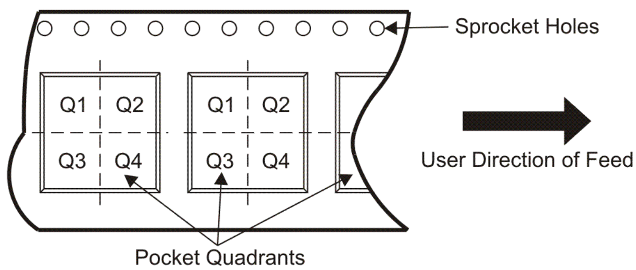




A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

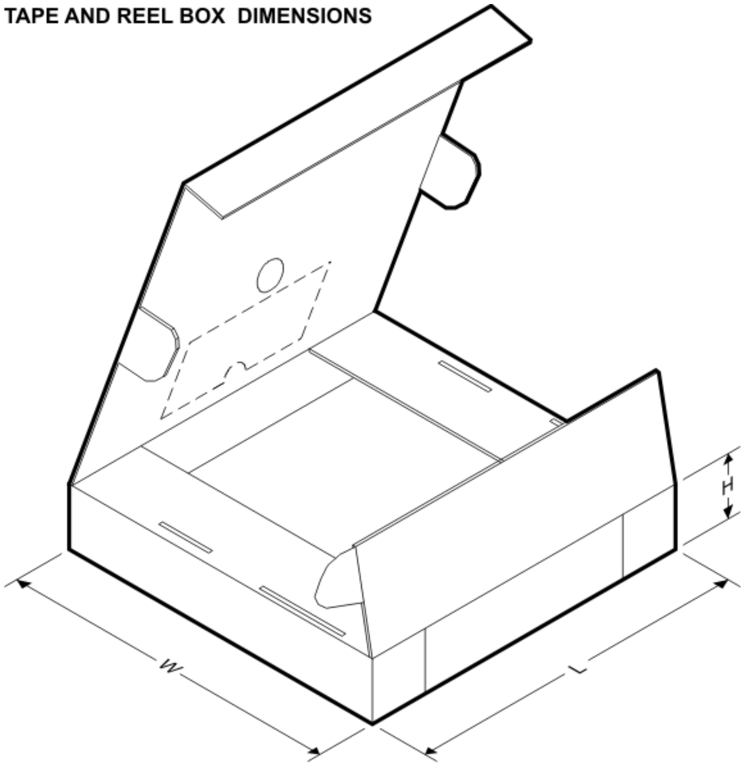
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE62005RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDCE62005RGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

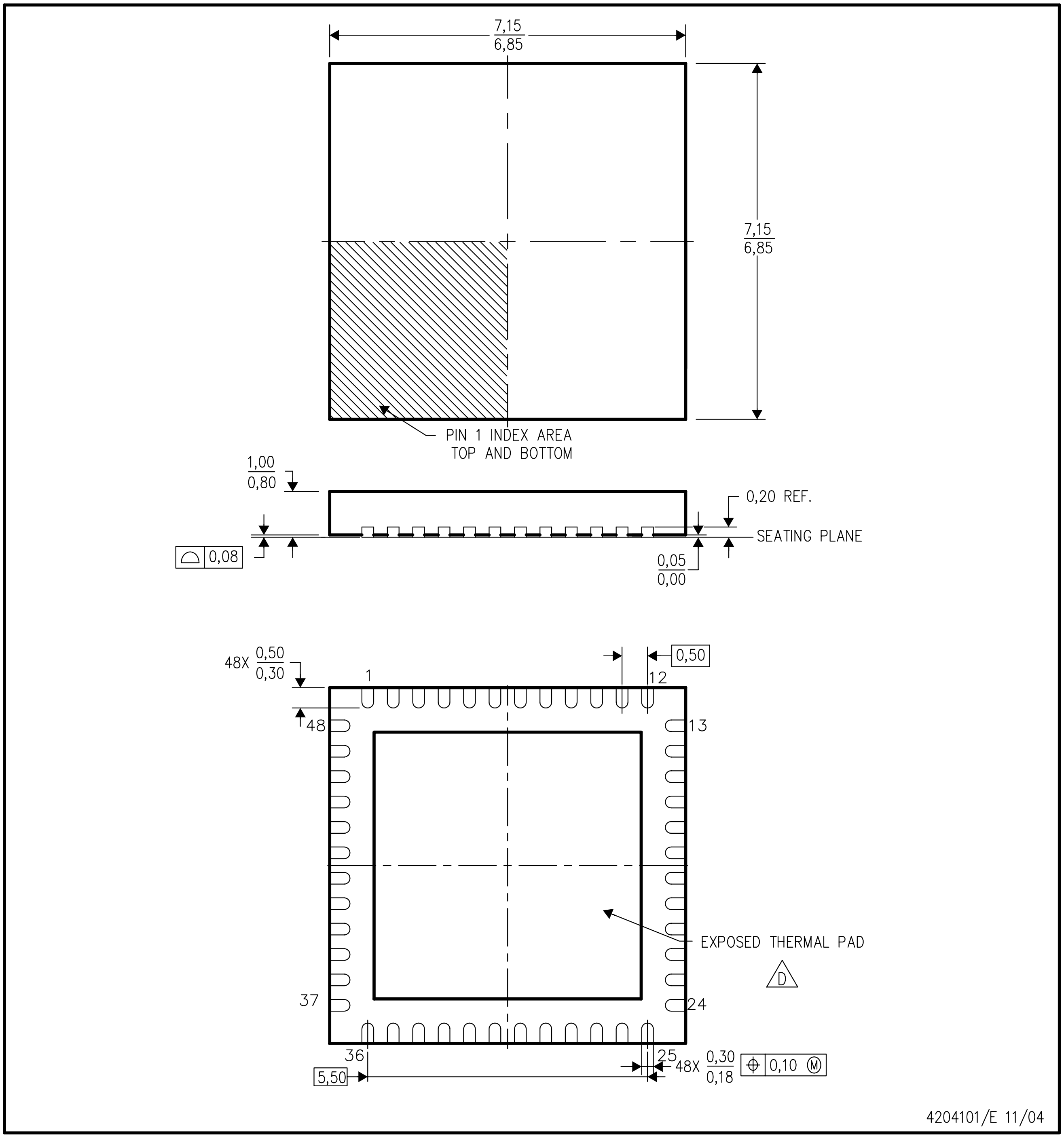
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE62005RGZR	VQFN	RGZ	48	2500	333.2	345.9	28.6
CDCE62005RGZT	VQFN	RGZ	48	250	333.2	345.9	28.6

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



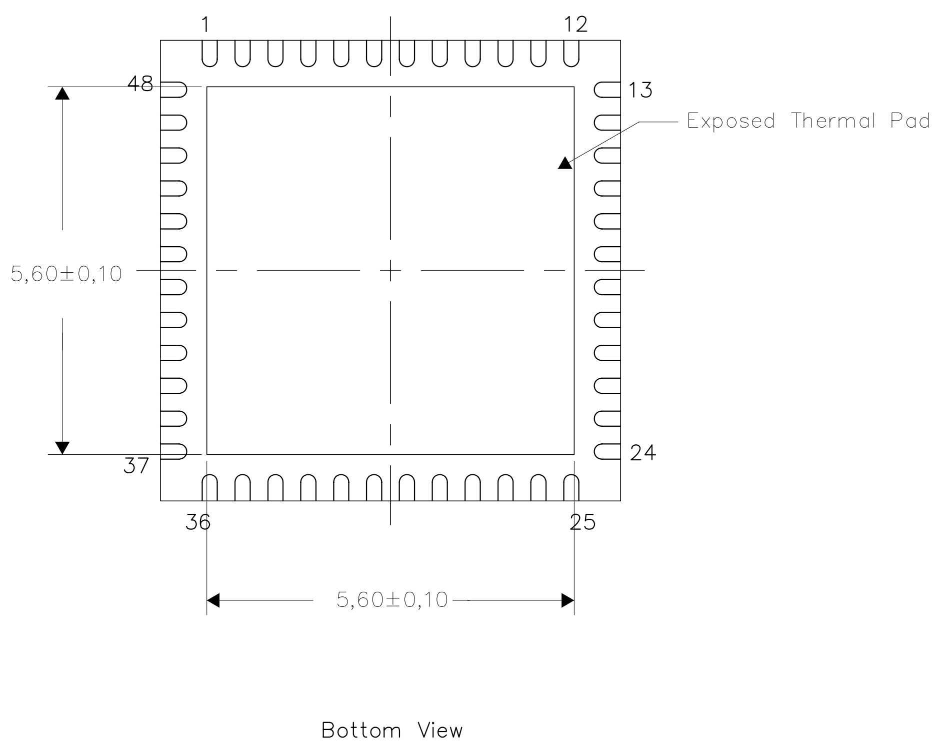
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

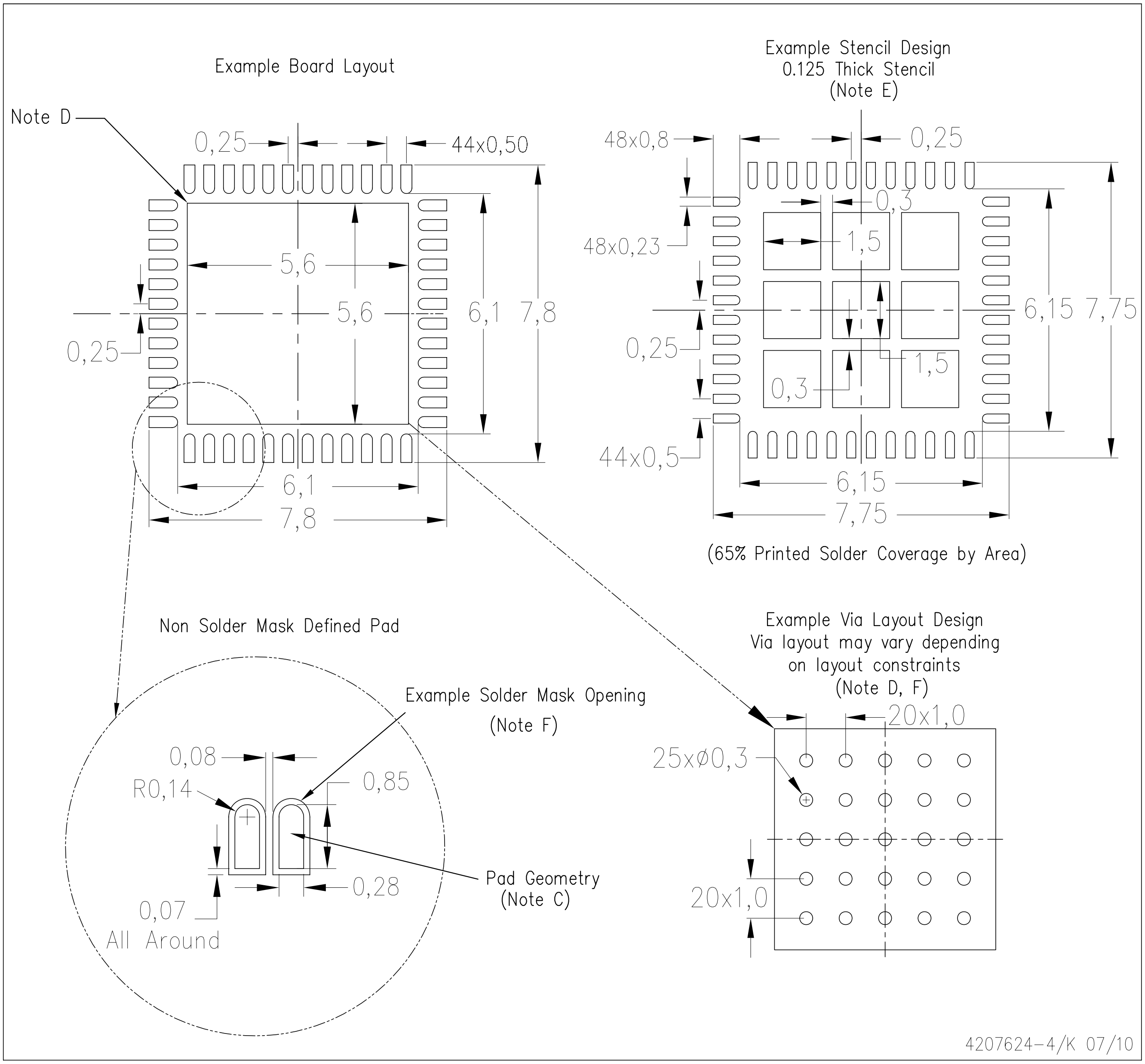
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S−PVQFN−N48) PLASTIC QUAD FLATPACK NO−LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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