REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23										
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
97-05-06

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, BICMOS, HIGH-SPEED OPTICAL/COPPER RECEIVER INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-96896
A	67268	

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E027-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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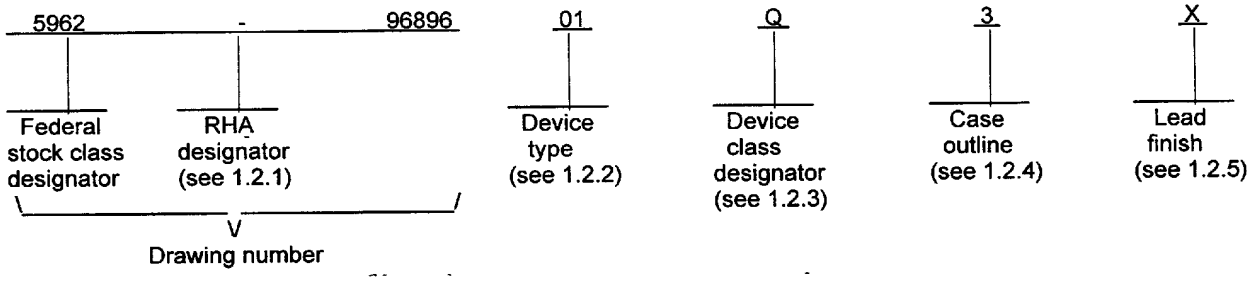
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7B933	High-speed optical/copper receiver interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
3	CQCC2-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) to ground potential continuous	-0.5 V to +7.0 V
DC voltage range applied to output	-0.5 V to V_{CC} maximum
DC input voltage range	-0.5 V to +7.0 V
DC output current (TTL LOW)	30 mA
DC output current (PECL HIGH)	-50 mA
DC input current	-30 to +0.5 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	2.6 W
Lead temperature (soldering, 10 seconds)	260°C
Thermal resistance Junction to case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	155°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	2.0 V
Maximum low-level input voltage (V_{IL})	0.8 V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{SC}.
3/ Values will be added when they become available.

HANDBOOKS

MIL-STD-

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein .

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Functional block/logic diagrams. The functional block/logic diagrams shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bus interface signals: Q_{0-7}, SC/$\overline{D}$, RVS, $\overline{RDY}$, CKR, SO, RF, REFCLK, MODE, $\overline{BTSTEN}$							
Output high voltage	V_{OHT}	V_{CC} = 4.5 V, I_{OH} = -2 mA V_{IN} = 0.0 V or 3.0 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OLT}	V_{CC} = 4.5 V, I_{OH} = 4 mA V_{IN} = 0.0 V or 3.0 V	1, 2, 3	All		0.45	V
Output short circuit current	I_{OST}	V_{OUT} = 0 V 2/	1, 2, 3	All	-15	-90	mA
Input high voltage	V_{IHT}		1, 2, 3	All	20	V_{CC}	V
Input low voltage	V_{ILT}		1, 2, 3	All	-0.5	0.8	V
Input high current	I_{IHT}	$V_{IN} = V_{CC}$	1, 2, 3	All	-10	+10	μA
Input low current	I_{ILT}	V_{IN} = 0.0 V	1, 2, 3	All		-500	μA
PECL interface signals: INB+, SI, A/B							
Input high voltage	V_{IHE}		1, 2, 3	All	V_{CC}-1.14	V_{CC}	V
Input low voltage	V_{ILE}		1, 2, 3	All	2.0	V_{CC}-1.5	V
Input high current 3/	I_{IHE}	$V_{IN} = V_{IHE}$ max	1, 2, 3	All		+500	μA
Input low current 3/	I_{ILE}	$V_{IN} = V_{ILE}$ min	1, 2, 3	All	+0.5		μA
Differential serial data inputs: INA+, INA-, INB+, INB-							
Differential input voltage	V_{DIFF}		1, 2, 3	All	0.05		V
Highest input voltage	V_{IHH}		1, 2, 3	All		V_{CC}	V
Lowest input voltage	V_{ILL}		1, 2, 3	All	2.0		V
Input high current	I_{IHH}	$V_{IN} = V_{IHH}$ max	1, 2, 3	All		750	μA
Input low current 4/	I_{LL}	$V_{IN} = V_{ILE}$ min	1, 2, 3	All	-200		μA
Miscellaneous: V_{CCN}, V_{CCQ}							
Power supply current 5/	I_{CCR}	Frequency = max	1, 2, 3	All	135	160	mA
Input capacitance	C_{IN}	f_o = 1 MHz, V_{CC} = 5.0 V See 4.4.1b	4	All		10	pF
Functional test		See 4.4.1c	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read clock reference, relative to REFCLK	t_1	6/	9, 10, 11	All	-1	+1	%
REFCLK clock period referenced to source word rate	t_2	7/	9, 10, 11	All	-0.1	+0.1	%
Read clock period	t_3	8/	9, 10, 11	All	30.3	62.5	ns
Bit time	t_4	Internal bit clock 9/ 13/	9 10, 11	All	3.03	6.25	ns
Read clock high pulse	t_5	8/	9, 10, 11	All	$5t_4$-3		ns
Read clock low pulse	t_6	8/	9, 10, 11	All	$5t_4$-3		ns
$\overline{RDY}$ hold time	t_7		9, 10, 11	All	t_4-3		ns
$\overline{RDY}$ pulse fall to CKR high	t_8		9, 10, 11	All	$5t_4$-3		ns
$\overline{RDY}$ pulse width high	t_9		9, 10, 11	All	$4t_4$-3		ns
Data access time	t_{10}	10/ 11/	9, 10, 11	All	$2t_4$-2	$2t_4$+4	ns
Data hold time	t_{11}	10/ 11/	9, 10, 11	All	t_4-3		ns
Data hold time from CKR rise	t_{12}	10/ 11/	9, 10, 11	All	$2t_4$-3		ns
REFCLK clock pulse high	t_{13}		9, 10, 11	All	6.5		ns
REFCLK clock pulse low	t_{14}		9, 10, 11	All	6.5		ns
Propagation delay SI to SO	t_{15}	12/	9, 10, 11	All		20	ns
Static alignment	t_{16}	13/ 14/	9 10, 11	All		100	ps
Error free window	t_{17}	13/ 15/	9 10, 11	All	$0.9t_4$		ps

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified, for dc test parameters, all test conditions shall be worst case conditions; V_{IH} = 2.0 V and V_{IL} = 0.8 V. For ac test parameters, all tests are performed using the input waveforms in figure 4. The following conditions also apply:

All timing references are made with respect to +1.5 V for TTL-level signals or to the 50% point between V_{OH} and V_{OL} for PECL levels. PECL input rise and fall times must be < 1 ns between the 20% and 80% points. TTL input rise and fall time must be < 1 ns between 1 V and 2 V points.

2/ Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.

3/ Applies to A/$\overline{B}$ only.

4/ Input currents are always positive at all voltages above $V_{CC}/2$.

5/ Maximum I_{CCR} is measured with V_{CC} = max, RF = low, and outputs unloaded.

6/ The period of t_1 will match the period of the transmitter byte clock when the receiver is receiving serial data. When data is interrupted, t_1 may drift to one of the range limits.

7/ The receiver REFCLK has no phase or frequency relationship to the CKR and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within 0.1% of the transmitted byte clock, necessitating a ±500 ppm crystal reference.

8/ This parameter does not apply during framing operations when a clock stretch can occur.

9/ Receiver bit time (t_4) is an internal clock that cannot be directly measured. It is calculated as $t_1/10$ when no data is being received, otherwise it tracks the received data stream.

10/ Data includes Q_{0-7}, SC/$\overline{D}$, and RVS.

11/ t_{10} and t_{11} specifications are only valid if all outputs (CKR, $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$ and RVS) are loaded with similar DC and AC loads.

12/ The PECL switching threshold is the midpoint between the PECL V_{OH} and V_{OL} specification (approximately V_{CC}-1.35 V). The TTL switching threshold is 1.5 V.

13/ Tested initially and after any design or process change that may affect these parameters, but not 100% tested. Not included in production and Group A testing. Supporting data on file to validate data limit.

14/ Static alignment is a measure of the alignment of the receiver sampling point relative to the center of a bit. Static alignment is measured by sliding one bit edge on 3000 nominal transitions until a bit error occurs.

15/ Error free window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter <50% Dj.

Device type	All	Device type	All	Device type	All	Device type	All
Case outline	3	Case outline	3	Case outline	3	Case outline	3
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	INA-	8	GND	15	Q_3 (Q_e)	22	CKR
2	INA+	9	V_{CCN}	16	Q_2 (Q_d)	23	SO
3	A/$\overline{B}$	10	RVS (Q_j)	17	Q_1 (Q_c)	24	V_{CCQ}
4	$\overline{BTSTEN}$	11	Q_7 (Q_h)	18	Q_0 (Q_b)	25	REFCLK
5	RF	12	Q_6 (Qg)	19	SC/$\overline{D}$ (Q_a)	26	MODE
6	GND	13	Q_5 (Q_f)	20	GND	27	SI (INB-)
7	$\overline{RDY}$	14	Q_4 (Q_i)	21	V_{CCQ}	28	SI (INB+)

FIGURE 1. Terminal connections.

Data byte name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data byte name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.2	010 00000	100111 0101	011000 0101
D1.0	000 00001	011101 0100	100010 1011	D1.2	010 00001	011101 0101	100010 0101
D2.0	000 00010	101101 0100	010010 1011	D2.2	010 00010	101101 0101	010010 0101
D3.0	000 00011	110001 1011	110001 0100	D3.2	010 00011	110001 0101	110001 0101
D4.0	000 00100	110101 0100	001010 1011	D4.2	010 00100	110101 0101	001010 0101
D5.0	000 00101	101001 1011	101001 0100	D5.2	010 00101	101001 0101	101001 0101
D6.0	000 00110	011001 1011	011001 0100	D6.2	010 00110	011001 0101	011001 0101
D7.0	000 00111	111000 1011	000111 0100	D7.2	010 00111	111000 0101	000111 0101
D8.0	000 01000	111001 0100	000110 1011	D8.2	010 01000	111001 0101	000110 0101
D9.0	000 01001	100101 1011	100101 0100	D9.2	010 01001	100101 0101	100101 0101
D10.0	000 01010	010101 1011	010101 0100	D10.2	010 01010	010101 0101	010101 0101
D11.0	000 01011	110100 1011	110100 0100	D11.2	010 01011	110100 0101	110100 0101
D12.0	000 01100	001101 1011	001101 0100	D12.2	010 01100	001101 0101	001101 0101
D13.0	000 01101	101100 1011	101100 0100	D13.2	010 01101	101100 0101	101100 0101
D14.0	000 01110	011100 1011	011100 0100	D14.2	010 01110	011100 0101	011100 0101
D15.0	000 01111	010111 0100	101000 1011	D15.2	010 01111	010111 0101	101000 0101
D16.0	000 10000	011011 0100	100100 1011	D16.2	010 10000	011011 0101	100100 0101
D17.0	000 10001	100011 1011	100011 0100	D17.2	010 10001	100011 0101	100011 0101
D18.0	000 10010	010011 1011	010011 0100	D18.2	010 10010	010011 0101	010011 0101
D19.0	000 10011	110010 1011	110010 0100	D19.2	010 10011	110010 0101	110010 0101
D20.0	000 10100	001011 1011	001011 0100	D20.2	010 10100	001011 0101	001011 0101
D21.0	000 10101	101010 1011	101010 0100	D21.2	010 10101	101010 0101	101010 0101
D22.0	000 10110	011010 1011	011010 0100	D22.2	010 10110	011010 0101	011010 0101
D23.0	000 10111	111010 0100	000101 1011	D23.2	010 10111	111010 0101	000101 0101
D24.0	000 11000	110011 0100	001100 1011	D24.2	010 11000	110011 0101	001100 0101
D25.0	000 11001	100110 1011	100110 0100	D25.2	010 11001	100110 0101	100110 0101
D26.0	000 11010	010110 1011	010110 0100	D26.2	010 11010	010110 0101	010110 0101
D27.0	000 11011	110110 0100	001001 1011	D27.2	010 11011	110110 0101	001001 0101
D28.0	000 11100	001110 1011	001110 0100	D28.2	010 11100	001110 0101	001110 0101
D29.0	000 11101	101110 0100	010001 1011	D29.2	010 11101	101110 0101	010001 0101
D30.0	000 11110	011110 0100	100001 1011	D30.2	010 11110	011110 0101	100001 0101
D31.0	000 11111	101011 0100	010100 1011	D31.2	010 11111	101011 0101	010100 0101
D0.1	001 00000	100111 1001	011000 1001	D0.3	011 00000	100111 0011	011000 1100
D1.1	001 00001	011101 1001	100010 1001	D1.3	011 00001	011101 0011	100010 1100
D2.1	001 00010	101101 1001	010010 1001	D2.3	011 00010	101101 0011	010010 1100
D3.1	001 00011	110001 1001	110001 1001	D3.3	011 00011	110001 1100	110001 0011
D4.1	001 00100	110101 1001	001010 1001	D4.3	011 00100	110101 0011	001010 1100
D5.1	001 00101	101001 1001	101001 1001	D5.3	011 00101	101001 1100	101001 0011
D6.1	001 00110	011001 1001	011001 1001	D6.3	011 00110	011001 1100	011001 0011
D7.1	001 00111	111000 1001	000111 1001	D7.3	011 00111	111000 1100	000111 0011
D8.1	001 01000	111001 1001	000110 1001	D8.3	011 01000	111001 0011	000110 1100
D9.1	001 01001	100101 1001	100101 1001	D9.3	011 01001	100101 1100	100101 0011
D10.1	001 01010	010101 1001	010101 1001	D10.3	011 01010	010101 1100	010101 0011
D11.1	001 01011	110100 1001	110100 1001	D11.3	011 01011	110100 1100	110100 0011
D12.1	001 01100	001101 1001	001101 1001	D12.3	011 01100	001101 1100	001101 0011
D13.1	001 01101	101100 1001	101100 1001	D13.3	011 01101	101100 1100	101100 0011
D14.1	001 01110	011100 1001	011100 1001	D14.3	011 01110	011100 1100	011100 0011
D15.1	001 01111	010111 1001	101000 1001	D15.3	011 01111	010111 0011	101000 1100
D16.1	001 10000	011011 1001	100100 1001	D16.3	011 10000	011011 0011	100100 1100
D17.1	001 10001	100011 1001	100011 1001	D17.3	011 10001	100011 1100	100011 0011
D18.1	001 10010	010011 1001	010011 1001	D18.3	011 10010	010011 1100	010011 0011
D19.1	001 10011	110010 1001	110010 1001	D19.3	011 10011	110010 1100	110010 0011
D20.1	001 10100	001011 1001	001011 1001	D20.3	011 10100	001011 1100	001011 0011
D21.1	001 10101	101010 1001	101010 1001	D21.3	011 10101	101010 1100	101010 0011
D22.1	001 10110	011010 1001	011010 1001	D22.3	011 10110	011010 1100	011010 0011
D23.1	001 10111	111010 1001	000101 1001	D23.3	011 10111	111010 0011	000101 1100
D24.1	001 11000	110011 1001	001100 1001	D24.3	011 11000	110011 0011	001100 1100
D25.1	001 11001	100110 1001	100110 1001	D25.3	011 11001	100110 1100	100110 0011
D26.1	001 11010	010110 1001	010110 1001	D26.3	011 11010	010110 1100	010110 0011
D27.1	001 11011	110110 1001	001001 1001	D27.3	011 11011	110110 0011	001001 1100
D28.1	001 11100	001110 1001	001110 1001	D28.3	011 11100	001110 1100	001110 0011
D29.1	001 11101	101110 1001	010001 1001	D29.3	011 11101	101110 0011	010001 1100
D30.1	001 11110	011110 1001	100001 1001	D30.3	011 11110	011110 0011	100001 1100
D31.1	001 11111	101011 1001	010100 1001	D31.3	011 11111	101011 0011	010100 1100

FIGURE 2. Truth table.

Data byte name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data byte name	Bits HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.4	100 00000	100111 0010	011000 1101	D0.6	110 00000	100111 0110	011000 0110
D1.4	100 00001	011101 0010	100010 1101	D1.6	110 00001	011101 0110	100010 0110
D2.4	100 00010	101101 0010	010010 1101	D2.6	110 00010	101101 0110	010010 0110
D3.4	100 00011	110001 1101	110001 0010	D3.6	110 00011	110001 0110	110001 0110
D4.4	100 00100	110101 0010	001010 1101	D4.6	110 00100	110101 0110	001010 0110
D5.4	100 00101	101001 1101	101001 0010	D5.6	110 00101	101001 0110	101001 0110
D6.4	100 00110	011001 1101	011001 0010	D6.6	110 00110	011001 0110	011001 0110
D7.4	100 00111	111000 1101	000111 0010	D7.6	110 00111	111000 0110	000111 0110
D8.4	100 01000	111001 0010	000110 1101	D8.6	110 01000	111001 0110	000110 0110
D9.4	100 01001	100101 1101	100101 0010	D9.6	110 01001	100101 0110	100101 0110
D10.4	100 01010	010101 1101	010101 0010	D10.6	110 01010	010101 0110	010101 0110
D11.4	100 01011	110100 1101	110100 0010	D11.6	110 01011	110100 0110	110100 0110
D12.4	100 01100	001101 1101	001101 0010	D12.6	110 01100	001101 0110	001101 0110
D13.4	100 01101	101100 1101	101100 0010	D13.6	110 01101	101100 0110	101100 0110
D14.4	100 01110	011100 1101	011100 0010	D14.6	110 01110	011100 0110	011100 0110
D15.4	100 01111	010111 0010	101000 1101	D15.6	110 01111	010111 0110	101000 0110
D16.4	100 10000	011011 0010	100100 1101	D16.6	110 10000	011011 0110	100100 0110
D17.4	100 10001	100011 1101	100011 0010	D17.6	110 10001	100011 0110	100011 0110
D18.4	100 10010	010011 1101	010011 0010	D18.6	110 10010	010011 0110	010011 0110
D19.4	100 10011	110010 1101	110010 0010	D19.6	110 10011	110010 0110	110010 0110
D20.4	100 10100	001011 1101	001011 0010	D20.6	110 10100	001011 0110	001011 0110
D21.4	100 10101	101010 1101	101010 0010	D21.6	110 10101	101010 0110	101010 0110
D22.4	100 10110	011010 1101	011010 0010	D22.6	110 10110	011010 0110	011010 0110
D23.4	100 10111	111010 0010	000101 1101	D23.6	110 10111	111010 0110	000101 0110
D24.4	100 11000	110011 0010	001100 1101	D24.6	110 11000	110011 0110	001100 0110
D25.4	100 11001	100110 1101	100110 0010	D25.6	110 11001	100110 0110	100110 0110
D26.4	100 11010	010110 1101	010110 0010	D26.6	110 11010	010110 0110	010110 0110
D27.4	100 11011	110110 0010	001001 1101	D27.6	110 11011	110110 0110	001001 0110
D28.4	100 11100	001110 1101	001110 0010	D28.6	110 11100	001110 0110	001110 0110
D29.4	100 11101	101110 0010	010001 1101	D29.6	110 11101	101110 0110	010001 0110
D30.4	100 11110	011110 0010	100001 1101	D30.6	110 11110	011110 0110	100001 0110
D31.4	100 11111	101011 0010	010100 1101	D31.6	110 11111	101011 0110	010100 0110
D0.5	101 00000	100111 1010	011000 1010	D0.7	111 00000	100111 0001	011000 1110
D1.5	101 00001	011101 1010	100010 1010	D1.7	111 00001	011101 0001	100010 1110
D2.5	101 00010	101101 1010	010010 1010	D2.7	111 00010	101101 0001	010010 1110
D3.5	101 00011	110001 1010	110001 1010	D3.7	111 00011	110001 1110	110001 0001
D4.5	101 00100	110101 1010	001010 1010	D4.7	111 00100	110101 0001	001010 1110
D5.5	101 00101	101001 1010	101001 1010	D5.7	111 00101	101001 1110	101001 0001
D6.5	101 00110	011001 1010	011001 1010	D6.7	111 00110	011001 1110	011001 0001
D7.5	101 00111	111000 1010	000111 1010	D7.7	111 00111	111000 1110	000111 0001
D8.5	101 01000	111001 1010	000110 1010	D8.7	111 01000	111001 0001	000110 1110
D9.5	101 01001	100101 1010	100101 1010	D9.7	111 01001	100101 1110	100101 0001
D10.5	101 01010	010101 1010	010101 1010	D10.7	111 01010	010101 1110	010101 0001
D11.5	101 01011	110100 1010	110100 1010	D11.7	111 01011	110100 1110	110100 0001
D12.5	101 01100	001101 1010	001101 1010	D12.7	111 01100	001101 1110	001101 0001
D13.5	101 01101	101100 1010	101100 1010	D13.7	111 01101	101100 1110	101100 0001
D14.5	101 01110	011100 1010	011100 1010	D14.7	111 01110	011100 1110	011100 0001
D15.5	101 01111	010111 1010	101000 1010	D15.7	111 01111	010111 0001	101000 1110
D16.5	101 10000	011011 1010	100100 1010	D16.7	111 10000	011011 0001	100100 1110
D17.5	101 10001	100011 1010	100011 1010	D17.7	111 10001	100011 1110	100011 0001
D18.5	101 10010	010011 1010	010011 1010	D18.7	111 10010	010011 1110	010011 0001
D19.5	101 10011	110010 1010	110010 1010	D19.7	111 10011	110010 1110	110010 0001
D20.5	101 10100	001011 1010	001011 1010	D20.7	111 10100	001011 1110	001011 0001
D21.5	101 10101	101010 1010	101010 1010	D21.7	111 10101	101010 1110	101010 0001
D22.5	101 10110	011010 1010	011010 1010	D22.7	111 10110	011010 1110	011010 0001
D23.5	101 10111	111010 1010	000101 1010	D23.7	111 10111	111010 0001	000101 1110
D24.5	101 11000	110011 1010	001100 1010	D24.7	111 11000	110011 0001	001100 1110
D25.5	101 11001	100110 1010	100110 1010	D25.7	111 11001	100110 1110	100110 0001
D26.5	101 11010	010110 1010	010110 1010	D26.7	111 11010	010110 1110	010110 0001
D27.5	101 11011	110110 1010	001001 1010	D27.7	111 11011	110110 0001	001001 1110
D28.5	101 11100	001110 1010	001110 1010	D28.7	111 11100	001110 1110	001110 0001
D29.5	101 11101	101110 1010	010001 1010	D29.7	111 11101	101110 0001	010001 1110
D30.5	101 11110	011110 1010	100001 1010	D30.7	111 11110	011110 0001	100001 1110
D31.5	101 11111	101011 1010	010100 1010	D31.7	111 11111	101011 0001	010100 1110

FIGURE 3. Truth table - Continued.

Decoder patterns, special codes.

Special character byte name 5/	Special character code name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
		Command codes		
K28.0	C0.0 (C00)	000 00000	001111 0100	110000 1011
K28.1	C1.0 (C01)	000 00001	001111 1001	110000 0110
K28.2	C2.0 (C02)	000 00010	001111 0101	110000 1010
K28.3	C3.0 (C03)	000 00011	001111 0011	110000 1100
K28.4	C4.0 (C04)	000 00100	001111 0010	110000 1101
K28.5	C5.0 (C05)	000 00101	001111 1010	110000 0101
K28.6	C6.0 (C06)	000 00110	001111 0110	110000 1001
K28.7	C7.0 (C07)	000 00111	001111 1000	110000 0111
K23.7	C8.0 (C08)	000 01000	111010 1000	000101 0111
K27.7	C9.0 (C09)	000 01001	110110 1000	001001 0111
K29.7	C10.0 (C0A)	000 01010	101110 1000	010001 0111
K30.7	C11.0 (C0B)	000 01011	011110 1000	100001 0111
		Sequence detected codes		
C-SOF	C7.1 (C27)	001 00111	001111 1000	110000 0111
P-SOF	C7.2 (C47)	010 00111	001111 1000	110000 0111
		Exception codes		
Invalid data	C0.7 (CE0)	111 00000	xxxxxx xxxx	xxxxxx xxxx
-K28.5	C1.7 (CE1)	111 00001	001111 1010	001111 1010
+K28.5	C2.7 (CE2)	111 00010	110000 0101	110000 0101
Invalid RD	C4.7 (CE4)	111 00100	xxxxxx xxxx	xxxxxx xxxx

FIGURE 2. Truth table - Continued.

1/ Coding tables are only used when the transmitter is in Encoded mode (MODE = low).

2/ The notation used for the encoding tables follows that in ANSI X3.230-1994.

3/ Notation conventions:

a. Letters are used to represent bit positions within a character.
b. Captital letters (A, B, C, D, E, F, G, and H) represnt the unencoded bit postions of an 8-bit byte.
c. Lower case letters (a, b, c, d, e, i, f, g, h, and j) represnt the encoded bit positions of a 10-bit transmission character.
d. Bit positions of the unencoded byte are:

Receiver output - Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0
Letter designator - H G F E D C B A
MSB LSB

e. Bit positions of the encoded transmission character
Serial data input - j h g f i e d c b a
MSB LSB

f. Data byte name is a decimal notation based on unencoded character bit groupings.
Note reversed order of bits:
Data Byte - D5.2
Bit Names - ABCDE FGH
Bits - 10100 010

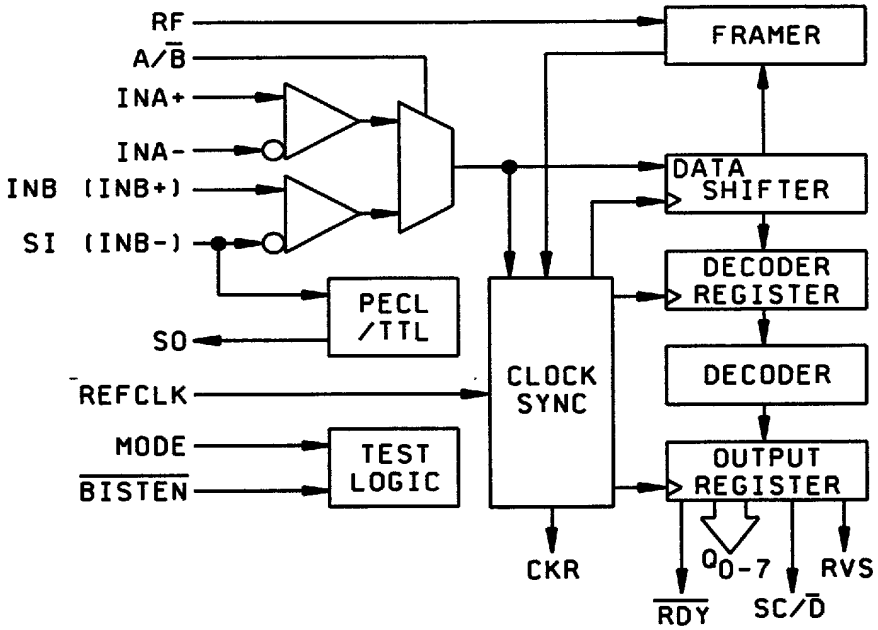
4/ Serial transmission characters are transmitted LSB first.

5/ Notation for Special Character byte names is patterned to match that of the data names.

6/ The C7.0, C7.1, and C7.2 special codes are all decoded from the same K28.7 transmission character. A C7.1 will be decoded if the immediately preceding character was a C1.0 (K28.1). A C7.2 will be decoded if the immediatley preceding character was a C5.0 (K28.5). A C7.0 will be decoded in all other cases.

7/ Exception codes are used to indicate the detection of errors in the received serial data stream.
a. A C0.7 indicates that the received 10-bit transmission character did not map to any valid data or special character, of any disparity.
b. A c1.7 indicates that a valid K28.5 character was received, however the character received had a negative running disparity (RD) when the receiver was expecting a positive RD.
c. A c2.7 indicates that a valid K28.5 character was received, however the character received had a positive running disparity (RD) when the receiver was expecting a negative RD.
d. A C4.7 indicates that the received 10-bit transmission character did map to any valid data or special character, however the character disparity was not correct. This may indicate an error in a previous character.

FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL

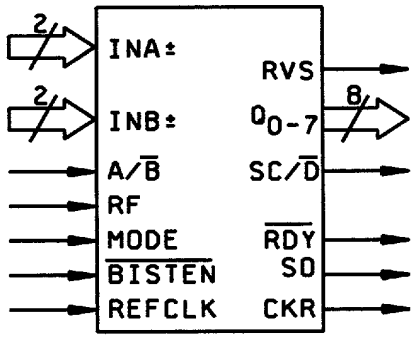


FIGURE 3. Functional block/logic diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96896
		REVISION LEVEL	SHEET 13

Key to switching waveforms

Waveform symbol	Inputs	Outputs
	MUST BE Steady	WILL BE Steady
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

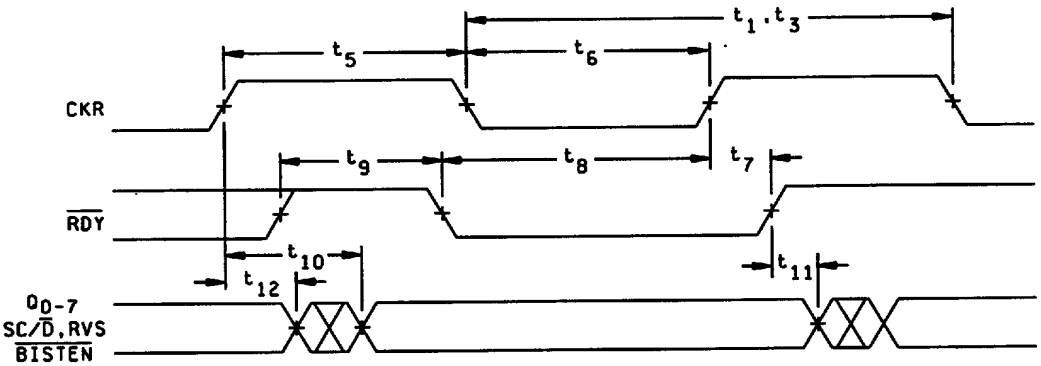


FIGURE 4. Switching waveforms and test circuit.

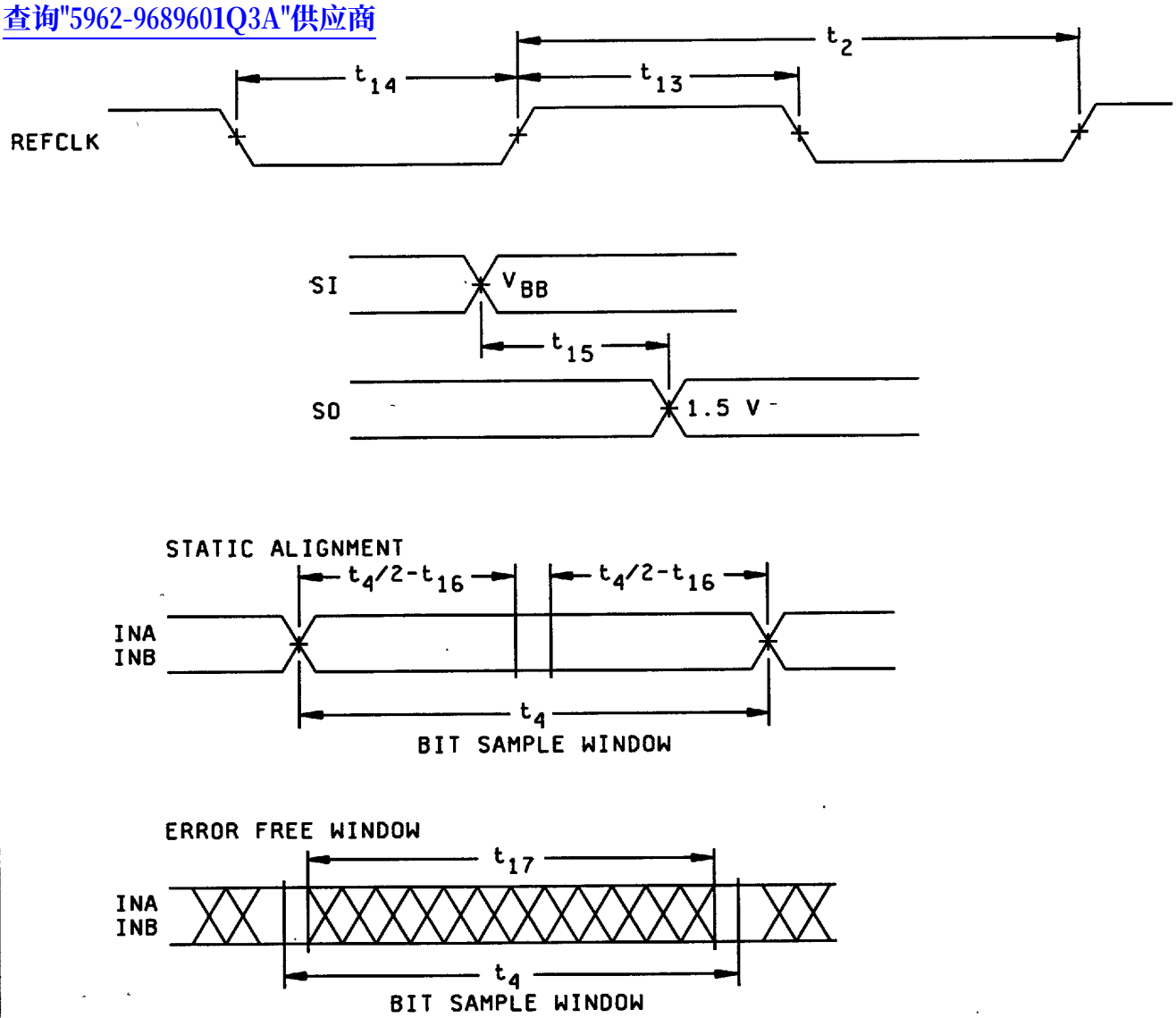
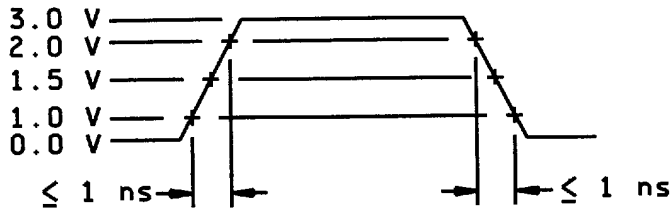
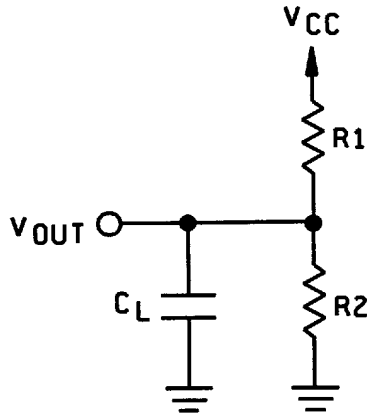


FIGURE 4. Switching waveforms and test circuit - Continued.



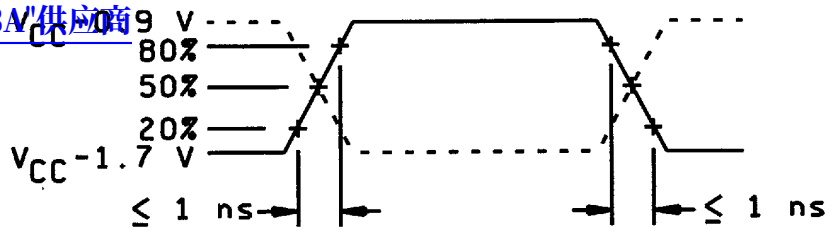
TTL INPUT WAVEFORM
(USED FOR TABLE I AC
ELECTRICAL PERFORMANCE TESTING)



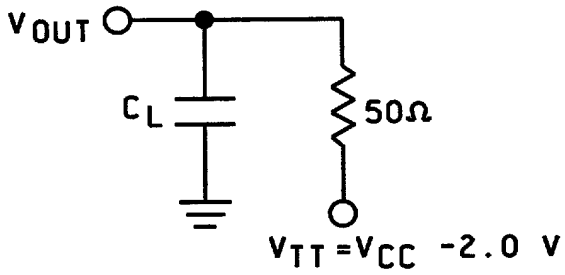
TTL OUTPUT LOAD

NOTES:
R_1 = 910Ω, R_2 = 510Ω.
C_L < 30 pF, includes scope probe, wiring and stray capacitance without device in test fixture. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.



ECL INPUT WAVEFORM
(USED FOR TABLE I AC
ELECTRICAL PERFORMANCE TESTING)



ECL OUTPUT LOAD

NOTES:
C_L < 5 pF, includes scope probe, wiring and stray capacitance without device in test fixture. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.
b. Subgroup 4 (C_{IN} measurments) shall be measured only for the initial test and after process or design changes which may affect capacitance. Tests shall be suffcient to validate limits as defined in Table I.
c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

Symbol	Name and function
Q_{0-7} (Q_{b-h})	**Q_{0-7} Parallel Data Output (TTL output).** Q_{0-7} contain the most recently received data. These outputs change synchronously with CKR. When MODE is high, $Q_{0, 1, \ldots 7}$ become $Q_{b, c, \ldots h}$ respectively.
SC/$\overline{D}$ (Q_a)	**Special Character/Data Select (TTL output).** SC/$\overline{D}$ indicates the context of the received data. High indicates a Control character (Special Code), low indicates a Data character. When MODE is high (placing the receiver in Unencoded mode), SC/$\overline{D}$ acts as the Q_a output. SC/$\overline{D}$ has the same timing as Q_{0-7}.
RVS (Q_j)	**Received Violation Symbol (TTL output).** A high on RVS indicates that a code violation has been detected in the received data stream. A low shows that no error has been detected. In BIST (Built-In Self-Test) mode, a low on RVS indicates correct operation of the transmitter, receiver, and link on a byte-by-byte basis. When MODE is high (placing the receiver in Unencoded mode), RVS acts as the Q_j output. RVS has the same timing as Q_{0-7}.
$\overline{RDY}$	**Data Output Ready (TTL output).** A low pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In BIST mode $\overline{RDY}$ will remain low for all but the last byte of a test loop and will pulse high one byte time per BIST loop.
CKR	**Clock Read (TTL output).** This byte rate clock output is phase and frequency aligned to the incoming serial data. $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	**Serial Data Input Select (PECL input).** This PECL 100K (+5 V referenced) input selects INA or INB as the active serial data input. If A/$\overline{B}$ is high, INA is connected to the shifter and signals connected to INA will be decoded. If A/$\overline{B}$ is low INB is selected.
INA+, INA-	**Serial Data Input A (differential PECL input).** The differential signal at the receiver end of the communications link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternate data input, as selected by the state of A/$\overline{B}$

6.5 - Continued.

INB-	**Serial Data Input B (single-ended or differential PECL input).** This input is either a single ended PECL data receiver (INB) or half of the INB differential pair. If SO is wired to V_{CC}, then INB± can be used as a differential line receiver interchangeably with INA±. If SO is normally connected and loaded, INB becomes a single-ended PECL 100K (+5 V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB-)	**Status Input (single-ended or differential PECL input).** This input is either a single-ended PECL status monitor input (SI) or half of the INB differential pair. If SO is wired to V_{CC}, then INB± can be used as a differential line receiver interchangeably with INA±. If SO is normally connected and loaded, SI becomes a single-ended PECL 100K (+5 V referenced) status monitor input, which is translated to a TTL-level signal at the SO output.
BTSTEN	**Built-In Self-Test Enable (TTL input) .** When BTSTEN is low, the receiver awaits a D0.0 character (sent once per BIST loop) and begins a continuous test sequence that tests the functionality of the transmitter, the receiver, and the link connecting them. In BIST mode the status of the test can be monitored with the RDY and RVS outputs. In normal use BTSTEN is held high or wired to V_{CC}.
SO	**Status Output (TTL output).** SO is the TTL translated output of SI. It is typically used to translate the Carrier Detect output from a fiber-optic receiver connected to SI. When this pin is normally connected and loaded (without an external pull-up resistor), SO will assume the same logic level as SI and INB will become a single-ended PECL serial dtat input. If the status monitor translation is not desired, then SO may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
RF	**Reframe Enable (TTL input).** RF controls the framer logic in the receiver. When RF is held high, each Sync or Null (K28.5) symbol detected in the shifter will frame the data that follows. If RF is high for 2048 consectutive bytes, the internal framer switches to double byte mode. When RF is held low, the framing logic is disabled. The incoming serial data stream is then continuously deserialized and decoded using byte boundries set by the internal byte counter. Bit error in the data stream will not cause alias Sync characters to reframe the data erroneously.
REFCLK	**Reference Clock (TTL input).** REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream.. REFCLK must be connected to crystalpcontrolled time base that runs within the frequency limits of the Tx/RX pair, and the frequency must be the same as the transmitter byte cock frequency (within ±0.1%).
MODE	**Decoder Mode Select (3-level input).** The level on the MODE input determines the decoding method to be used. When wired to GND, MODE selects 8B/10B decoding. When wired to V_{CC}, registered shifter contents bypass the decoder and are sent to Q_{a-j} directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.
V_{CCN}, V_{CCQ}	**Power supply.** V_{CCN} and V_{CCQ} are +5.0 Volt nominal power supply pins. V_{CCN} provides power for the output drivers. V_{CCQ} provides power for the internal circuitry.
GND	**Ground Pins.** Power supply and signal ground.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-05-06

Approved sources of supply for SMD 5962-96896 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9689601Q3A	65786	CY7B933LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.