REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to table I, table II, 4.3.1, 6.4, and figure 3. Editorial changes throughout.	1989 JAN 27	M. A. Frye
B	Add device type 02. Add one vendor, CAGE 44270. Make changes to table I, figure 2, and figure 3. Make editorial changes throughout.	1990 MAR 28	M. A. Frye

REV																								
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REV STATUS OF SHEETS	REV	B	A	B	B	B	B	B		B	A	A	B	B	B	B								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick C. Offinger

CHECKED BY: Charles E. Besore

APPROVED BY: M. A. Frye

DRAWING APPROVAL DATE: 21 APRIL 1988

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, CMOS ARINC BUS INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-86880

SHEET 1 OF 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1633

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86880	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS3282	CMOS ARINC bus interface circuit 1/
02	HI8282	CMOS ARINC bus interface circuit 1/

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings. 2/

Supply voltage (V_{CC})	7.0 V dc
Voltage at any pin (except 2, 3, 4, and 5)	GND -0.3 V dc to V_{CC} +0.3 V dc
Voltage at pins 2, 3, 4, and 5	-29 V dc to +29 V dc
Storage temperature range (T_{stg})	-65°C to +150°C
Power dissipation (P_D):	
Case Q	1.875 W at +25°C 3/
Case X	1.25 W at +25°C 3/
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
ARINC inputs:	
Logic "1" input voltage (V_{IH})	6.7 V dc minimum to 13 V dc maximum
Logic "0" input voltage (V_{IL})	-6.7 V dc minimum to -13 V dc maximum
Null input voltage (V_{IN})	-2.5 V dc minimum to +2.5 V dc maximum
Common mode voltage V (V_{CH})	-5 V dc minimum to +5 V dc maximum

1/ This circuit was designed to be compatible with the Aeronautical Radio, Incorporated (ARINC), specification 429 serial communications protocol. The applicable specifications are designed in this drawing.
2/ All voltages referenced to V_{SS}.
3/ Derate above +25°C, 12.5 mW/°C for case Q and 8.3 mW/°C for case X.

Bi-directional inputs:
Logic "1" input voltage (V_{IH})- - - - - - - - - - - 2.1 V dc minimum
Logic "0" input voltage (V_{IL})- - - - - - - - - - - 0.7 V dc maximum
All other inputs:
Logic "1" input voltage (V_{IH})- - - - - - - - - - - 3.5 V dc minimum
Logic "0" input voltage (V_{IL})- - - - - - - - - - - 0.7 V dc maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Logic "1" output voltage	V_{OH}	I_{OH} = -1.5 mA, V_{CC} = 5.0 V	All	1, 2, 3	2.7		V
Logic "0" output voltage	V_{OL}	I_{OL} = 1.8 mA, V_{CC} = 5.0 V	All	1, 2, 3		0.4	V
Output capacitance	C_O	T_A = +25°C 1/	All	4		15	pF
Supply current (standby)	I_{CC1}	V_{CC} = 5.25 V, V_{IN} = 0 V	All	1, 2, 3		20	mA
Supply current (operation)	I_{CC2}	V_{CC} = 5.25 V 2/	All	1, 2, 3		20	mA
Input leakage 3/	I_{IL}	V_{IN} = 0 V	01	1, 2, 3	-75		µA
		V_{IN} = 0 V, maximum pull-up current	02		-20		
	I_{IH}	V_{IN} = V_{CC}	All	1, 2, 3		10	µA
Input leakage (bi-directional input)	I_I	0 V $\le V_{IN} \le V_{CC}$	All	1, 2, 3	-1.5	1.5	µA
Input leakage (ARINC input)	I_{IL}	V_{IN} = 0 V	All	1, 2, 3	-450		µA
Input leakage (ARINC input)	I_{IH}	V_{IN} = V_{IH}	01	1, 2, 3		200	µA
		V_{CC} = 5.25 V, V_{IN} = V_{CC}	02			200	
Input impedance to V_{CC} (ARINC input)	R_H		All	4, 5, 6	12		kΩ
Input capacitance to V_{CC} (ARINC input)	C_H	T_A = +25°C 1/	All	4		20	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input capacitance to GND (ARINC input)	C_G	$T_A = +25°C$ 1/	All	4		20	pF
Differential input impedence (ARINC input)	R_I		All	4, 5, 6	12		kΩ
Input capacitance (all other inputs)	C_I	$T_A = +25°C$ 1/	All	4		15	pF
Input impedance to GND (ARINC input)	R_G		All	4, 5, 6	12		kΩ
Differential input capacitance (ARINC input	C_I	$T_A = +25°C$ 1/	All	4		20	pF
Clock frequency	F_C	V_{CC} = 4.75 V and 5.25 V, 50% duty cycle 5/	All	7, 8		1	MHz
Data rate	F_D	V_{CC} = 4.75 V and 5.25 V	All	7, 8		100	kHz
Data select to data enable time	t_{SELEN}	See figure 3	All	9, 10, 11	20		ns
Output data disable time	t_{DATAEN}	See figure 3 1/	01	9, 10, 11		30	ns
			02			150	
Control word register strobe pulse width	t_{CWSTR}	See figure 3	All	9, 10, 11	130		ns
Transmitter ready delay time	$t_{TX/R}$	See figure 3	All	9, 10, 11		840	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Data word setup time	t_{DWSET}	See figure 3	All	9, 10, 11	110		ns
Data word hold time	t_{DWHLD}	See figure 3	01	9, 10, 11	0		ns
			02		20		
Enable transmit to output data valid time	t_{ENDAT}	See figure 3 FD = 12.5 kbps	All	9, 10, 11		200	µs
		See figure 3 FD = 100 kbps				25	
Output data bit time	t_{BIT}	See figure 3 FD = 12.5 kbps	All	9, 10, 11	39.6	40.4	µs
		See figure 3 FD = 100 kbps			4.95	5.05	
Output data null time	t_{NUL}	See figure 3 FD = 12.5 kbps	All	9, 10, 11	39.6	40.4	µs
		See figure 3 FD = 100 kbps			4.95	5.05	
Data transmission word to $t_{X/R}$ set time	$t_{DTX/R}$	See figure 3	01	9, 10, 11		400	ns
		See figure 3 FD = 12.5 kbps	02			38.5	µs
		See figure 3 FD = 100 kbps				3.5	
Enable transmit turn-off time	t_{ENTXR}	See figure 3	All	9, 10, 11	0		ns
Data word gap time	t_{GAP}	See figure 3 FD = 12.5 kbps	All	9, 10, 11	316.8	323.2	µs
		See figure 3 FD = 100 kbps			39.6	40.4	
Data enable to parallel load delay time	t_{ENPL}	See figure 3	All	9, 10, 11	0		ns
Data enable hold for parallel hold time	t_{PLEN}	See figure 3	All	9, 10, 11	0		ns
Enable transmit delay time	$t_{TX/REN}$	See figure 3	All	9, 10, 11	0		ns
Control word setup time	t_{CWSET}	See figure 3	01	9, 10, 11	130		ns
			02		140		

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Control word hold time	t_{CWHLD}	See figure 3	01	9, 10, 11	0		ns
			02		40		
Parallel load pulse width	t_{PL}	See figure 3	All	9, 10, 11	200		ns
Parallel load 1 to parallel load 2 delay	t_{PL12}	See figure 3	All	9, 10, 11	0		ns
Clock rise time	t_{LHC}	See figure 3 1/	01	9, 10, 11		10	ns
Master reset pulse width	t_{MR}	See figure 3	01	9, 10, 11	200		ns
			02		400		
Receiver device ready time from 32nd data bit	$t_{D/R2}$	See figure 3 6/ FD = 12.5 kbps	All	9, 10, 11		128	µs
		FD = 100 kbps				16	
Device ready to enable time	$t_{D/REN}$	See figure 3	All	9, 10, 11	0		ns
Data enable pulse width	t_{EN}	See figure 3	01	9, 10, 11	200		ns
			02		240		
Data enable to data enable time	t_{ENEN}	See figure 3	All	9, 10, 11	50		ns
Data enable to device ready time	$t_{END/R}$	See figure 3	All	9, 10, 11		200	ns
Output data valid to enable time	t_{ENDATA}	See figure 3	All	9, 10, 11		200	ns
Data enable to data select time	t_{ENSEL}	See figure 3	01	9, 10, 11	20		ns
			02		50		

1/ Guaranteed but only tested initially and after design changes.
2/ V_{IN} = Logic "1" for all inputs except pins 8 and 33 which are logic "0".
3/ For case Q: Pins 8, 9, 10, 28, 29, 33, 34, 37, and 39.
For case X: Pins 10, 11, 12, 31, 32, 36, 37, 41, and 43.
4/ AC test conditions: V_{CC} = 5.0 V.
5/ 60 to 40 percent duty cycle is acceptable.
6/ Same delay for 25-bit word format. Device 01 only.

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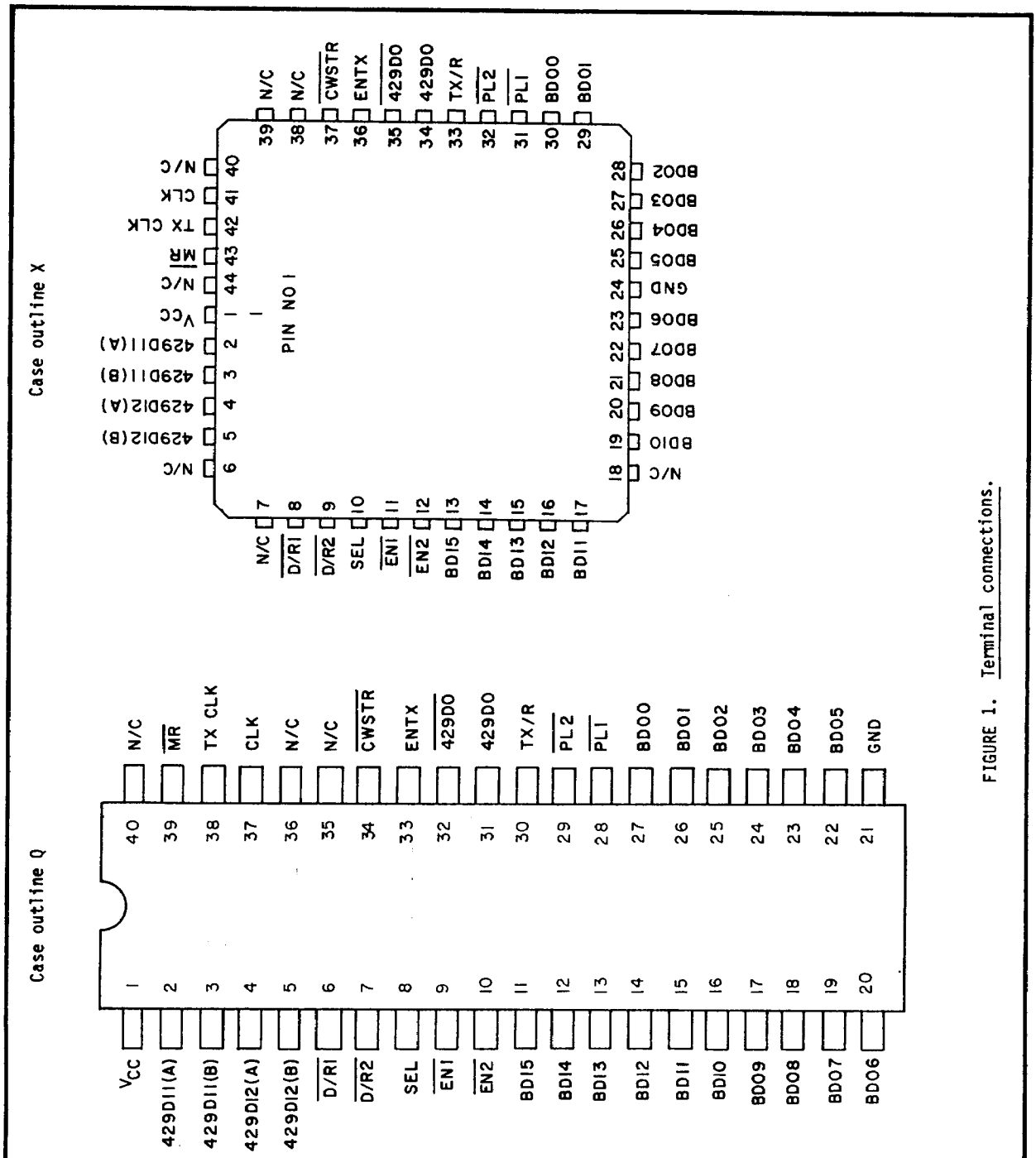

FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86880
		REVISION LEVEL	SHEET 8

DESC FORM 193A
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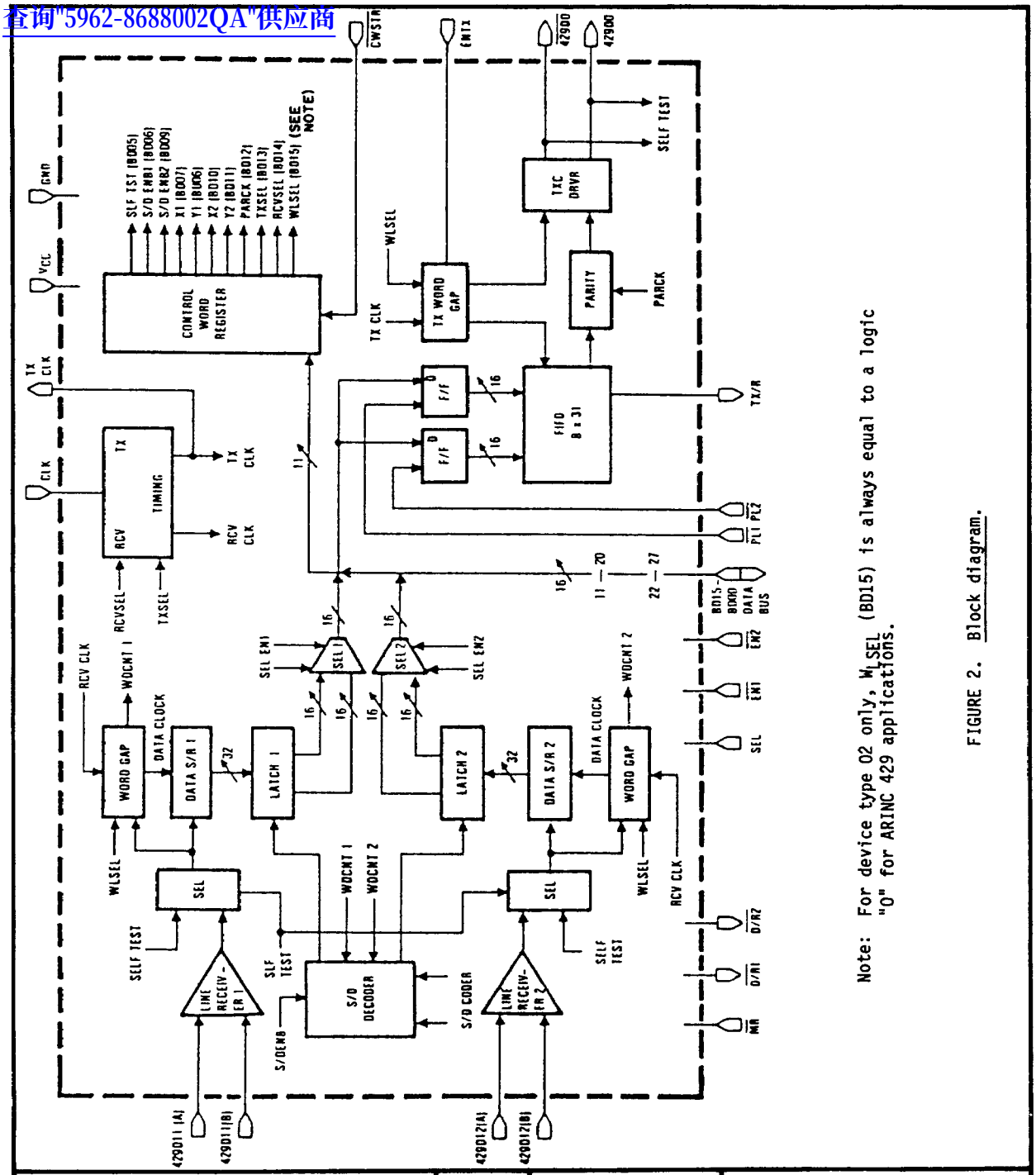
☆ U.S. GOVERNMENT PRINTING OFFICE: 1988—549-904



Note: For device type 02 only, W_{LSEL} (BD15) is always equal to a logic "0" for ARINC 429 applications.

FIGURE 2. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86880
		REVISION LEVEL B	SHEET 9

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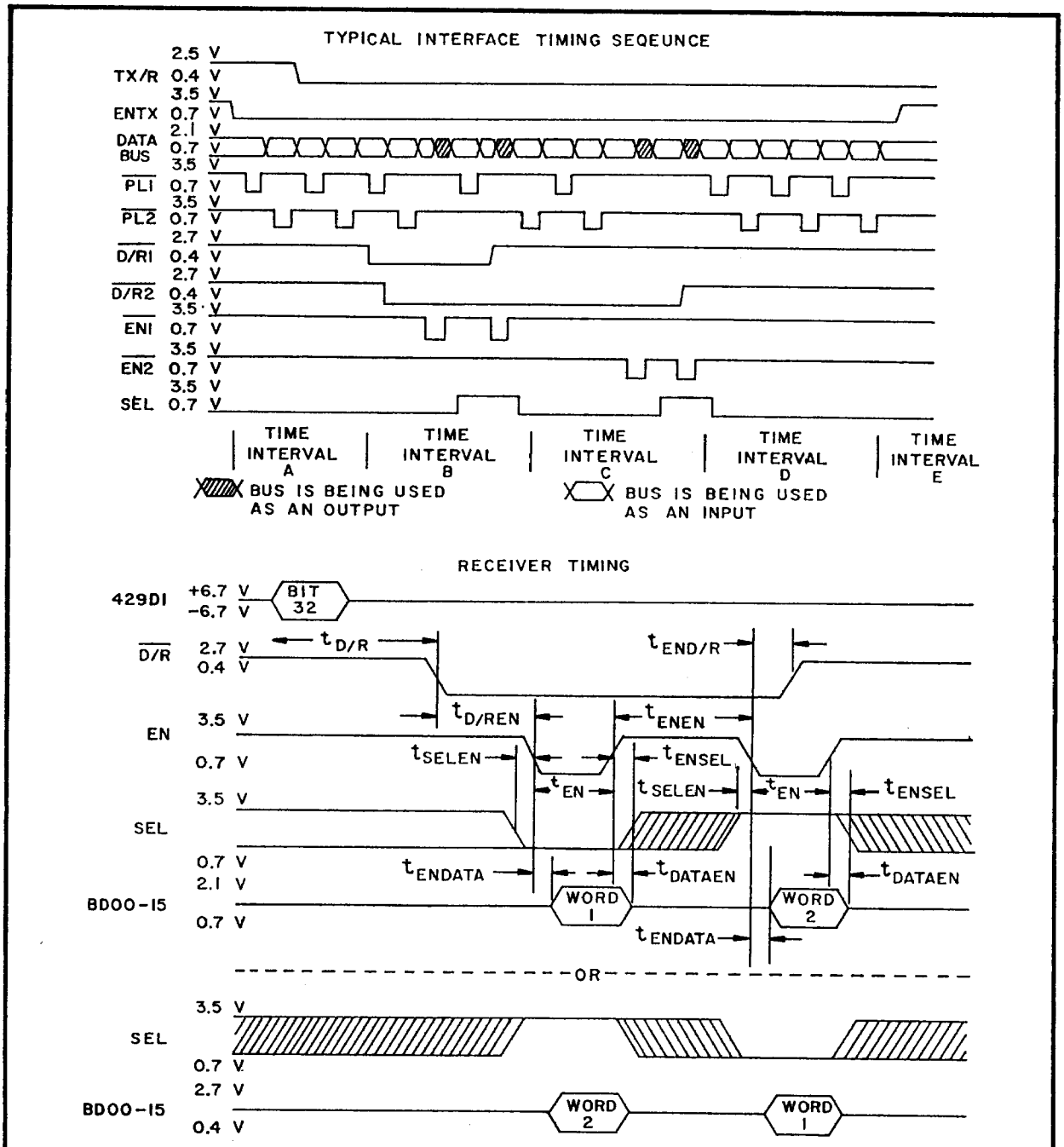


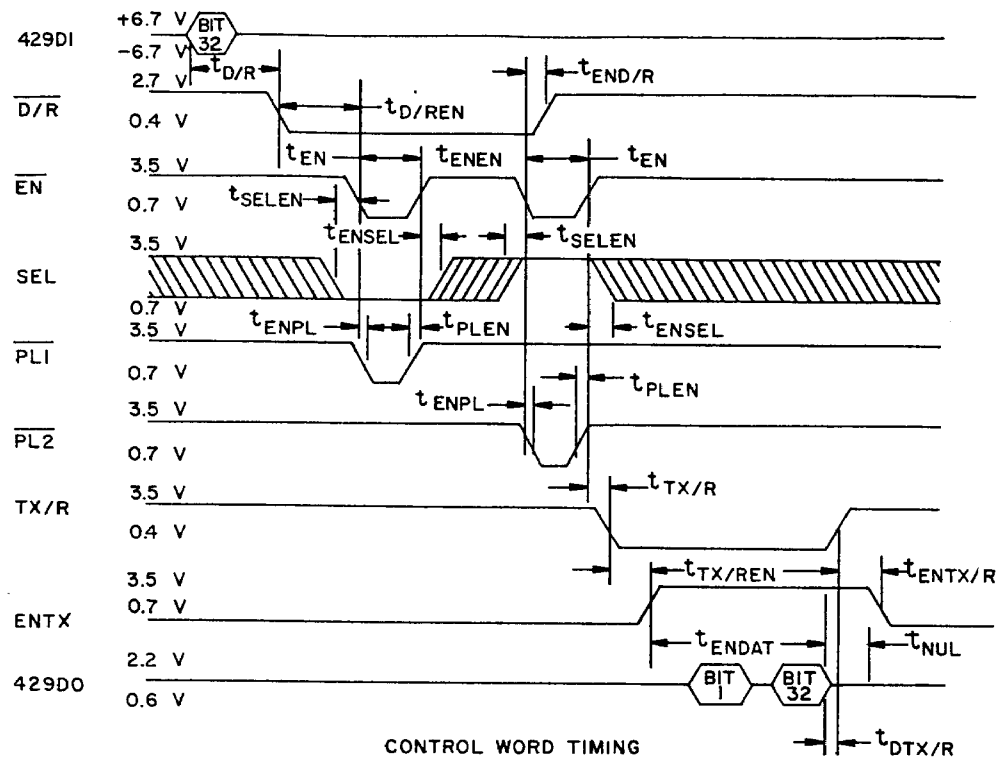
FIGURE 3. Switching waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86880
		REVISION LEVEL A	SHEET 10

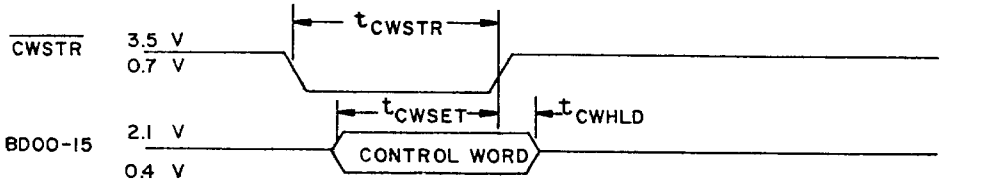
DESC FORM 193A
SEP 87

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

REPEATER OPERATION TIMING



CONTROL WORD TIMING



TRANSMITTER OUTPUT TIMING

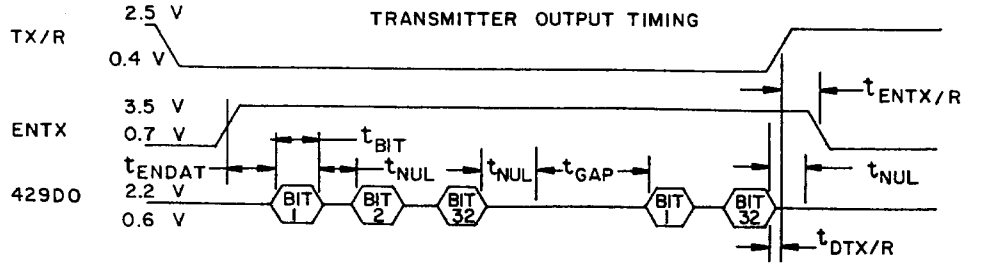
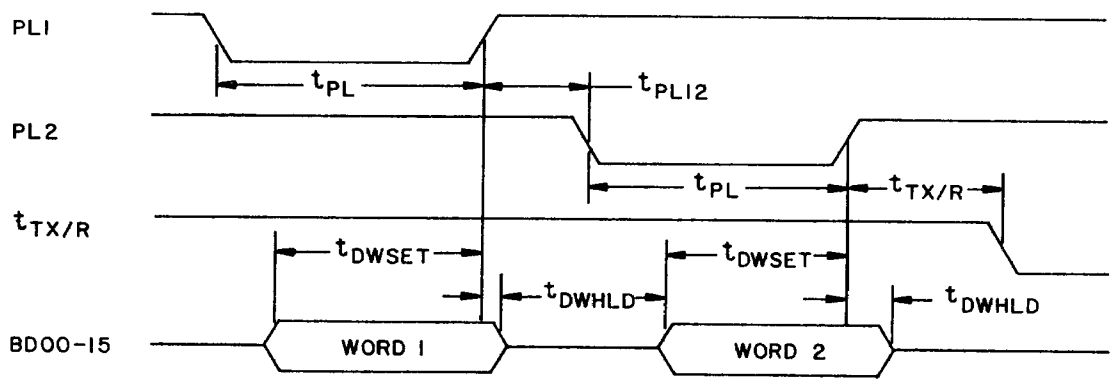


FIGURE 3. Switching waveforms - Continued.



TRANSMITTER FIFO WRITE TIMING

FIGURE 3. Switching waveforms - Continued.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices, all input and output terminals tested, and no failures.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,9
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordianted with the users of record for the individual documents. This coordiantion will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronic Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8688001QX	34371	HS1-3282/883
5962-8688001XX	34371	HS4-3282/883
5962-8688002QX	44270	HI-8282CM
5962-8688002XX	44270	HI-8282SM

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32901
44270	Holt, Incorporated 9351 Jeronimo Road Irvine, CA 92718