REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 03, 04, 05, and 06. Added electrical test limits for device types 03, 04, 05, and 06 to table I. Added vendor CAGE code 34335. Editorial changes throughout.	90-05-09	William K. Heckman
B	Added device types 07, 08, 09, and 10. Added electrical parameters testing to table I for device 07, 08, 09, and 10. Added a new package for device 07. Editorial changes throughout.	92-03-25	

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	B																			
SHEET	35																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
89-02-06

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, SERIAL, COMMUNICATION CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88689
A	67268	

SHEET 1 OF 35

DESC FORM 193
JUL 91

5962-E293

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying number (PIN). The complete PIN shall be as shown in the following example:

5962-88689	01	Q	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z85C3006	6.0 MHz	Serial communication controller
02	Z85C3008	8.0 MHz	Serial communication controller 2/
03	AM85C30-10	10.0 MHz	Serial communication controller with SDLC enhancements 1/
04	AM85C30-12	12.0 MHz	Serial communication controller with SDLC enhancements
05	AM85C30-16	16.0 MHz	Serial communication controller with SDLC enhancements 1/
06	AM85C30-08	8.0 MHz	Serial communication controller with SDLC enhancements 1/
07	Z85C3010	10.0 MHz	Serial communication controller 3/
08	Z8523010	10.0 MHz	Serial communication controller with SDLC enhancements 1/
09	Z8523016	16.0 MHz	Serial communication controller with SDLC enhancements 1/
10	Z8523008	8.0 MHz	Serial communication controller with SDLC enhancements 1/

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	CJ-1 (44-lead, .658" x .658" x .190"), square "J" lead chip carrier
Y	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to ground)	-0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground)	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation	0.5 W
Lead temperature (soldering, 10 seconds)	+270°C
Maximum operating junction temperature (T_J)	+180°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.2 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Frequency of operation:	
Device type 01	0.5 MHz to 6.0 MHz
Device types 02, 06, 10	0.5 MHz to 8.0 MHz
Device types 03, 07, 08	0.5 MHz to 10 MHz
Device types 04	0.5 MHz to 12.5 MHz
Device types 05, 09	0.5 MHz to 16.4 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1/ Device types 03, 05, 06 and 08, 09, 10 are not functionally identical.

2/ Device type 02 is not functionally identical with 06 or 10.

3/ Device type 07 is not functionally identical with 03 or 08.

Clock rise time and fall times:

Device type 09	5 ns maximum
Device type 05	8 ns maximum
Device types 01, 02, 03, 04, 06, 07, 08, 10	10 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing diagrams and test circuits. The timing diagrams and test circuits shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Units
					Min	Max	
High input voltage	V_{IH}		1, 2, 3	All	2.2	V_{CC}+0.3 2/	V
Low input voltage	V_{IL}				-0.3 2/	0.8	
Logic low output voltage	V_{OL}	I_{OL} = 2.0 mA V_{CC} = 4.5 V				0.5	
Logic high output voltage	V_{OH1}	I_{OH} = -16 mA V_{CC} = 4.5 V			2.4		
	V_{OH2}	I_{OH} = -250 µA V_{CC} = 4.5 V			V_{CC}-0.8		
Power supply current	I_{CC}	V_{IH} = 4.8 V V_{IL} = 0.2 V V_{CC} = 5.0 V Oscillator off		01, 02, 06		30	mA
				03, 07, 08		18	
				04, 05, 09		22	
				10		15	
Output leakage current low	I_{LOL}	V_{OUT} = 0.4 V V_{CC} = 5.5 V		All	-10		µA
Output leakage current high	I_{LOH}	V_{OUT} = 2.4 V V_{CC} = 5.5 V				+10	
Input low current	I_{IL}	V_{IN} = 0.4 V V_{CC} = 5.5 V			-10		
Input high current	I_{IH}	V_{IN} = 2.4 V V_{CC} = 5.5 V				+10	
Input capacitance	C_{IN}	fc = 1.0 MHz See 4.3.1c	4			10	pF
Output capacitance	C_{OUT}					15	
Bidirectional capacitance	$C_{I/O}$					20	
Functional test		See 4.3.1d V_{CC} = 4.5 V, 5.5 V	7, 8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
Maximum frequency	f_{MAX}	See figure 3 V_{CC} = 4.5 V	9, 10, 11		05, 09	16.0		MHz
					04	12.0		
					03, 07, 08	10.0		
					02, 06, 10	8.0		
					01	6.0		
PCLK low width	t_{wPCl}	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V		1	01	70	1000	ns
					02, 06, 10	50	1000	
					03, 07, 08	40	1000	
					04	34	1000	
					05, 09	26	1000	
PCLK high width	t_{wPCH}			2	01	70	1000	ns
					02, 06, 10	50	1000	
					03, 07, 08	40	1000	
					04	34	1000	
					05, 09	26	1000	
PCLK fall time 2/ 18/	t_{fPC}			3	01, 02, 03 04, 06, 07 08, 10		10	
					05		8	
					09		5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
PCLK rise time 2/ 18/	t_{rPC}	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	4	01, 02, 03 04, 06, 07 08, 10		10	ns
					05		8	
					09		5	
PCLK cycle time	t_{cPC}			5	01	165	2000	ns
					02, 06, 10	125	2000	
					03, 07, 08	100	2000	
					04	80	2000	
					05, 09	61	2000	
Address to $\overline{WR}$ ↓ set up time	$t_{sA(WR)}$			6	01	80		ns
					02, 06, 10	70		
					03, 07, 08	50		
					04	45		
					05, 09	35		
Address to $\overline{WR}$ ↑ hold time	$t_{hA(WR)}$			7	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
Address to $\overline{RD}$ ↓ setup time	$t_{sA(RD)}$	See figure 3, read and write interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	8	01	80		ns
					02, 06, 10	70		
					03, 07, 08	50		
					04	45		
					05, 09	35		
Address to $\overline{RD}$ ↑ hold time	$t_{hA(RD)}$			9	All	0		ns
$\overline{INTACK}$ to PCLK ↑ setup time 3/	$t_{sIA(PC)}$			10	01, 02, 03 06, 07, 08 10	20		ns
					04, 05, 09	15		
$\overline{INTACK}$ to $\overline{WR}$ ↓ setup time 4/	$t_{sIAi(WR)}$			11	01	160		ns
					02, 06, 10	145		
					07	130		
					03, 08	120		
					04	95		
					05, 09	70		
$\overline{INTACK}$ to $\overline{WR}$ ↑ hold time	$t_{hIA(WR)}$			12	All	0		ns
$\overline{INTACK}$ to $\overline{RD}$ ↓ setup time 4/	$t_{sIAi(RD)}$			13	01	160		ns
					02, 03, 06 07, 08, 10	145		
					04	95		
					05, 09	70		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits Min	Limits Max	Units
$\overline{INTACK}$ to $\overline{RD}$ ↑ hold time 3/	$t_{sIAi(RD)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	14	All	0		ns
$\overline{INTACK}$ to PCLK ↑ hold time	$t_{hIA(PC)}$			15	01	100		ns
					02, 06, 10	40		
					03, 07, 08	30		
					04	20		
					05, 09	15		
$\overline{CE}$ low to $\overline{WR}$ ↓ setup time	$t_{sCEl(WR)}$			16	All	0		ns
$\overline{CE}$ to $\overline{WR}$ ↑ hold time	$t_{hCE(WR)}$			17	All	0		ns
$\overline{CE}$ high to $\overline{WR}$ ↓ setup time	$t_{sCEh(WR)}$			18	01	70		ns
					02, 06, 10	60		
					03, 07, 08	50		
					04	40		
					05, 09	30		
$\overline{CE}$ low to $\overline{RD}$ ↓ setup time 4/	$t_{sCEl(RD)}$			19	All	0		ns
$\overline{CE}$ to $\overline{RD}$ ↑ hold time 4/	$t_{hCE(RD)}$			20	All	0		ns
$\overline{CE}$ high to $\overline{RD}$ ↓ setup time 4/	$t_{sCEh(RD)}$			21	01	70		ns
					02, 06, 10	60		
					03, 07, 08	50		
					04	40		
					05, 09	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits Min	Limits Max	Units
$\overline{RD}$ low width 4/	t_{wRDl}	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	22	01	200		ns
					02, 06, 10	150		
					03, 07, 08	125		
					04	90		
					05, 09	75		
$\overline{RD}$ ↓ to read data active delay 2/	$t_{dRD(DRA)}$			23	All	0		ns
$\overline{RD}$ ↑ to read data not valid delay 2/	$t_{dRDr(DR)}$			24	All	0		ns
$\overline{RD}$ ↓ to read data valid delay	$t_{dRDf(DR)}$			25	01		180	ns
					02, 06, 10		140	
					03, 07, 08		125	
					04		90	
					05, 09		70	
$\overline{RD}$ ↑ to read data float delay 2/ 5/	$t_{dRD(DRZ)}$			26	01		45	
					02, 06, 10		40	
					03, 07, 08		35	
					09		30	
					04		25	
					05		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
Address required valid to read data valid delay	$t_{dA(DR)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10%, V_{CC} = 4.55 V	9, 10, 11	27	01		280	ns
					02, 06, 10		220	
					07		180	
					03, 08		160	
					04		120	
					05, 09		100	
$\overline{WR}$ low width	t_{wWRl}			28	01	200		ns
					02, 06, 10	150		
					03, 07, 08	125		
					04	90		
					05, 09	75		
$\overline{WR}$ ↓ to write data valid	$t_{sDW(WR)}$			29	03, 06, 07		35	ns
					04		25	
					05, 08, 09 10		20	
					01, 02		0	
WRITE data to $\overline{WR}$ hold time	$t_{hDW(WR)}$			30	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{WR}$ ↓ to wait valid delay 6/	$t_{dWR(W)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ± 10%, V_{CC} = 4.5 V	9, 10, 11	31	01		200	ns
					02, 06, 10		170	
					07		160	
					03, 08		100	
					04		70	
					05, 09		50	
$\overline{RD}$ ↓ to wait valid delay 6/	$t_{dRD(W)}$			32	01		200	ns
					02, 06, 10		170	
					07		160	
					03, 08		100	
					04		70	
					05, 09		50	
$\overline{WR}$ ↓ to $\overline{W}/\overline{REQ}$ not valid delay	$t_{dWRf(REQ)}$			33	01		200	ns
					02, 06, 10		170	
					07		160	
					03, 08		120	
					04		100	
					05, 09		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits Min	Limits Max	Units
$\overline{RD}$ ↓ to W/$\overline{REQ}$ not valid delay	$t_{dRDf(REQ)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	34	01		200	ns
					02, 06, 10		170	
					07		160	
					03, 08		120	
					04		100	
					05, 09		70	
$\overline{WR}$ ↓ to $\overline{DTR}$/$\overline{REQ}$ not valid delay	$t_{dWRr(REQ)}$			35	All		4.0 t_{cPC}	ns
$\overline{WR}$ ↓ to $\overline{DTR}$/$\overline{REQ}$ not valid delay	$t_{dWRr(EREQ)}$ 17/			35	03, 06, 08 10		120	ns
					04		100	
					05, 09		70	
$\overline{RD}$ ↑ to $\overline{DTR}$/$\overline{REQ}$ not valid delay	$t_{dRDr(REQ)}$			36	All		4.0 t_{cPC}	ns
PCLK ↓ to $\overline{INT}$ valid delay 6/	$t_{dPC(INT)}$			37	01, 02, 06 07, 10		500	ns
					03		400	
					04		350	
					08		320	
					05, 09		175	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{INTACK}$ to $\overline{RD}$ ↓ (acknowledge) delay 7/	$t_{dIAi(RD)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ± 10% V_{CC} = 4.5 V	9, 10, 11	38	01	200		ns
					02, 06, 10	150		
					03, 07, 08	125		
					04	95		
					05, 09	50		
$\overline{RD}$ (acknowledge) width	t_{WRDA}			39	01	200		ns
					02, 06, 10	150		
					03, 07, 08	125		
					04	95		
					05, 09	75		
$\overline{RD}$ ↓ (acknowledge) to read data valid delay	$t_{dRDA(DR)}$			40	01		180	ns
					02, 03, 06 07, 08, 10		140	
					04		90	
					05, 09		70	

See footnotes at end of table.

I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
IEI to $\overline{RD}$ ↓ (acknowledge) setup time	$t_{sIEI(RDA)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	41	01	100		ns
					02, 03, 06 07, 08, 10	95		
					04	65		
					05, 09	50		
IEI to $\overline{RD}$ ↑ (acknowledge) hold time	$t_{hIEI(RDA)}$			42	All	0		ns
IEI to IEO delay time	$t_{dIEI(IEO)}$			43	01		100	ns
					02, 03, 06 07, 08, 10		95	
					04		65	
					05, 09		45	
PCLK ↑ to IEO delay	$t_{dPC(IEO)}$			44	01		250	ns
					02, 03, 06 07		200	
					08		175	
					04		130	
					05, 09		80	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits Min	Limits Max	Units
$\overline{RD}$ ↓ to $\overline{INT}$ inactive delay 6/	$t_{dRA(INT)}$	See figure 3, read and write, interrupt, reset, and cycle timings. C_L = 50 pF ±10% V_{CC} = 4.5 V	9, 10, 11	45	01, 02, 06 07		500	ns
					03, 10		450	
					08		320	
					04		260	
					05, 09		200	
$\overline{RD}$ ↑ to $\overline{WR}$ ↓ delay for no reset 2/	$t_{dRD(WRQ)}$			46	01, 02, 03 06, 07, 08 10	15		ns
					04, 05, 09	10		
$\overline{WR}$ ↑ to $\overline{RD}$ ↓ delay for no reset 2/	$t_{dWRQ(RD)}$			47	01	30		ns
					02, 03, 06 07, 08, 10	15		
					04, 05, 09	10		
$\overline{WR}$ and $\overline{RD}$ coincident low for reset 2/	t_{WRES}			48	01	200		ns
					02, 03, 06 10	150		
					07, 08	100		
					04	85		
					05, 09	75		
Valid access recovery time 2/ 8/	t_{rC}			49	01, 02, 06 07, 08, 09 10	4.0 t_{cPC}		ns
					03, 04, 05	3.5 t_{cPC}		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
PCLK ↓ to $\overline{W/REQ}$ valid delay	$t_{dPC(REQ)}$	See figure 3, general timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	1	01, 02, 06, 07, 10		250	ns
					03, 08		150	
					04		120	
					05, 09		80	
PCLK ↓ to wait inactive delay	$t_{dPC(W)}$			2	01, 02, 06, 07, 10		350	ns
					03, 08		250	
					04		220	
					05, 09		180	
$\overline{RxC}$ ↑ to PCLK ↑ setup time (PCLK ÷ 4 case only) 9/ 10/	$t_{sRXC(PC)}$			3	01	70	t_{wPCl}	ns
					02, 06	60	t_{wPCl}	
					07	40	t_{wPCl}	
					03, 04, 05 08, 09, 10	0		
RxD to $\overline{RxC}$ ↑ setup time 9/ (X1 mode)	$t_{sRXD(RXCr)}$			4	All	0		ns
RxD to $\overline{RxC}$ ↑ hold time 9/ (X1 mode)	$t_{hRXD(RXCf)}$			5	01, 02, 06 07, 10	150		ns
					03, 08	125		
					04	100		
					05, 09	50		
RxD to $\overline{RxC}$ ↓ setup time (X1 mode) 9/ 11/	$t_{sRXD(RXCf)}$			6	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
RxD to $\overline{RxC}$ ↓ hold time (X1 mode) 9/ 11/	$t_{hRXD(RXCf)}$	See figure 3, general timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	7	01, 02, 06, 07, 10	150		ns
					03, 08	125		
					04	100		
					05, 09	50		
$\overline{SYNC}$ to $\overline{RxC}$ ↑ setup time 9/	$t_{sSY(RXC)}$			8	01, 02, 06, 07, 10	-200		ns
					03, 08	-150		
					04	-125		
					05, 09	-100		
$\overline{SYNC}$ to $\overline{RxC}$ ↑ hold time 9/	$t_{hSY(RXC)}$			9	All	5.0 t_{cPC}		ns
$\overline{TxC}$ ↓ to PCLK ↑ setup time 10/ 12/	$t_{sTXC(PC)}$			10	All	0		ns
$\overline{TxC}$ ↓ to TxD delay 12/ (X1 mode)	$t_{dTXCf(TXD)}$			11	01		230	ns
					02, 06		200	
					10		190	
					03, 07, 08		150	
					04		130	
					05, 09		80	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{TxC}$ ↑ to TxD delay 11/ 12/ (X1 mode)	$t_{dTXCr(TXD)}$	See figure 3, general timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	12	01		230	ns
					02, 06		200	
					10		190	
					03, 07, 08		150	
					04		130	
					05, 09		80	
TxD to $\overline{TRxC}$ delay (send clock echo)	$t_{dTXD(TRX)}$			13	01, 02, 06 07, 10		200	ns
					03, 08		140	
					04		120	
					05, 09		80	
$\overline{RTxC}$ high width 13/	t_{wRTxh}			14	01	180		ns
					02, 06, 07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		
$\overline{RTxC}$ low width 13/	t_{wRTx1}			15	01	180		ns
					02, 06, 07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{RTxC}$ cycle time 13/ 14/ (RxD, TxD)	t_{cRTX}	See figure 3, general timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	16	01	640		ns
					02, 06	500		
					10	472		
					03, 07, 08	400		
					04	320		
					05, 09	244		
Crystal oscillator period 3/ 15/	t_{cRTXX}			17	01	165	1000	ns
					02, 06, 10	125	1000	
					03, 07, 08	100	1000	
					04	80	1000	
					05, 09	62	1000	
$\overline{TRxC}$ high width 13/	t_{wTRXh}			18	01	180		ns
					02, 06, 07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{TRxC}$ low width 13/	t_{WTRX1}	See figure 3, general timings. C_L = 50 pF ±10%, V_{CC} = 4.5 V	9, 10, 11	19	01	180		ns
					02, 06, 07	150		
					10	130		
					03, 08	120		
					04	100		
					05, 09	80		
$\overline{TRxC}$ cycle time 13/ 14/	t_{cTRX}			20	01	640		ns
					02, 06	500		
					10	472		
					03, 07, 08	400		
					04	320		
					05, 09	244		
$\overline{DCD}$ to $\overline{CTS}$ pulse width	t_{WEXT}			21	01, 02, 06 07, 10	200		ns
					03, 08	120		
					04	100		
					05, 09	70		
$\overline{SYNC}$ pulse width	t_{WSY}			22	01, 02, 06 07, 10	200		ns
					03, 08	120		
					04	100		
					05, 09	70		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.00 V ±10% 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits		Units
						Min	Max	
$\overline{RxC}$ ↑ to $\overline{W/REQ}$ valid delay 2/ 9/ 16/	$t_{dRXC(REQ)}$	See figure 3, system timing. C_L = 50 pF ±10%, V_{CC} =4.5 V	9, 10, 11	1	08, 09, 10	13	17	t_{cPC}
					01, 02, 03, 04, 05, 06, 07	8	12	
$\overline{RxC}$ ↑ to wait inactive delay 2/ 6/ 9/ 16/	$t_{dRXC(W)}$			2	08, 09, 10	13	17	t_{cPC}
					01, 02, 03, 04, 05, 06, 07	8	14	
$\overline{RxC}$ ↑ to $\overline{SYNC}$ valid delay	$t_{dRXC(SY)}$			3	08, 09, 10	9	12	t_{cPC}
					01, 02, 03 04, 05, 06, 07	4	7	
$\overline{RxC}$ ↑ to $\overline{INT}$ valid delay 2/ 6/ 9/ 16/	$t_{dRXC(INT)}$			4	08, 09, 10	15	21	t_{cPC}
					01, 02, 03 04, 05, 06, 07	10	16	
$\overline{TxC}$ ↑ to $\overline{W/REQ}$ valid delay 2/ 12/ 16/	$t_{dTXC(REQ)}$			5	08, 09, 10	8	11	t_{cPC}
					01, 02, 03 04, 05, 06, 07	5	8	
$\overline{TxC}$ ↓ to wait inactive delay 2/ 6/ 12/ 16/	$t_{dTXC(W)}$			6	08, 09, 10	8	14	t_{cPC}
					01, 02, 03 04, 05, 06, 07	5	11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.00\ V \pm 10\%$ 1/ unless otherwise specified	Group A subgroups	Ref. no.	Device types	Limits Min	Limits Max	Unit
$\overline{TxC}$ ↓ to $\overline{DTR}/\overline{REQ}$ valid delay 2/ 12/ 16/	$t_{dTXC(DRQ)}$	See figure 3, system timing. $C_L = 50\ pF \pm 10\%$, $V_{CC} = 4.5\ V$	9, 10, 11	7	08, 09, 10	7	10	t_{cPC}
					01, 02, 03 04, 05, 06 07	4	7	
$\overline{TxC}$ ↓ to $\overline{DTR}/\overline{REQ}$ valid delay 2/ 12/ 16/ 17/	$t_{dTXC(EDRQ)}$			7a	08, 09, 10	9	12	t_{cPC}
					03, 04, 05 06	5	8	
$\overline{TxC}$ ↓ to $\overline{INT}$ valid delay 2/ 6/ 12/ 16/	$t_{dTXC(INT)}$			8	08, 09, 10	9	13	t_{cPC}
					01, 02, 03 04, 05, 06 07	6	10	
$\overline{SYNC}$ transition to $\overline{INT}$ valid delay 2/ 6/ 16/	$t_{dSY(INT)}$			9	All	2	6	t_{cPC}
$\overline{DCD}$ or $\overline{CTS}$ transition to $\overline{INT}$ valid delay 2/ 6/ 16/	$t_{dEXT(INT)}$			10	10	3	8	t_{cPC}
					01, 02, 03 04, 05, 06 07, 08, 09	2	6	

1/ All test must be performed under the worst case condition.
2/ Guaranteed to the limit specified herein if not tested.
3/ Tested in interrupt acknowledge cycle only.
4/ Parameter does not apply to interrupt acknowledge transactions.
5/ Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.
6/ Open-drain output, measured with open-drain test load.
7/ Parameter is system dependent. For any SCC in the daisy chain, $t_{dIAi(RD)}$ must be greater than the sum of $t_{dPC(IEO)}$ for the highest priority device in the daisy chain, $t_{sIEI(RDA)}$ for the SCC, and $t_{dIEIf(IEO)}$ for each device separating them in the daisy chain.
8/ Parameter applies only between transactions involving the SCC.
9/ RxC is RTxC or TRxC, whichever is supplying the receive clock.
10/ Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
11/ Parameter applies only to FM encoding/decoding.
12/ TxC is TRxC or RTxC, whichever is supplying the transmit clock.
13/ Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
14/ The maximum receive or transmit data is one-fourth PCLK.
15/ Both RTxC and SYNC have 30 pF capacitors to ground connected to them.
16/ The value of this parameter is dependent on PCLK cycle time.
17/ Applies to versions with SDLC enhancements only.
18/ For device type 03, 04, 05, and 06, clock rise and fall times are controlled at approximately 5 ns by the tester.

All device types

Case Q

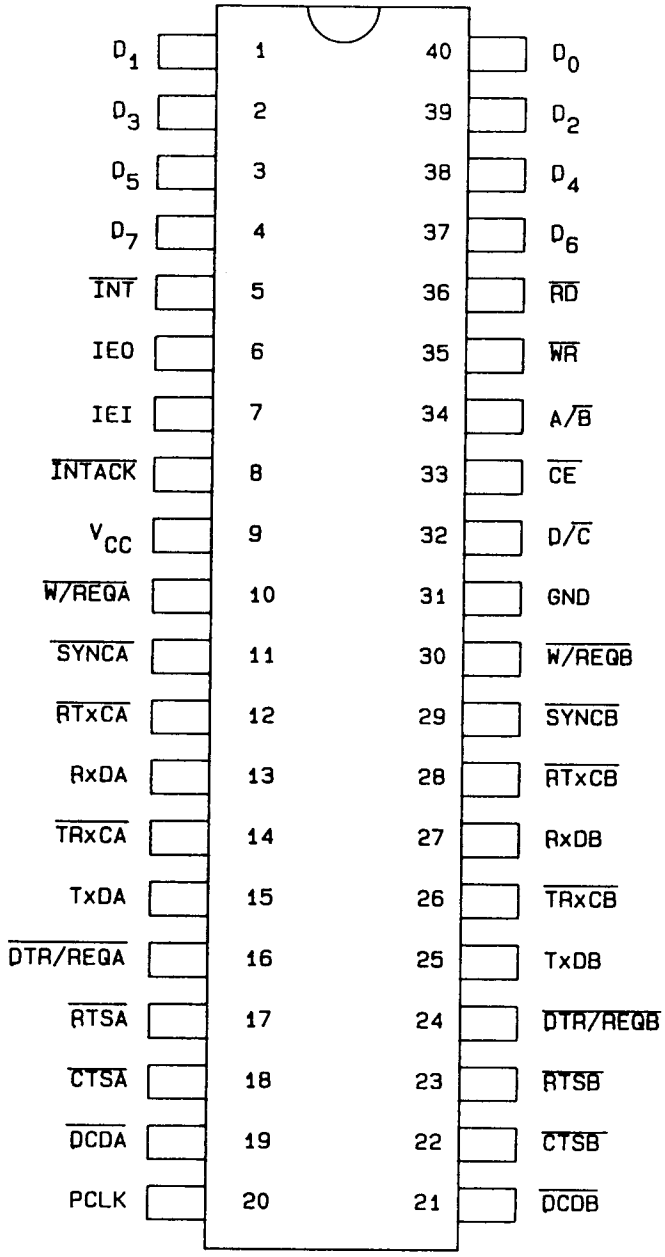
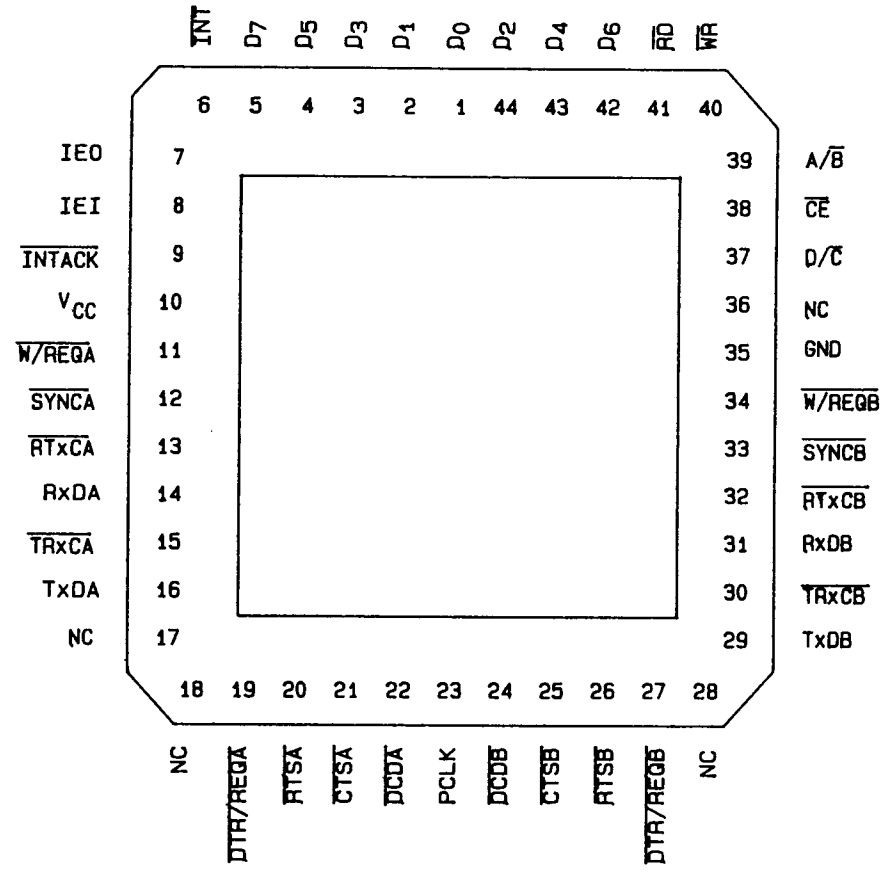


FIGURE 1. Terminal connections.

All device types

Case Y and X 1/



1/ Case X is applicable to device type 07 only.

FIGURE 1. Terminal connections. - Continued.

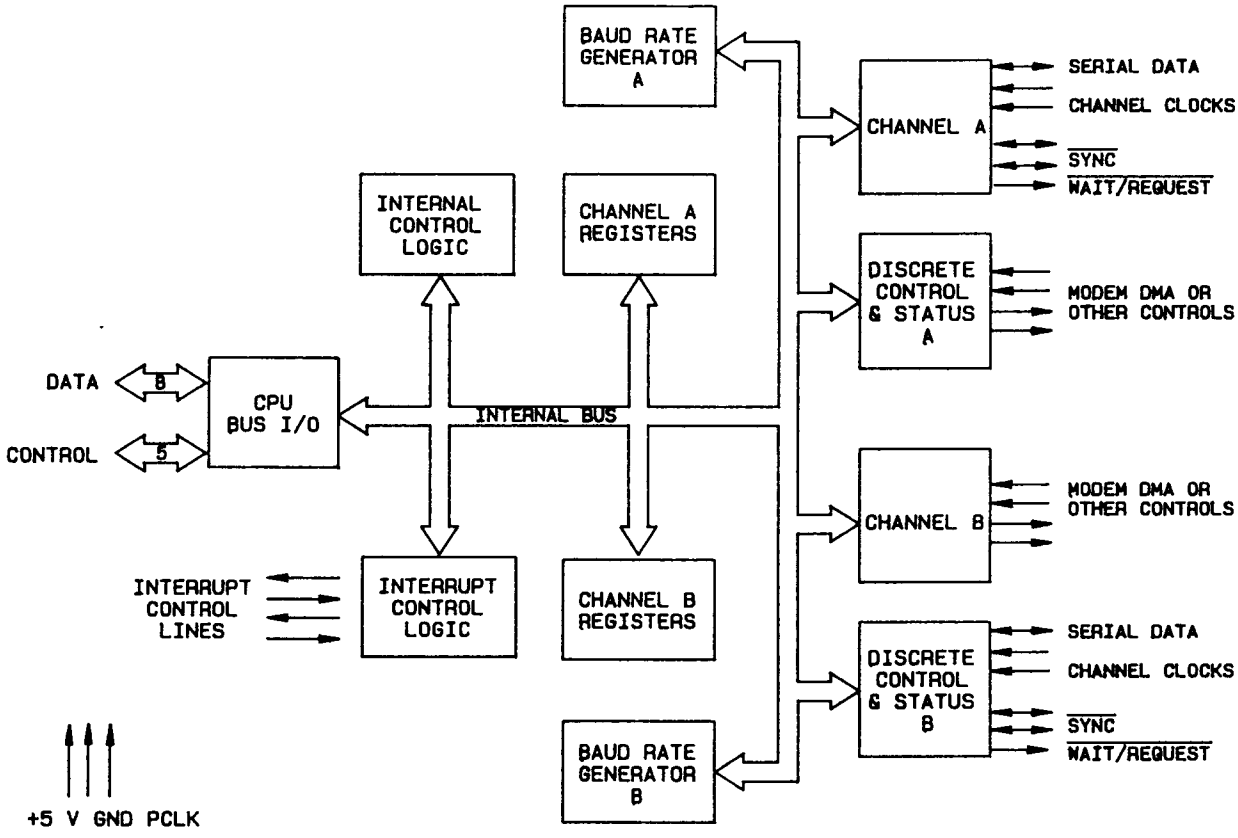


FIGURE 2. Block diagram.

All device types. (Read and Write timings.)

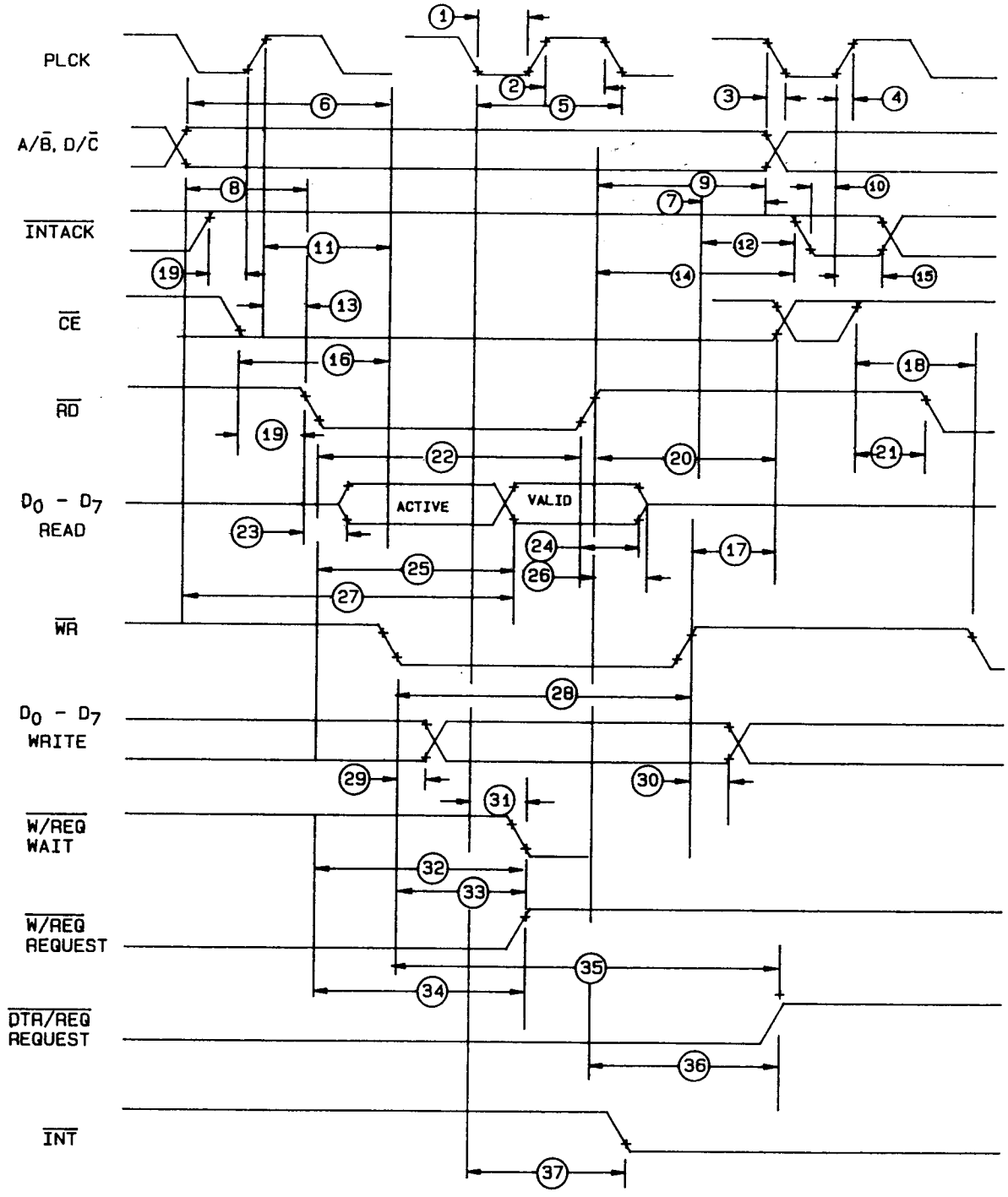
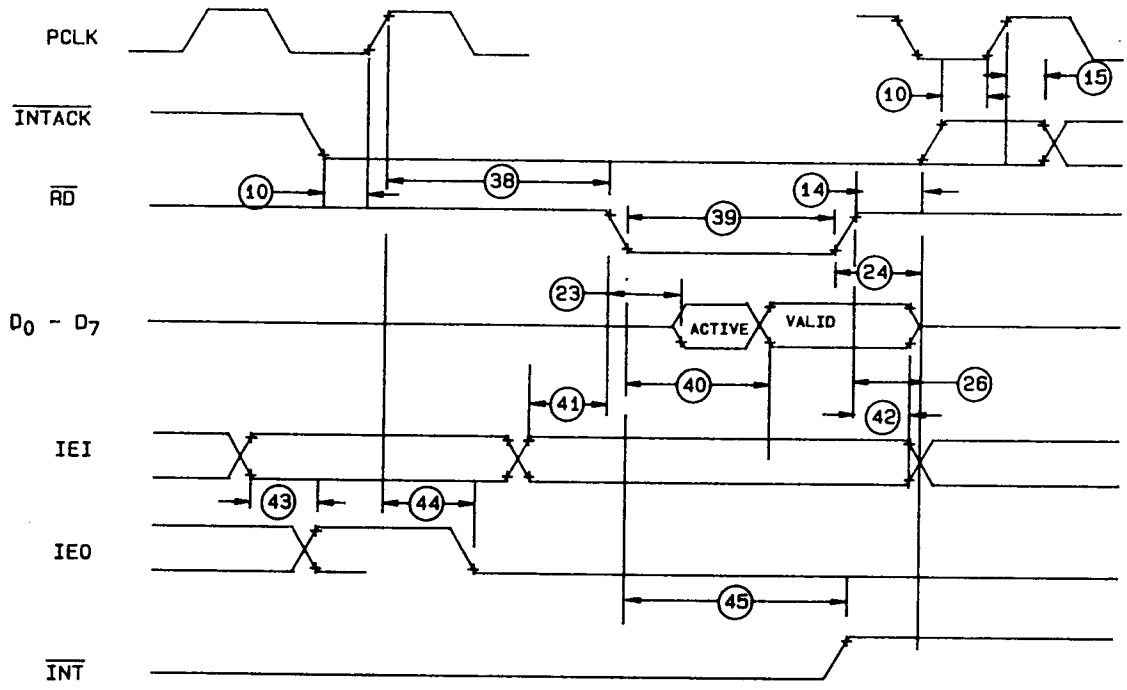


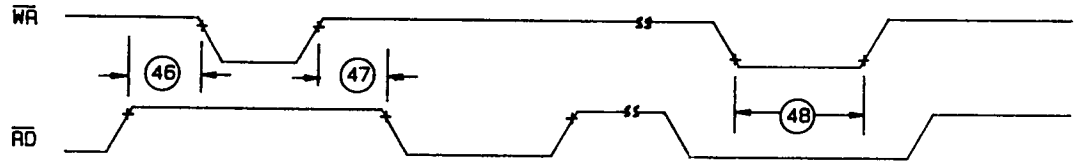
FIGURE 3. Timing diagrams and test circuits.

All device types.

Interrupt acknowledge timing



Reset timing



Circle timing

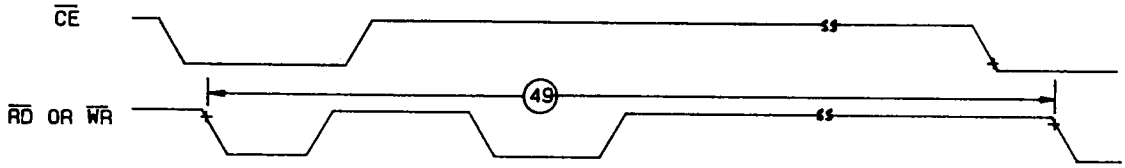


FIGURE 3. Timing diagrams and test circuits - Continued.

All device types.

General timing.

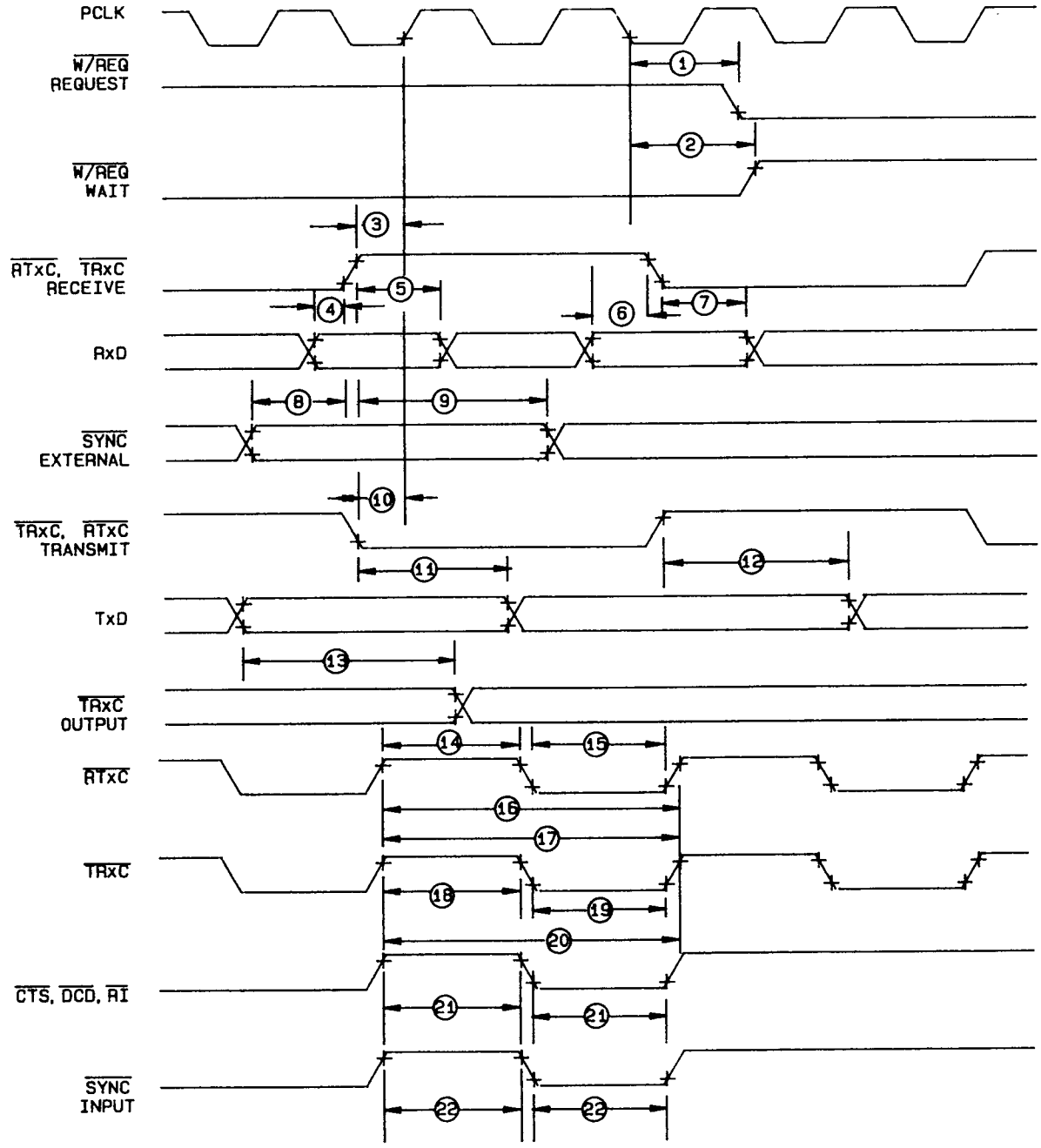


FIGURE 3. Timing diagrams and test circuits - Continued.

All device types.

System timing

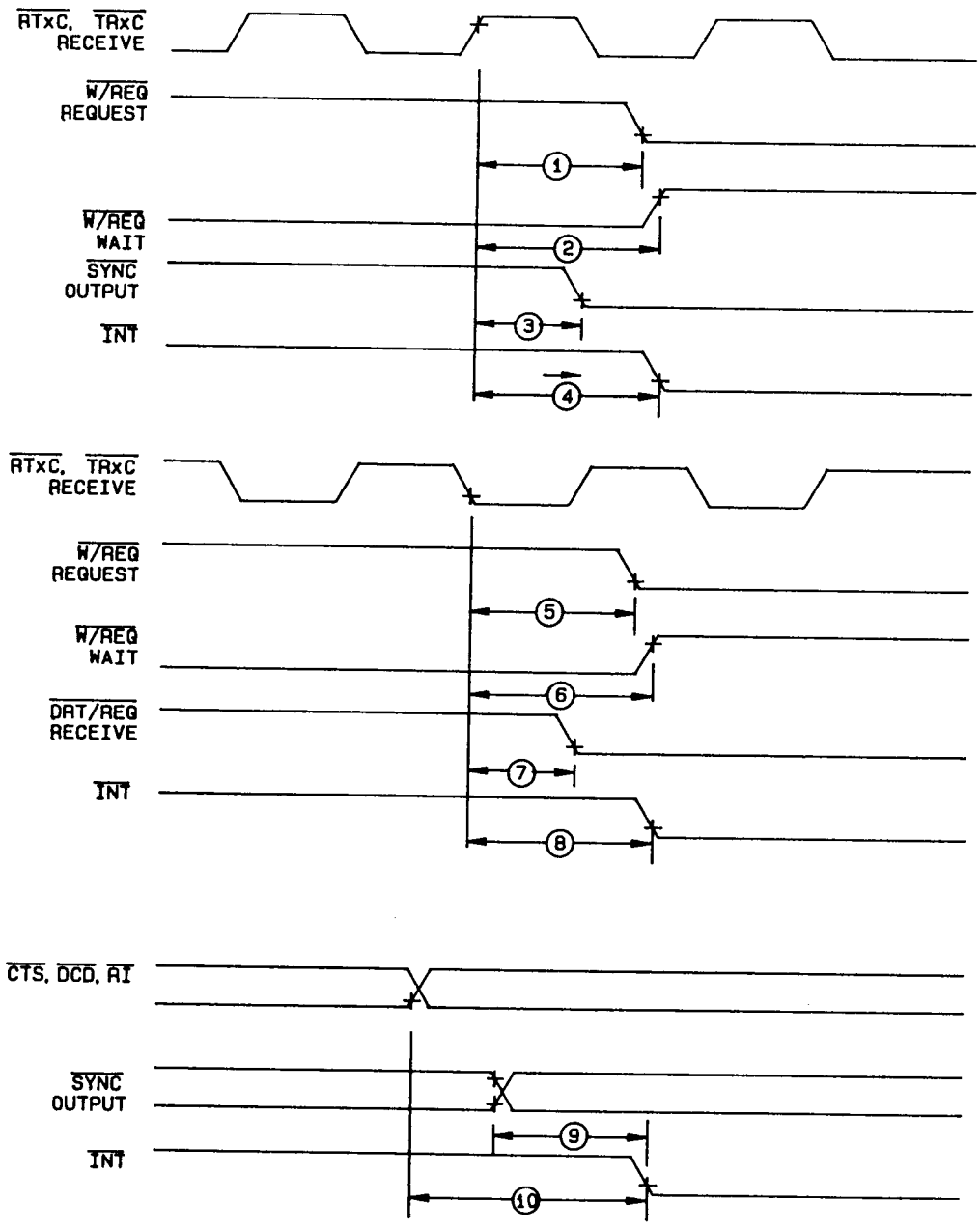
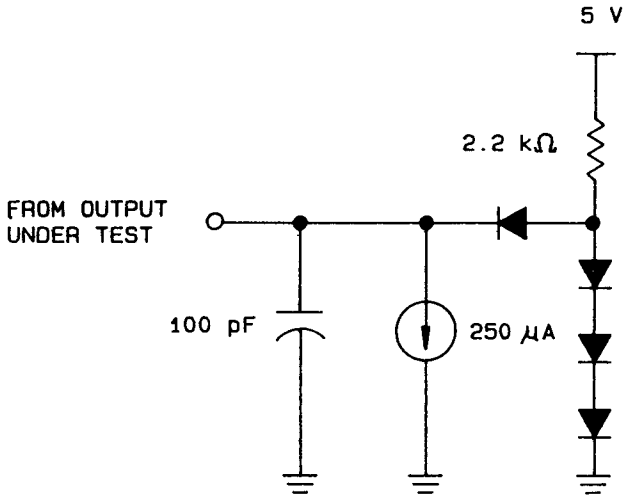


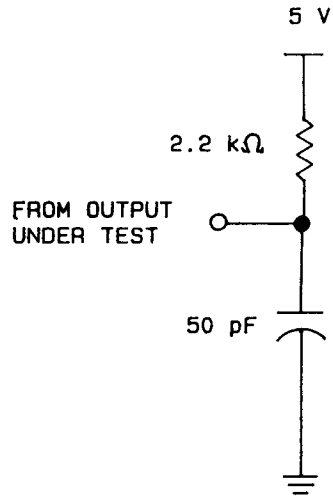
FIGURE 3. Timing diagrams and test circuits - Continued.

Switching test circuits

Standard test load



Open drain test load



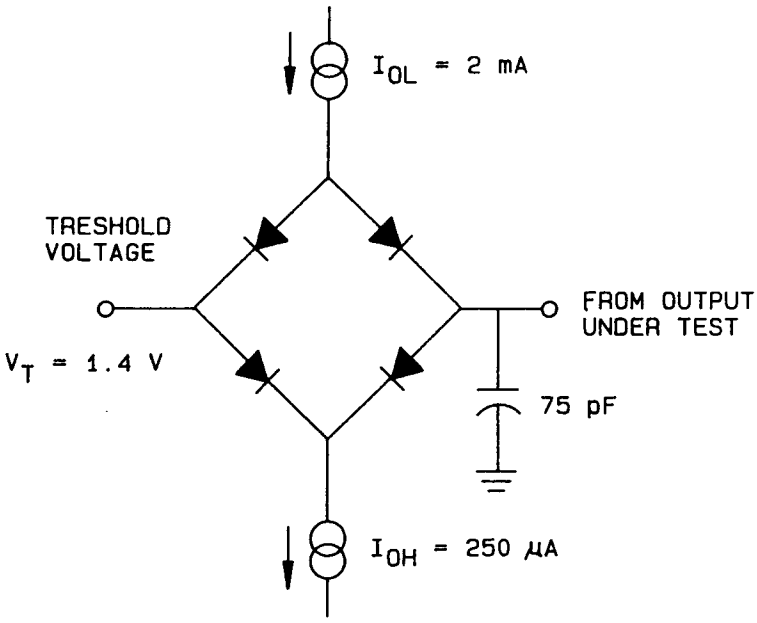
Switching test input/output waveform

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0"
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

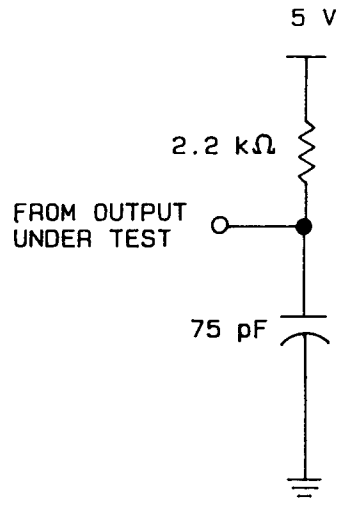
FIGURE 3. Timing diagrams and test circuits - Continued.

Switching test circuits

Standard test load



Open drain test load



Switching test input/output waveform

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0"
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 3. Timing diagrams and test circuits - Continued.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects is required.

d. Subgroups 7 and 8 functional testing, shall verify of functionality of device.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C and D end point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8525.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

3.3 Pin descriptions

A/$\overline{B}$	Channel A/channel B select (input). This signal selects the channel in which the read or write operation occurs.
$\overline{CE}$	Chip enable (input, active low). This signal selects the SCC for a read or write operation.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to send (inputs, active low). If these pins are programmed as auto enables, a low on the inputs enables the respective transmitters. If not programmed as auto enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.
D/$\overline{C}$	Data/control select (input). This signal defines the type of information transferred to or from the SCC. A high means data is transferred, a low indicates a command.
$\overline{DCDA}$, $\overline{DCDB}$	Data carrier detect (inputs, active low). These pins function as receiver enables if they are programmed for auto enables; otherwise they may be used as general- purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D_0-D_7	Data bus (bidirectional, three-state). These lines carry data and commands to and from the SCC.
$\overline{DTR/REQA}$, $\overline{DTR/REQB}$	Data terminal ready/request (outputs, active low). These outputs follow the state programmed into the DTR bit. They can also be used as general purpose outputs or as request lines for a DMA controller.
IEI	Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.
IEO	Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.
$\overline{INT}$	Interrupt request (output, open-drain, active low). This signal is activated when the SCC requests an interrupt.
$\overline{INTACK}$	Interrupt acknowledge (input, active low). This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is high). $\overline{INTACK}$ is latched by the rising edge of PCLK.
PCLK	Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.
$\overline{RD}$	Read (input, active low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the interrupt acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
RxDA, RxDB	Receive data (inputs, active high). These input signals receive serial data at standard TTL levels.

RTxCA, RTxCB	Receive/transmit clocks (inputs, active low). These pins can be programmed in several different modes of operation. In each channel, RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the digital phase-locked loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$	Request to send (outputs, active low). When the request to send (RTS) bit in write register 5 is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset in the asynchronous mode and auto enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with auto enable off, the $\overline{\text{RTS}}$ pin strictly follows the state of the RTS bit. Both pins can be used as general purpose outputs.
$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$	Synchronization (inputs or outputs, active low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the asynchronous receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the synchronous/hunt status bits in read register 0 but have no other function. In external synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{\text{SYNC}}$ must be driven low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{\text{SYNC}}$. In the internal synchronization mode (monosync and bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
TxDA, TxDB	Transmit data (outputs, active high). These output signals transmit serial data at standard TTL levels.
$\overline{\text{TRxCA}}$, $\overline{\text{TRxCB}}$	Transmit/receive clocks (inputs or outputs, active low). These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
$\overline{\text{WR}}$	Write (input, active low). When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ is interpreted as a reset.
$\overline{\text{W/REQA}}$, $\overline{\text{W/REQB}}$	Wait/request (outputs, open-drain when programmed for a wait function, driven high or low when programmed for a request function). These dual-purpose outputs may be programmed as request lines for a DMA controller or as wait lines to synchronize the CPU to the SCC data rate. The reset state is wait.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.