查询"MC34182P"供应商

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC34181,2,4
MC35181,2,4
MC33181,2,4

2

LOW POWER, HIGH SLEW RATE, WIDE BANDWIDTH, JFET INPUT OPERATIONAL AMPLIFIERS

Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4, MC35181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operate at 210 μA per amplifier and offer 4.0 MHz of gain bandwidth product and 10 V/μs slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33181/2/4, MC34181/2/4, MC35181/2/4 series of devices are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

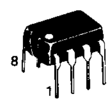
- Low Supply Current: 210 μA (Per Amplifier)
- Wide Supply Operating Range: ±1.5 V to ±18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection

ORDERING INFORMATION

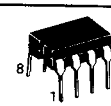
Op Amp Function	Device	Test Temperature Range	Package
Single	MC34181P MC34181D	0 to +70°C	Plastic DIP SO-8
	MC33181P MC33181D	−40 to +85°C	Plastic DIP SO-8
	MC35181U	−55 to +125°C	Ceramic DIP
Dual	MC34182P MC34182D	0 to +70°C	Plastic DIP SO-8
	MC33182P MC33182D	−40 to +85°C	Plastic DIP SO-8
	MC35182U	−55 to +125°C	Ceramic DIP
Quad	MC34184P MC34184D	0 to +70°C	Plastic DIP SO-14
	MC33184P MC33184D	−40 to +85°C	Plastic DIP SO-14
	MC35184L	−55 to +125°C	Ceramic DIP

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

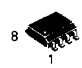
SILICON MONOLITHIC INTEGRATED CIRCUITS



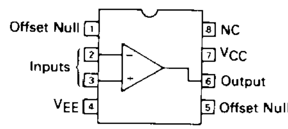
P SUFFIX
PLASTIC PACKAGE
CASE 626



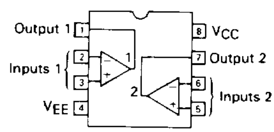
U SUFFIX
CERAMIC PACKAGE
CASE 693



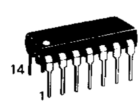
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



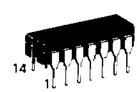
(Single, Top View)



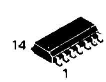
(Dual, Top View)



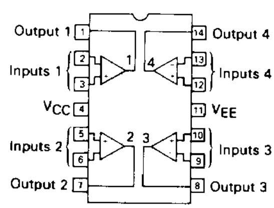
P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



(Quad, Top View)

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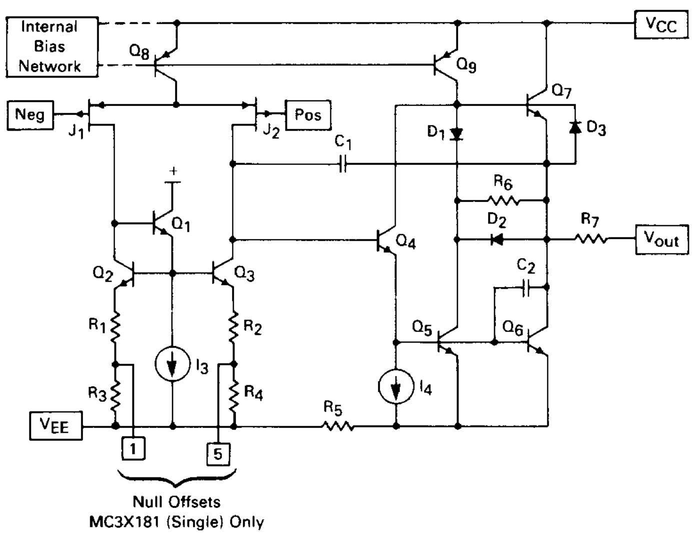
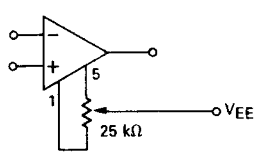
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	Volts
Input Differential Voltage Range	V_{IDR}	Note 1	Volts
Input Voltage Range	V_{IR}	Note 1	Volts
Output Short-Circuit Duration (Note 2)	t_S	Indefinite	Seconds
Operating Junction Temperature	T_J		°C
Ceramic Package		+160	
Plastic Package		+150	
Storage Temperature Range	T_{stg}		°C
Ceramic Package		−65 to +160	
Plastic Package		−60 to +150	

NOTES:
1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)





MC3X181 Input Offset Voltage Null Circuit

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0°C to +70°C (MC34181)		—	—	3.0	
T_A = −40°C to +85°C (MC33181)		—	—	3.5	
T_A = −55°C to +125°C (MC35181)		—	—	4.5	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0°C to +70°C (MC34182)		—	—	4.0	
T_A = −40°C to +85°C (MC33182)		—	—	4.5	
T_A = −55°C to +125°C (MC35182)		—	—	5.5	
Quad					
T_A = +25°C		—	4.0	10	
T_A = 0°C to +70°C (MC34184)		—	—	11	
T_A = −40°C to +85°C (MC33184)		—	—	11.5	
T_A = −55°C to +125°C (MC35184)		—	—	12.5	
Average Temperature Coefficient of V_{IO} (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	0.001	0.05	
T_A = 0°C to +70°C		—	—	1.0	
T_A = −40°C to +85°C		—	—	2.0	
T_A = −55°C to +125°C		—	—	13	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	0.003	0.1	
T_A = 0°C to +70°C		—	—	2.0	
T_A = −40°C to +85°C		—	—	4.0	
T_A = −55°C to +125°C		—	—	25	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} + 4.0 V) to (V_{CC} − 2.0 V)			V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing (V_{ID} = 1.0 V, R_L = 10 kΩ)					V
T_A = +25°C	V_O+	+13.5	+14	—	
	V_O-	—	−14	−13.5	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, V_O = 0 V)	I_D				μA
Single					
T_A = +25°C		—	210	250	
T_A = T_{low} to T_{high}		—	—	250	
Dual					
T_A = +25°C		—	420	500	
T_A = T_{low} to T_{high}		—	—	500	
Quad					
T_A = +25°C		—	840	1000	
T_A = T_{low} to T_{high}		—	—	1000	

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF)	SR				V/μs
A_V = +1.0		7.0	10	—	
A_V = −1.0		—	10	—	
Settling Time (A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V Step)	t_s				μs
To Within 0.10%		—	1.1	—	
To Within 0.01%		—	1.5	—	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	4.0	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 10 kΩ, V_O = 20 V_{p-p}, THD = 5%)	BW_P	—	200	—	kHz
Phase Margin (−10 V < V_O < +10 V)	$Ø_m$				Degrees
R_L = 10 kΩ		—	67	—	
R_L = 10 kΩ, C_L = 100 pF		—	34	—	
Gain Margin (−10 V < V_O < +10 V)	A_m				dB
R_L = 10 kΩ		—	6.7	—	
R_L = 10 kΩ, C_L = 100 pF		—	3.4	—	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	38	—	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.01	—	pA/√Hz
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = 10, R_L = 10 kΩ, 2 V_{p-p} < V_O < 20 V_{p-p}, f = 10 kHz	THD	—	0.04	—	%
Channel Separation (R_L = 10 kΩ, −10 V < V_O < +10 V, 0 Hz < f < 10 kHz)	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	$\lvert Z_O \rvert$	—	200	—	Ω

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

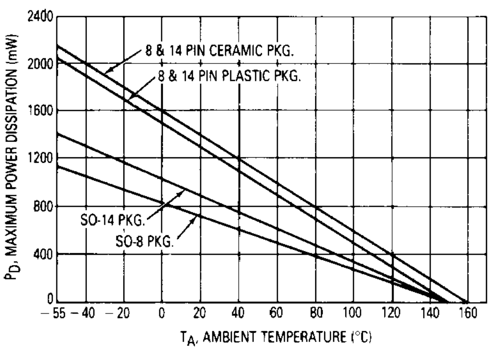

FIGURE 2 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

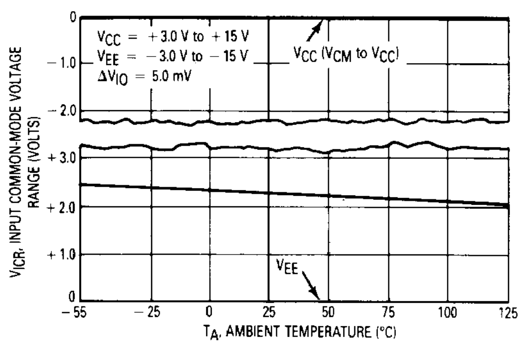

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FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE

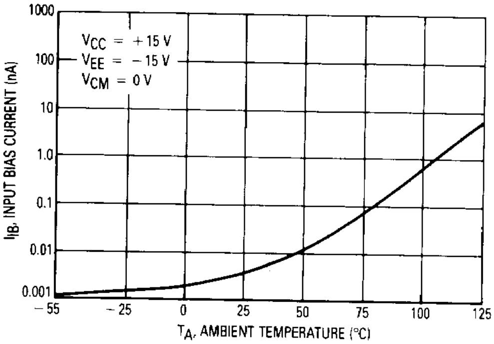

FIGURE 4 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE

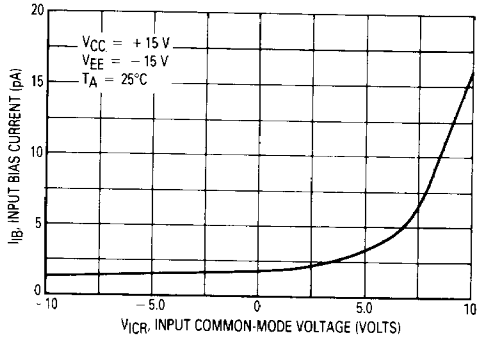

FIGURE 5 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE

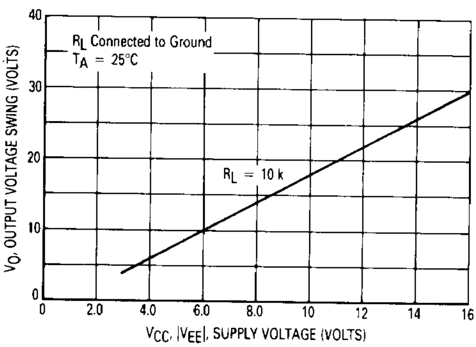

FIGURE 6 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

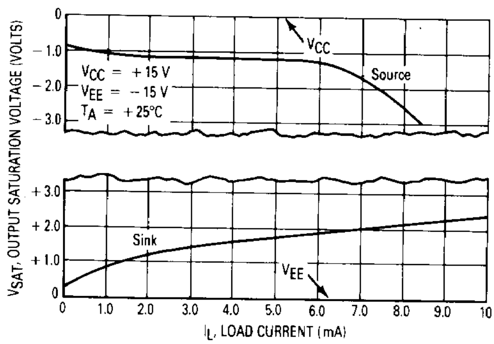

FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND

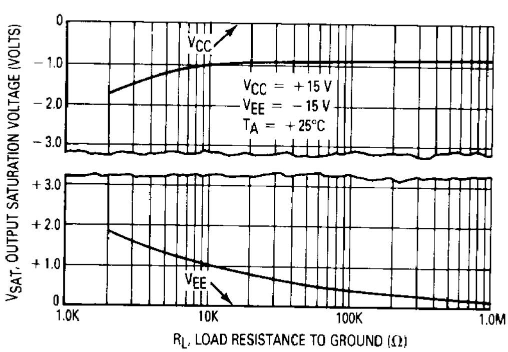

FIGURE 8 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO V_{CC}

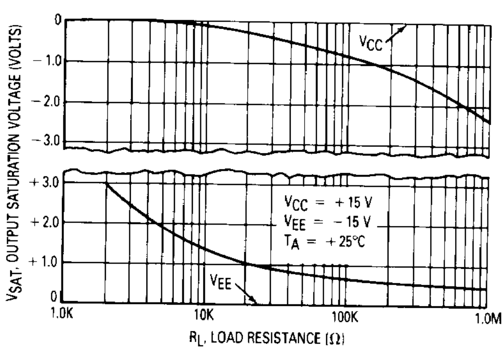

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FIGURE 9 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE

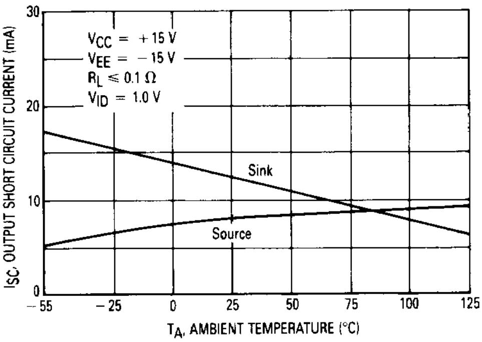

FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

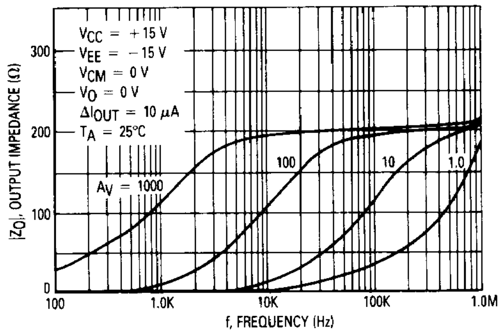

FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

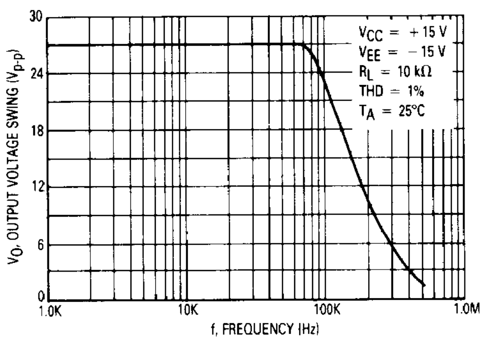

FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

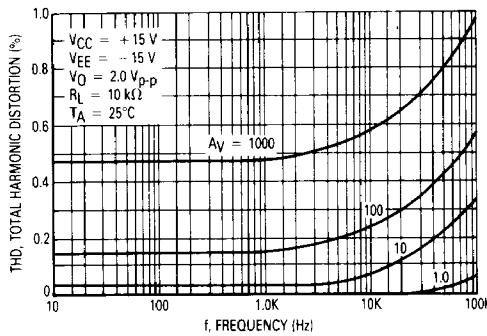

FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

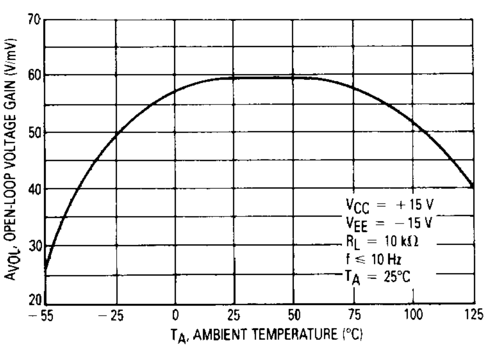

FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

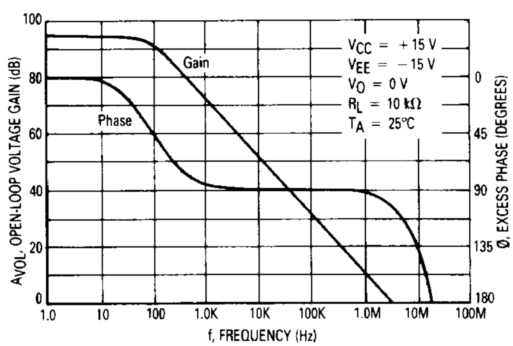

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FIGURE 15 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE

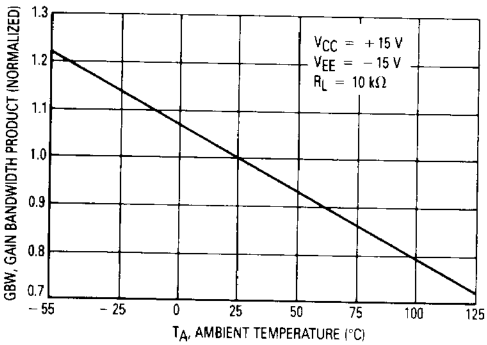

FIGURE 16 — OUTPUT VOLTAGE OVERSHOOT versus LOAD CAPACITANCE

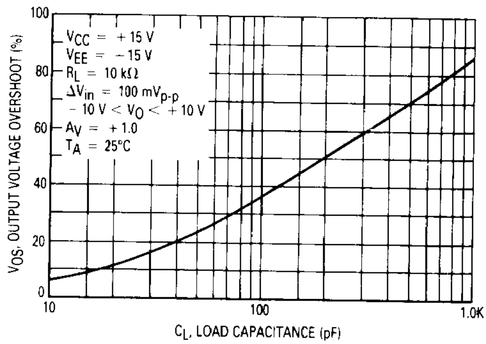

FIGURE 17 — PHASE MARGIN versus LOAD CAPACITANCE

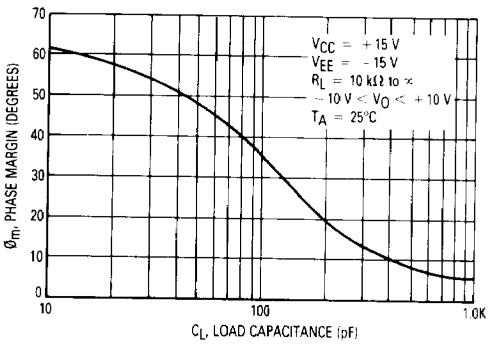

FIGURE 18 — GAIN MARGIN versus LOAD CAPACITANCE

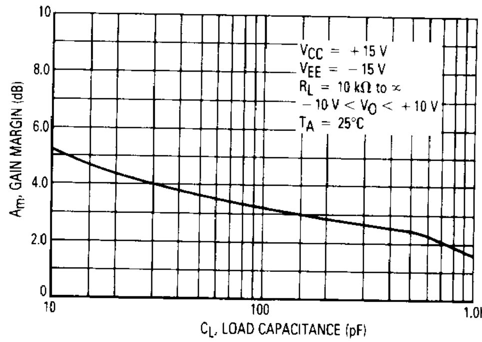

FIGURE 19 — PHASE MARGIN versus TEMPERATURE

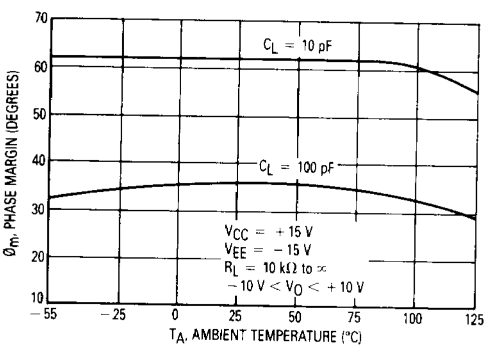

FIGURE 20 — GAIN MARGIN versus TEMPERATURE

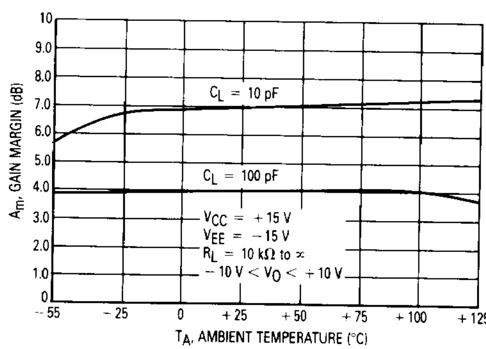

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FIGURE 27 — CHANNEL SEPARATION versus FREQUENCY

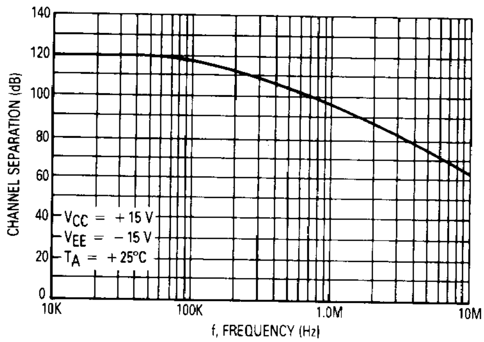

FIGURE 28 — TRANSIENT RESPONSE

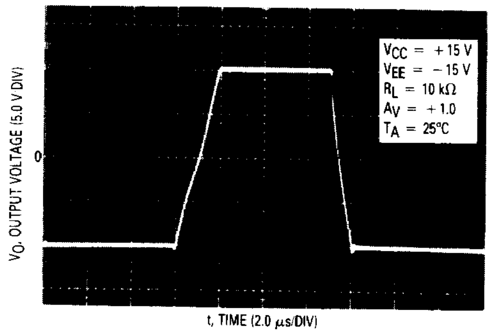

FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE