



# LC7940KD

# LC7941KDR

CMOS IC

## Dot-Matrix LCD Drivers

### Overview

The LC7940KD and LC7941KDR are segment driver LSIs for driving large, dot-matrix LCD displays. They read 4-bit parallel or serial input, display data from a controller into an 80-bit latch, and then generate LCD drive signals corresponding to that data. The LC7940KD and LC7941KDR feature mirror-image pin assignments, allowing them to be used together to increase component density. They are designed to be used with the LC7942KD (QIP80D) common driver to drive large LCD panels.

### Features

- 80 built-in LCD display drive circuits
- 1/8 to 1/128 display duty cycle
- Serial or 4-bit parallel data input
- Chip disable for low power dissipation for large-sized panels
- Bias supply voltage can be supplied externally
- Operating supply voltage and ambient temperature
  - V<sub>DD</sub> (logic block): 2.7 to 5.5V/-20 to +85°C
  - V<sub>DD</sub>-V<sub>EE</sub> (LCD block): 8 to 20V/-20 to +85°C
- CMOS process
- Package: QIP100D(LC7940KD)/QIP100DR(LC7941KDR)

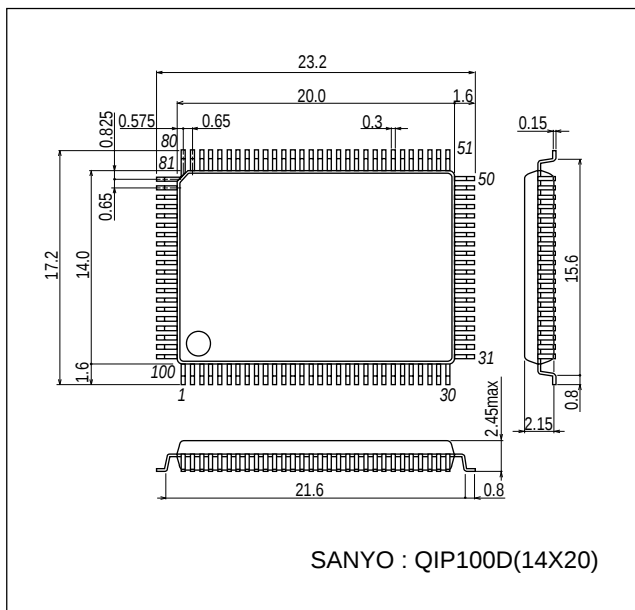
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unit: mm (typ)

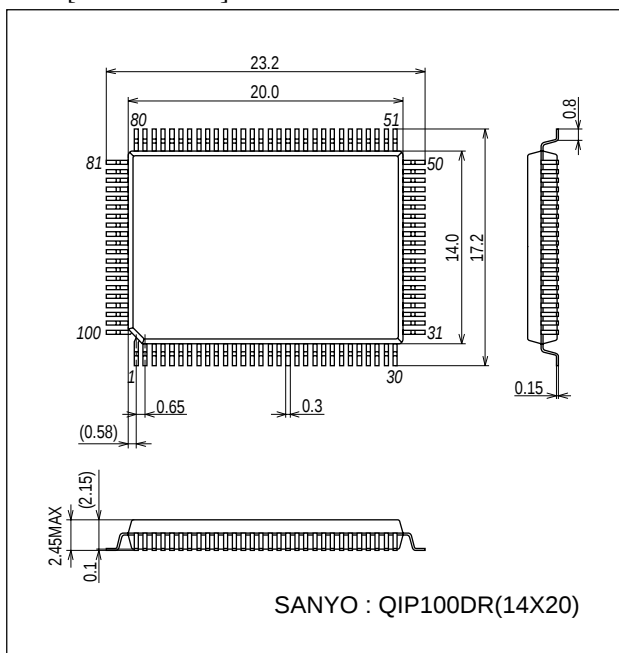
3180 [LC7940KD]



## Package Dimensions

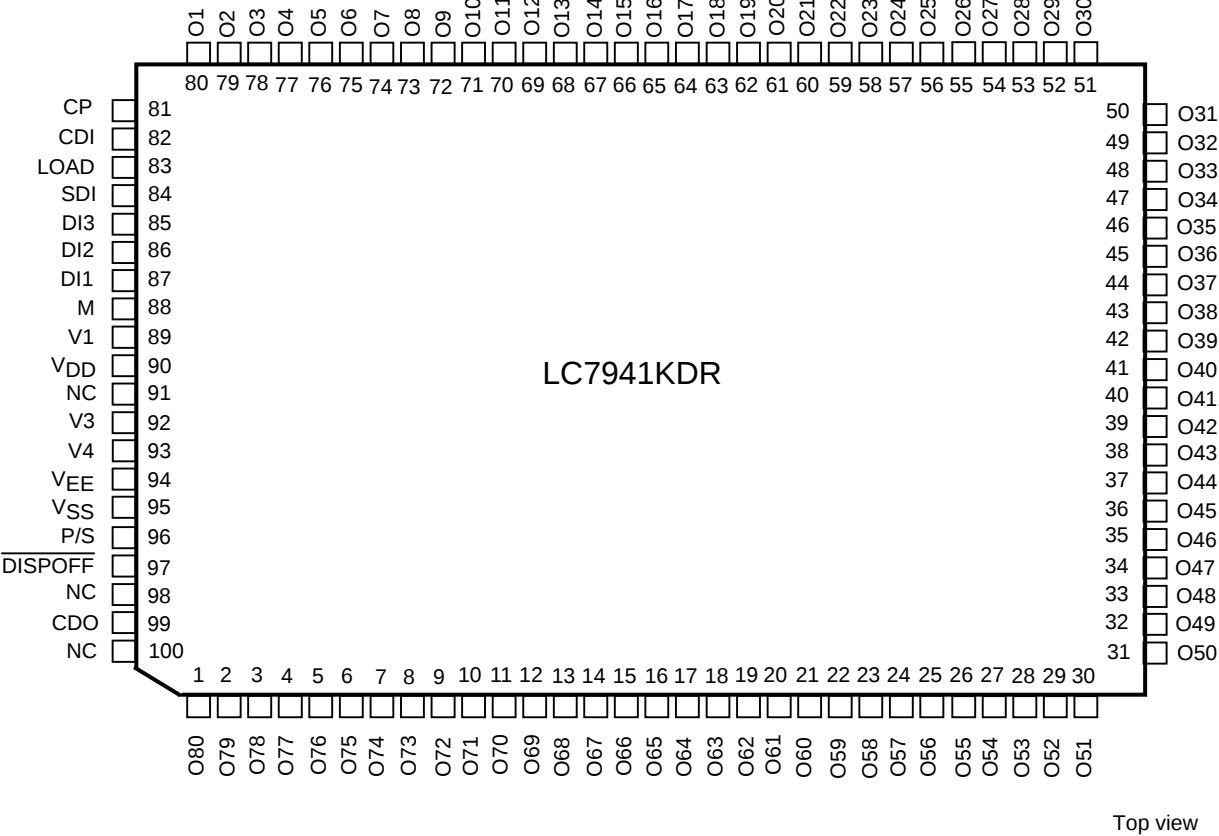
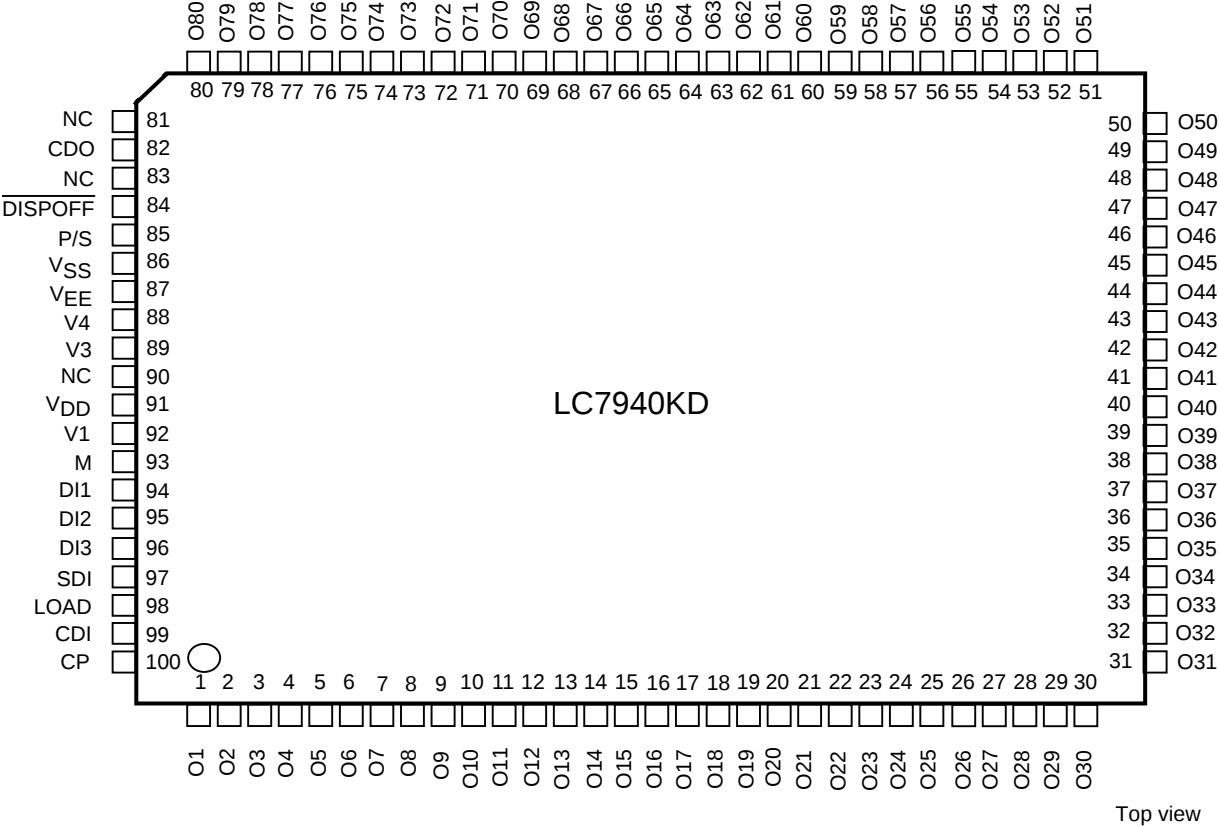
unit: mm (typ)

3329 [LC7941KDR]

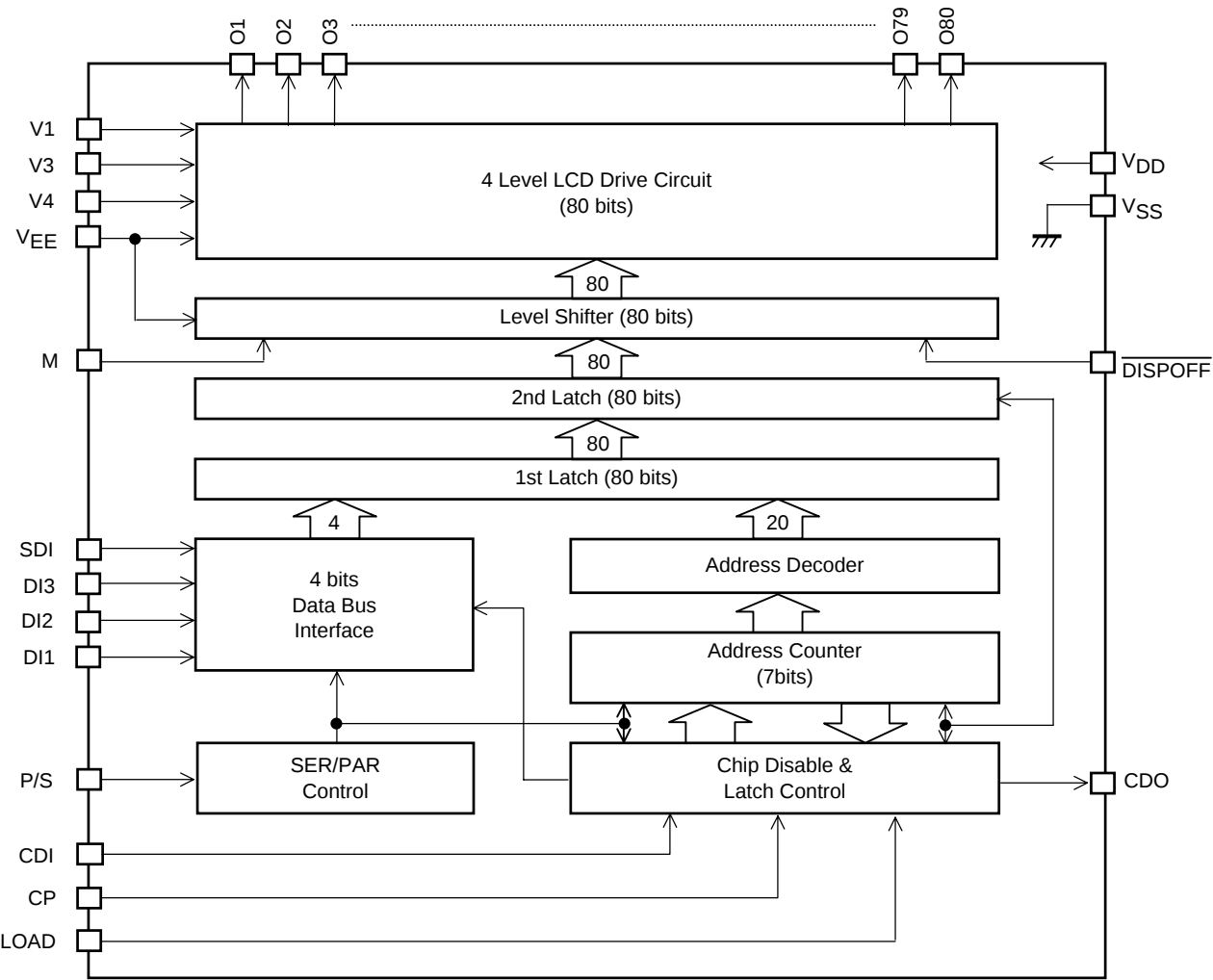


LC7940KD / LC7941KDR

[Pin Assignment](#) 供应商



Block Diagram"供应商



# LC7940KD / LC7941KDR

查海Function"供应商

| Pin No     |           | Symbol                      | I/O             | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
|------------|-----------|-----------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---|-----------------------------|--------|---|-----|----|----|---|-----|-----|----|----|-----|-----|----|----|-----|-----|-----------------|----|-----|---|----|
| LC7940KD   | LC7941KDR |                             |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 91         | 90        | V <sub>DD</sub>             | Supply          | LCD panel drive voltage supplies<br>V <sub>DD</sub> -V <sub>SS</sub> is the logic supply.<br>V <sub>DD</sub> -V <sub>EE</sub> is the LCD supply.                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 86         | 95        | V <sub>SS</sub>             |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 87         | 94        | V <sub>EE</sub>             |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 92         | 89        | V1                          | Supply          | LCD panel drive voltage supplies<br>V1 and V <sub>EE</sub> are selected levels.<br>V3 and V4 are not-selected levels.                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 89         | 92        | V3                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 88         | 93        | V4                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 100        | 81        | CP                          | I               | Display data input clock (falling edge trigger).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 99         | 82        | CDI                         | I               | Chip disable.<br>Data is read in When LOW, and not read in When HIGH.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 98         | 83        | LOAD                        | I               | Display data latch clock (falling edge trigger).<br>On the falling edge, the LCD drive signals set by the display data are output.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 97         | 84        | SDI                         | I               | Serial data input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 96         | 85        | DI3                         | I               | <table><tr><th colspan="2">Data input</th><th colspan="3">LCD driver output</th></tr><tr><td>SDI</td><td>O4</td><td>O8</td><td rowspan="4">→</td><td>O80</td></tr><tr><td>DI3</td><td>O3</td><td>O7</td><td>O79</td></tr><tr><td>DI2</td><td>O2</td><td>O6</td><td>O78</td></tr><tr><td>DI1</td><td>O1</td><td>O5</td><td>O77</td></tr></table>                                                                                                                                                                                                                                               | Data input |   | LCD driver output           |        |   | SDI | O4 | O8 | → | O80 | DI3 | O3 | O7 | O79 | DI2 | O2 | O6 | O78 | DI1 | O1              | O5 | O77 |   |    |
| Data input |           | LCD driver output           |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| SDI        | O4        | O8                          | →               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | O80        |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| DI3        | O3        | O7                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | O79        |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| DI2        | O2        | O6                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | O78        |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| DI1        | O1        | O5                          |                 | O77                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 95         | 86        | DI2                         | I               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 94         | 87        | DI1                         | I               | In serial data input mode, DI1 to DI3 should all be tied HIGH or LOW.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 93         | 88        | M                           | I               | LCD panel drive voltage output alternation control signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 85         | 96        | P/S                         | I               | Data input mode select. 4-bit parallel input when HIGH, and serial input when LOW.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 82         | 99        | CDO                         | O               | Cascade connection pin for extension segment drivers.<br>Data is read out when HIGH. Goes LOW after data is read out.<br>Connected to the CDI input of the next chip.                                                                                                                                                                                                                                                                                                                                                                                                                         |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 1 to 80    | 80 to 1   | O1 to O80                   | O               | <div>LCD drive outputs.<br/>The output drive level is determined by the display data, M signal and <math>\overline{\text{DISPOFF}}</math> input as shown below.<table><tr><th>M</th><th>Q</th><th><math>\overline{\text{DISPOFF}}</math></th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V<sub>EE</sub></td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table><br/>Note* don't care (tied HIGH or LOW)</div> | M          | Q | $\overline{\text{DISPOFF}}$ | Output | L | L   | H  | V3 | L | H   | H   | V1 | H  | L   | H   | V4 | H  | H   | H   | V <sub>EE</sub> | *  | *   | L | V1 |
| M          | Q         | $\overline{\text{DISPOFF}}$ | Output          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| L          | L         | H                           | V3              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| L          | H         | H                           | V1              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| H          | L         | H                           | V4              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| H          | H         | H                           | V <sub>EE</sub> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| *          | *         | L                           | V1              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 84         | 97        | $\overline{\text{DISPOFF}}$ | I               | O1 to O80 output control input pin.<br>When LOW, V1 is output on the O1 to O80 outputs.<br>See the truth table.                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 81         | 91        | NC                          | -               | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 83         | 98        | NC                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |
| 90         | 100       | NC                          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |   |                             |        |   |     |    |    |   |     |     |    |    |     |     |    |    |     |     |                 |    |     |   |    |

# LC7940KD / LC7941KDR

## Specifications

**Absolute Maximum Ratings** at  $T_a=25\pm2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                      | Symbol              | Conditions | Ratings              | Unit             |
|--------------------------------|---------------------|------------|----------------------|------------------|
| Maximum supply voltage (logic) | $V_{DD}$ max        | -          | -0.3 to +7.0         | V                |
| Maximum supply voltage (LCD)   | $V_{DD}-V_{EE}$ max | *1         | 0 to 22              | V                |
| Maximum input voltage          | $V_I$ max           | -          | -0.3 to $V_{DD}+0.3$ | V                |
| Operating temperature range    | $T_{opr}$           | -          | -20 to +85           | $^\circ\text{C}$ |
| Storage temperature range      | $T_{stg}$           | -          | -40 to +125          | $^\circ\text{C}$ |

Note \*1 The following relations between elements should be maintained:

$$V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}, V_{DD}-V_3 \leq 7\text{V}, V_4-V_{EE} \leq 7\text{V}$$

**Allowable Operating Ranges** at  $T_a = -20$  to  $85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

| Parameter                    | Symbol          | Conditions                                          | Ratings     |     |             | Unit |
|------------------------------|-----------------|-----------------------------------------------------|-------------|-----|-------------|------|
|                              |                 |                                                     | min         | typ | max         |      |
| Supply voltage (logic)       | $V_{DD}$        | -                                                   | 2.7         | -   | 5.5         | V    |
| Supply voltage (LCD)         | $V_{DD}-V_{EE}$ | *2, 3                                               | 8           | -   | 20          | V    |
| Input high level voltage     | $V_{IH}$        | CP, CDI, DI1 to DI3, M, SDI, P/S, DISPOFF, and LOAD | $0.8V_{DD}$ | -   | -           | V    |
| Input low level voltage      | $V_{IL}$        | CP, CDI, DI1 to DI3, M, SDI, P/S, DISPOFF, and LOAD | -           | -   | $0.2V_{DD}$ | V    |
| CP Shift clock frequency     | $f_{CP}$        | CP                                                  | -           | -   | 3.3         | MHz  |
| CP pulse width               | $t_{WC}$        | CP                                                  | 100         | -   | -           | ns   |
| LOAD pulse width             | $t_{WL}$        | LOAD                                                | 100         | -   | -           | ns   |
| DIn and SDI to CP setup time | $t_{SETUP}$     | DIn and SDI to CP                                   | 80          | -   | -           | ns   |
| DIn and SDI to CP hold time  | $t_{HOLD}$      | DIn and SDI to CP                                   | 80          | -   | -           | ns   |
| CP to LOAD time              | $t_{CL1}$       | CP to LOAD                                          | 0           | -   | -           | ns   |
|                              | $t_{CL2}$       | CP to LOAD                                          | 100         | -   | -           | ns   |
| LOAD to CP time              | $t_{LC}$        | LOAD to CP                                          | 100         | -   | -           | ns   |
| CP rise time                 | $t_R$           | CP                                                  | -           | -   | 50          | ns   |
| CP fall time                 | $t_F$           | CP                                                  | -           | -   | 50          | ns   |
| LOAD rise time               | $t_{RL}$        | LOAD                                                | -           | -   | 50          | ns   |
| LOAD fall time               | $t_{FL}$        | LOAD                                                | -           | -   | 50          | ns   |

Note \*2 The following relations between elements should be maintained:

$$V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}, V_{DD}-V_3 \leq 7\text{V}, V_4-V_{EE} \leq 7\text{V}$$

\*3 When the power is turned on, either the logic system power must be turned on before the LCD drive system power or else they must both be turned on at the same time. When the power is turned off, either the LCD drive system power must be turned off before the logic system power, or else both must be turned off at the same time.

# LC7940KD / LC7941KDR

Electrical Characteristics at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

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| Parameter                 | Symbol      | Conditions                                                                             | Ratings      |     |     | Unit             |
|---------------------------|-------------|----------------------------------------------------------------------------------------|--------------|-----|-----|------------------|
|                           |             |                                                                                        | min          | typ | max |                  |
| Input high level current  | $I_{IH}$    | $V_{IN} = V_{DD}$ : LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and DISPOFF                | -            | -   | 1   | $\mu\text{A}$    |
| Input low level current   | $I_{IL}$    | $V_{IN} = V_{SS}$ : LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and DISPOFF                | -1           | -   | -   | $\mu\text{A}$    |
| Output high level voltage | $V_{OH}$    | $I_{OH} = -400\mu\text{A}$ : CDO                                                       | $V_{DD}-0.4$ | -   | -   | V                |
| Output low level voltage  | $V_{OL}$    | $I_{OL} = 400\mu\text{A}$ : CDO                                                        | -            | -   | 0.4 | V                |
| Driver on resistance      | $R_{ON}$    | $V_{DD}-V_{EE} = 18\text{V}$ , $ V_{DE}-V_O  = 0.25\text{V}$ *4                        | -            | 0.7 | 2   | $\text{k}\Omega$ |
| Standby current drain     | $I_{ST}$    | CDI = $V_{DD}$ , $V_{DD}-V_{EE} = 18\text{V}$ , CP = 3.3MHz, Output unloaded: $V_{SS}$ | -            | -   | 200 | $\mu\text{A}$    |
| Operating current drain   | $I_{SS}$ *5 | $V_{DD}-V_{EE} = 18\text{V}$ , CP = 3.3MHz, LOAD = 5.156kHz M = 52Hz: $V_{SS}$         | -            | -   | 1.0 | mA               |
|                           | $I_{EE}$ *6 | $V_{DD}-V_{EE} = 18\text{V}$ , CP = 3.3MHz, LOAD = 5.156kHz M = 52Hz: $V_{EE}$         | -            | -   | 0.1 | mA               |

Note \*4  $V_{DE}$  = one of  $V_1$ ,  $V_3$ ,  $V_4$  or  $V_{EE}$ .  $V_1 = V_{DD}$ ,  $V_3 = 9/11(V_{DD}-V_{EE})$ ,  $V_4 = 2/11(V_{DD}-V_{EE})$

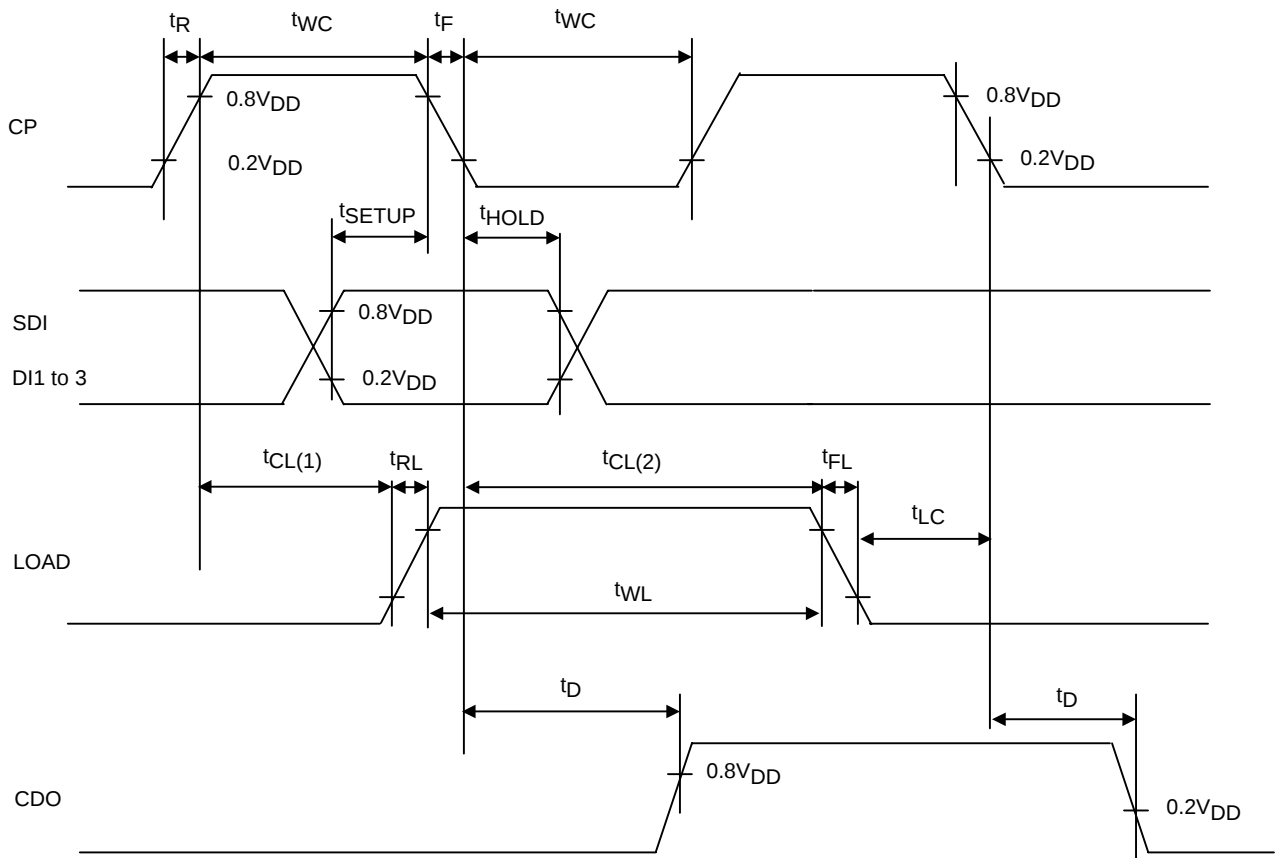
\*5  $I_{SS}$  is the current flowing from  $V_{DD}-V_{SS}$ .

\*6  $I_{EE}$  is the current flowing from  $V_{DD}-V_{EE}$

Switching Characteristics at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

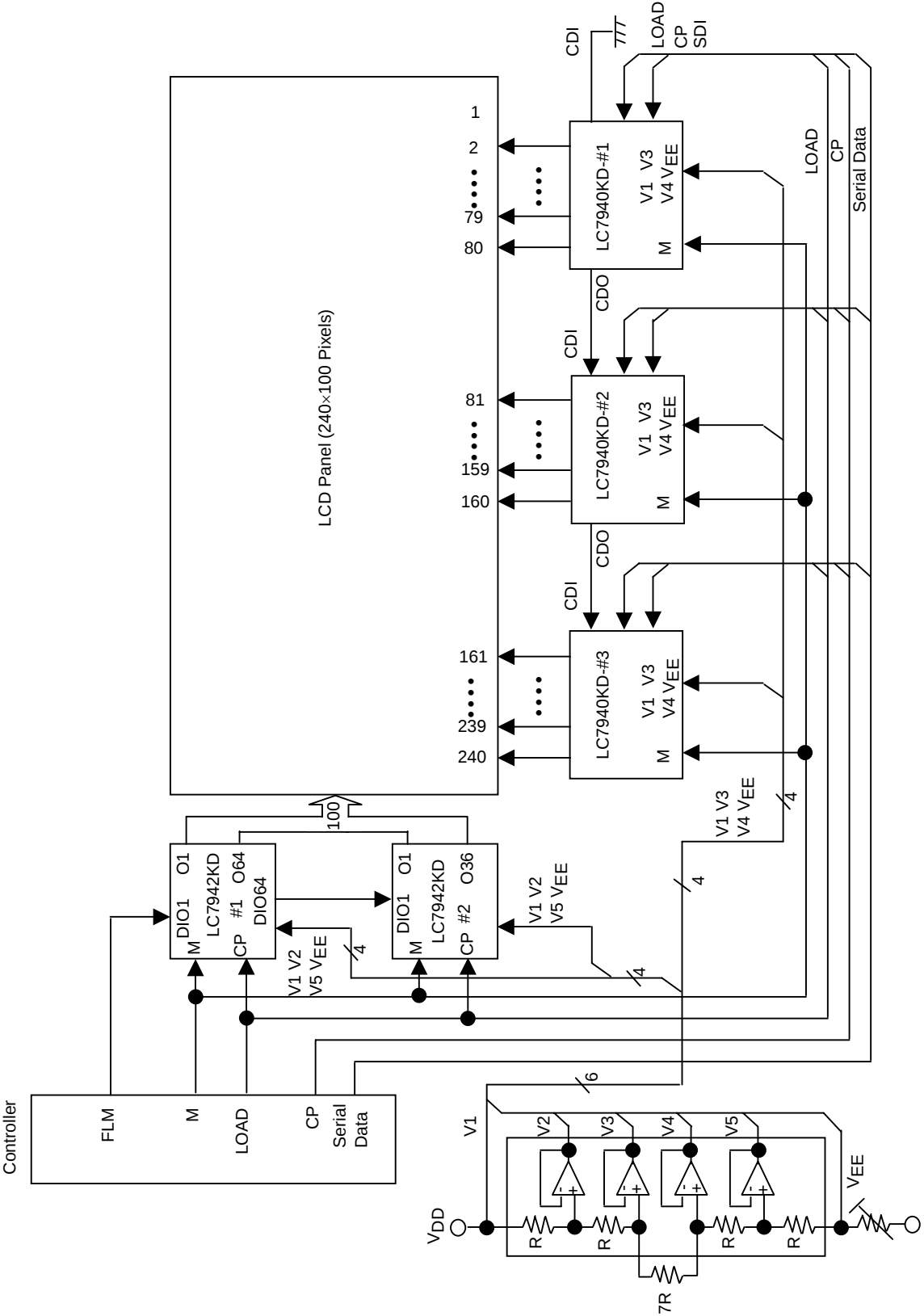
| Parameter         | Symbol | Conditions   | Ratings |     |     | Unit |
|-------------------|--------|--------------|---------|-----|-----|------|
|                   |        |              | min     | typ | max |      |
| Output delay time | $t_D$  | CL=30pF: CDO | -       | -   | 200 | ns   |

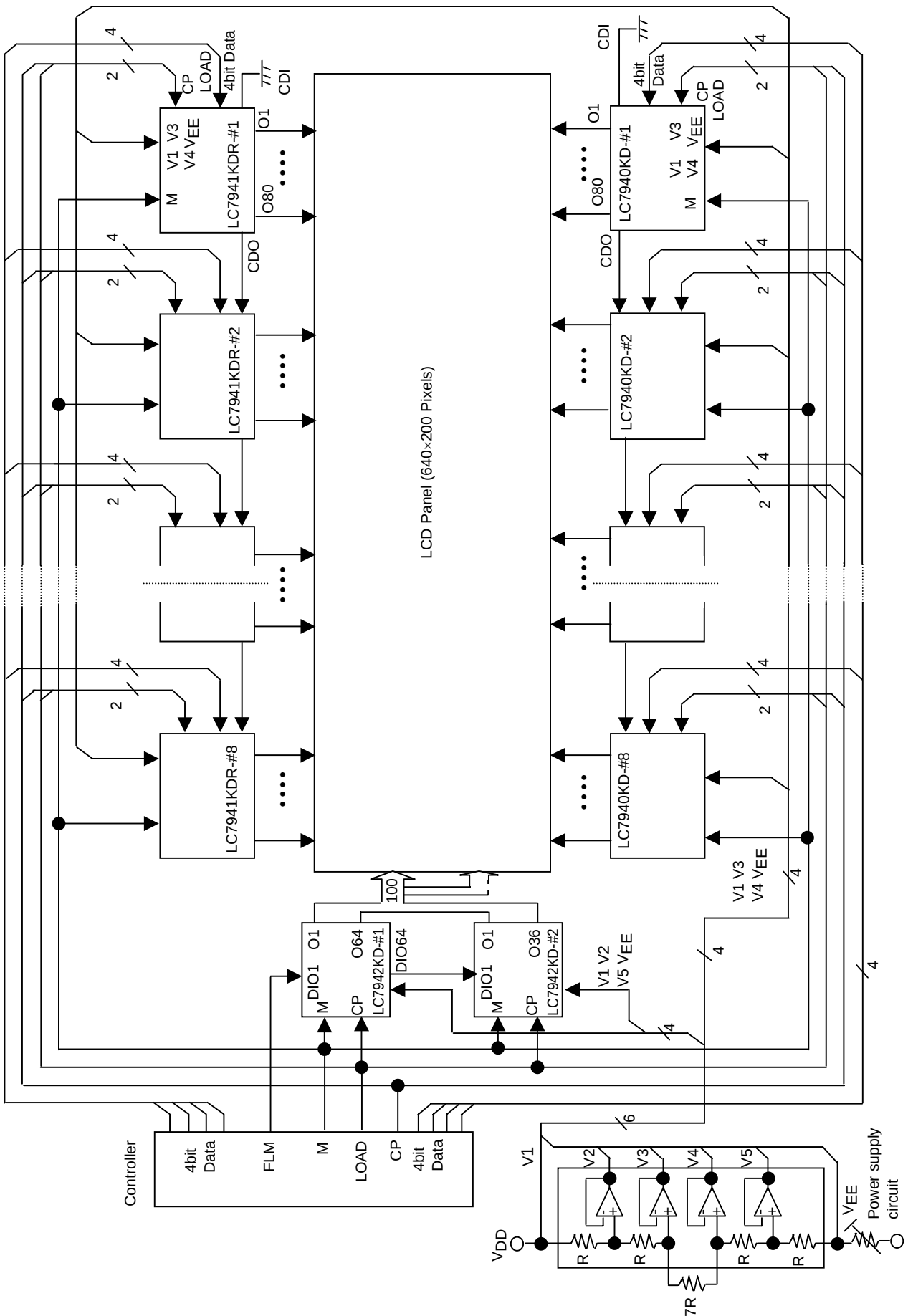
## Switching Characteristics Diagram



Application Notes 应用笔记

Chapter 10 LCD Panel1



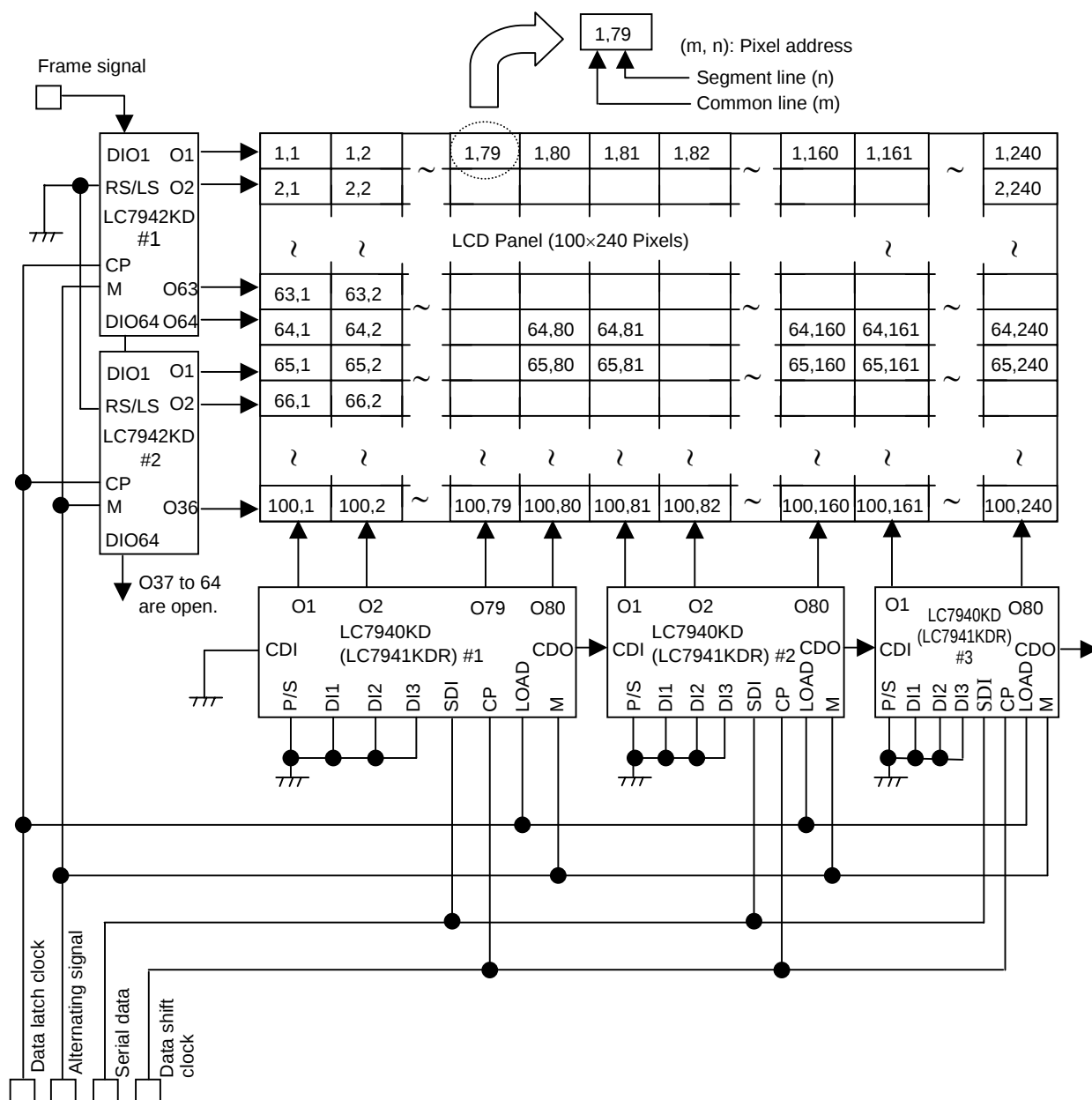


## 100×240-Pixel LCD Panel Application

A 100×240-Pixel LCD Panel requires the following drivers.

- 3×LC7940KD (or LC7941KDR) drivers
- 2×LC7942KD drivers

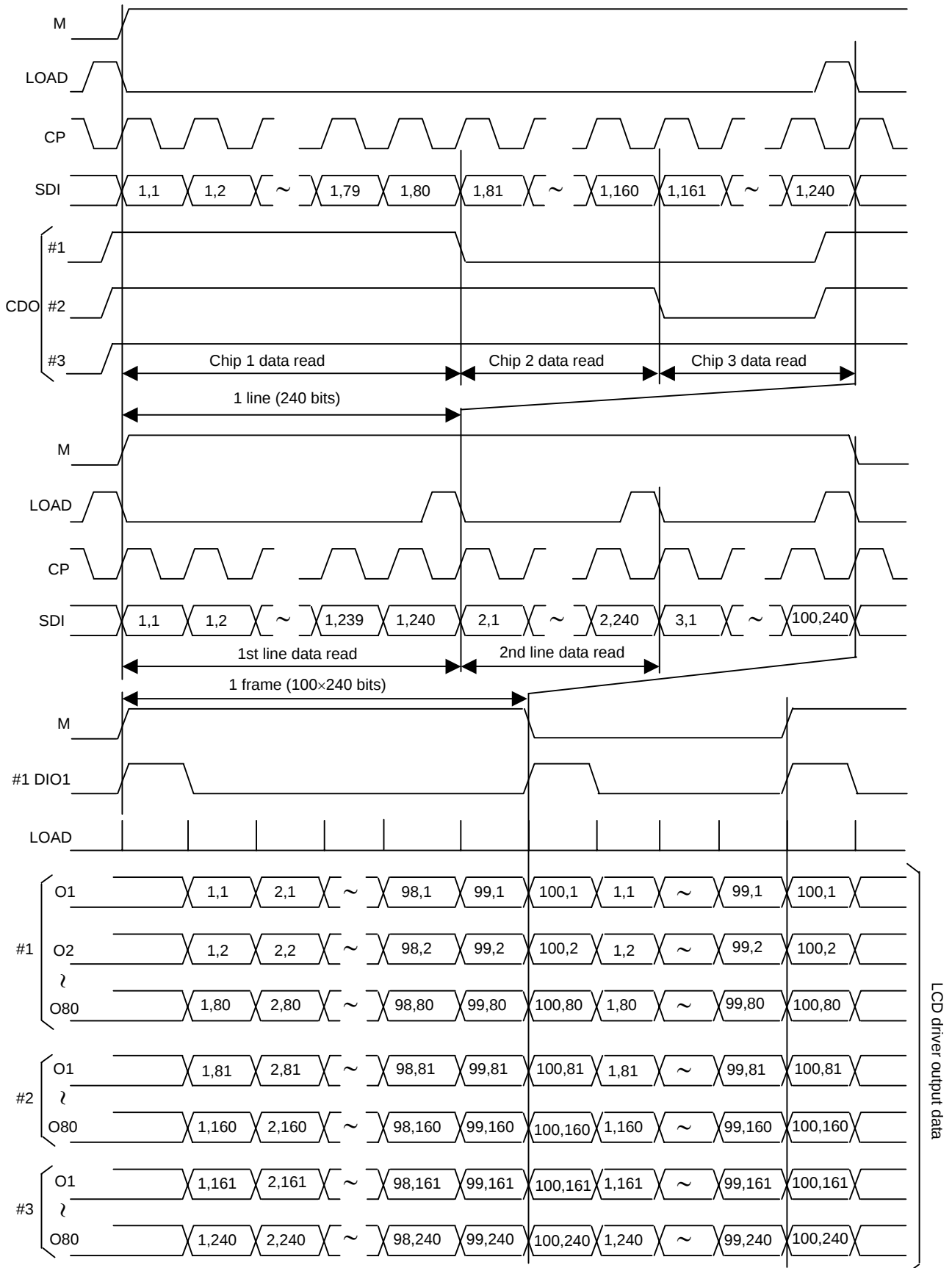
An example using 1/100 duty cycle is shown below.



(1) The LC7942KD chips are cascaded by connecting DIO64 on chip 1 to DIO1 on chip 2. For a 100-bit shift register, O37 to O64 on chip 2 are left open.

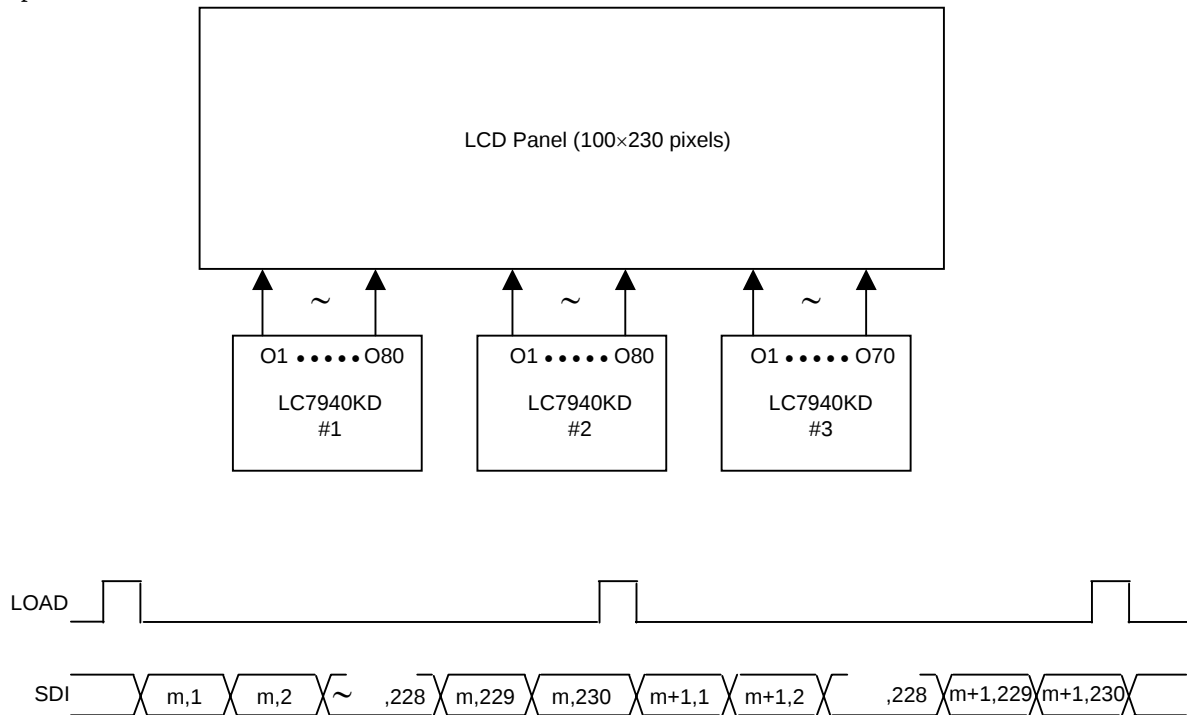
(2) The LC7940KD (or LC7941KDR) chips are cascaded by connecting CDO on chip 1 to CDI on chip 2, and CDO on chip 2 to CDI on chip 3. CDI on chip 1 is tied to GND, and CDO on chip 3 is not used. This configuration allows the input of 240-bit serial data.

# 100×240-pixel LCD Panel Timing Diagram



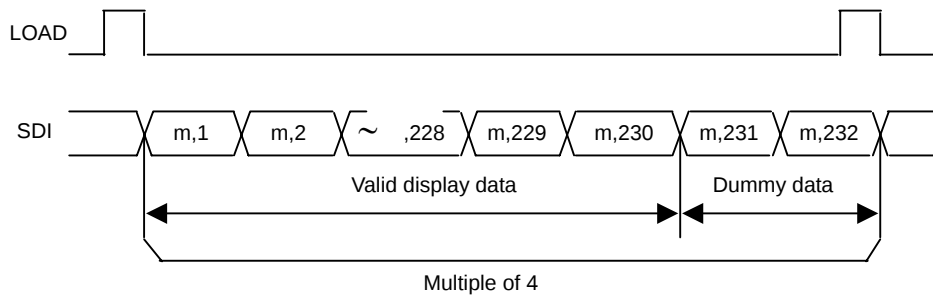
## Segment Data Output Multiples of 4

Example.



If this timing data is sent, data elements (m, 229), (m, 230), (m+1, 229), (m+1, 230)... will not appear in the output (O69 and O70 on chip 3). This is because the LC7940KD (or LC7941KDR) converts serial/parallel data in 4-bit units, which also decrease power dissipation.

For data that is not a multiple of 4, like 230, the following scheme is used.



In this case, (m, 231) is output on O71 on chip 3, and (m, 232) on O72 on chip 3. However, these outputs are not connected to the panel and are, therefore, invalid.

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