NDF05N50Z, NDP05N50Z, NDD05N50Z

N-Channel Power MOSFET 500 V, 1.25 Ω

Features

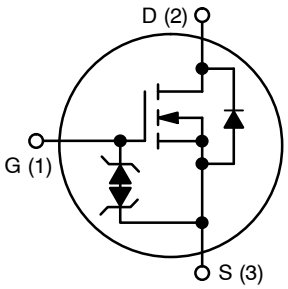
- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

V_{DSS}	$R_{DS(on)}$ (TYP) @ 2.2 A
500 V	1.25 Ω

N−Channel

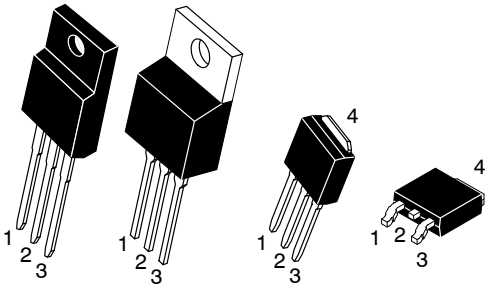


ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDP	NDD	Unit
Drain−to−Source Voltage	V_{DSS}	500			V
Continuous Drain Current $R_{\theta JC}$	I_D	5 (Note 1)	5	4.7	A
Continuous Drain Current $R_{\theta JC}$, T_A = 100°C	I_D	3.2 (Note 1)	3.2	3	A
Pulsed Drain Current, V_{GS} @ 10 V	I_{DM}	20 (Note 1)	20	19	A
Power Dissipation $R_{\theta JC}$	P_D	28	96	83	W
Gate−to−Source Voltage	V_{GS}	±30			V
Single Pulse Avalanche Energy, I_D = 5.0 A	E_{AS}	130			mJ
ESD (HBM) (JESD22−A114)	V_{esd}	3000			V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T_A = 25°C) (Figure 17)	V_{ISO}	4500			V
Peak Diode Recovery	dv/dt	4.5 (Note 2)			V/ns
Continuous Source Current (Body Diode)	I_S	5			A
Maximum Temperature for Soldering Leads	T_L	260			°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Limited by maximum junction temperature
2. I_S = 4.4 A, di/dt ≤ 100 A/μs, $V_{DD} \le BV_{DSS}$, T_J = +150°C



TO−220FP CASE 221D STYLE 1 | **TO−220AB CASE 221A STYLE 5** | **IPAK CASE 369D STYLE 2** | **DPAK CASE 369AA STYLE 2**

MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

THERMAL RESISTANCE

Parameter		Symbol	Value	Unit
Junction−to−Case (Drain)	NDP05N50Z NDF05N50Z NDD05N50Z	$R_{\theta JC}$	1.3 4.4 1.5	°C/W
Junction−to−Ambient Steady State	(Note 3) NDP05N50Z (Note 3) NDF05N50Z (Note 4) NDD05N50Z (Note 3) NDD05N50Z−1	$R_{\theta JA}$	50 50 38 80	

3. Insertion mounted
4. Surface mounted on FR4 board using 1″ sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA		500			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, I_D = 1 mA			0.6		V/°C
Drain−to−Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	25°C			1	μA
			150°C			50	
Gate−to−Source Forward Leakage	I_{GSS}	V_{GS} = ±20 V				±10	μA
ON CHARACTERISTICS (Note 5)							
Static Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.2 A			1.25	1.5	Ω
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 50 μA		3.0		4.5	V
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 2.5 A			3.5		S
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz			530		pF
Output Capacitance	C_{oss}				68		
Reverse Transfer Capacitance	C_{rss}				15		
Total Gate Charge	Q_g	V_{DD} = 250 V, I_D = 5 A, V_{GS} = 10 V			18.5		nC
Gate−to−Source Charge	Q_{gs}				4		
Gate−to−Drain (“Miller”) Charge	Q_{gd}				10		
Plateau Voltage	V_{GP}				6.5		V
Gate Resistance	R_g				4.5		Ω
RESISTIVE SWITCHING CHARACTERISTICS							
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 5 A, V_{GS} = 10 V, R_G = 5 Ω			11		ns
Rise Time	t_r				15		
Turn−Off Delay Time	$t_{d(off)}$				24		
Fall Time	t_f				14		
SOURCE−DRAIN DIODE CHARACTERISTICS (T_C = 25°C unless otherwise noted)							
Diode Forward Voltage	V_{SD}	I_S = 5 A, V_{GS} = 0 V				1.6	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, V_{DD} = 30 V I_S = 5 A, di/dt = 100 A/μs			255		ns
Reverse Recovery Charge	Q_{rr}				1.25		μC

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

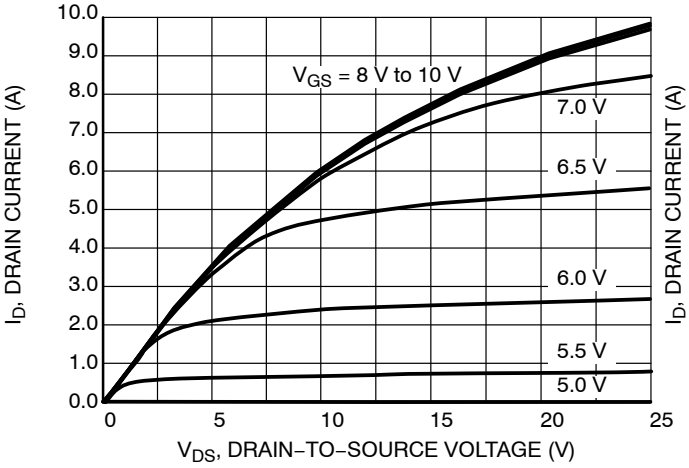


Figure 1. On−Region Characteristics

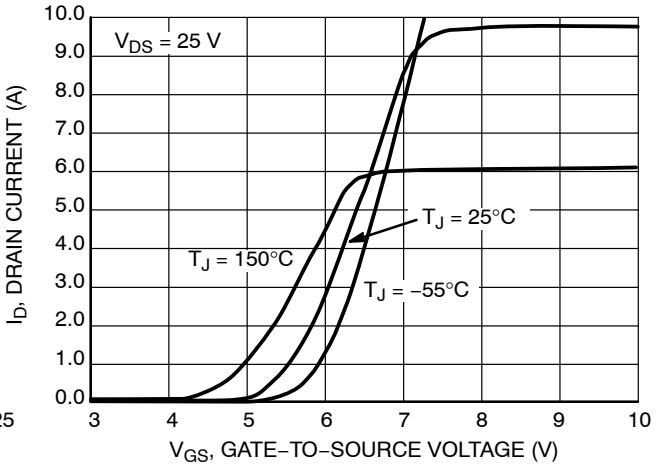


Figure 2. Transfer Characteristics

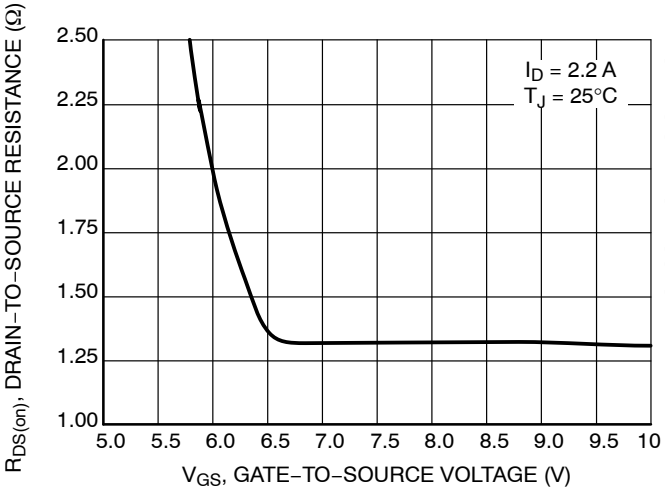


Figure 3. On−Region versus Gate−to−Source Voltage

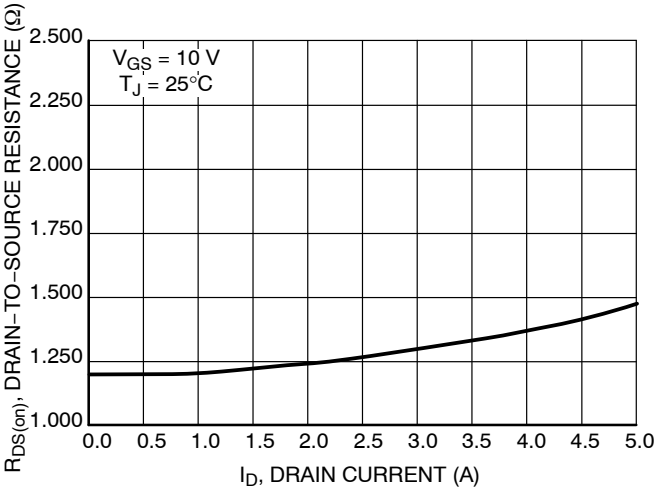


Figure 4. On−Resistance versus Drain Current and Gate Voltage

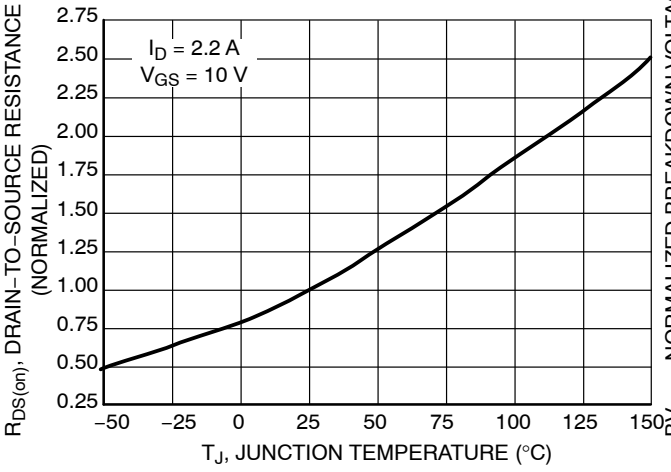


Figure 5. On−Resistance Variation with Temperature

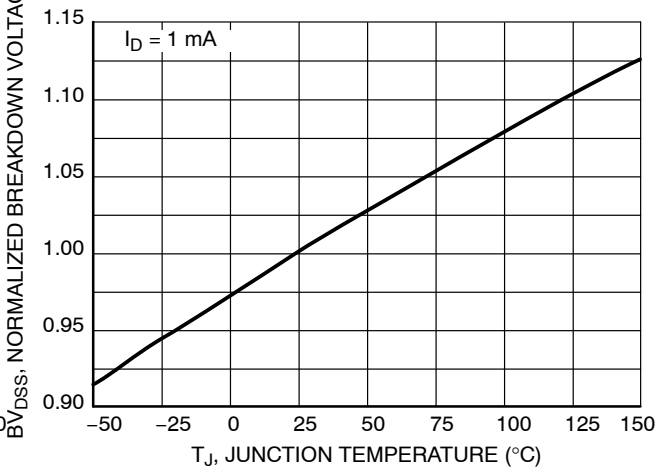


Figure 6. BV_{DSS} Variation with Temperature

TYPICAL CHARACTERISTICS

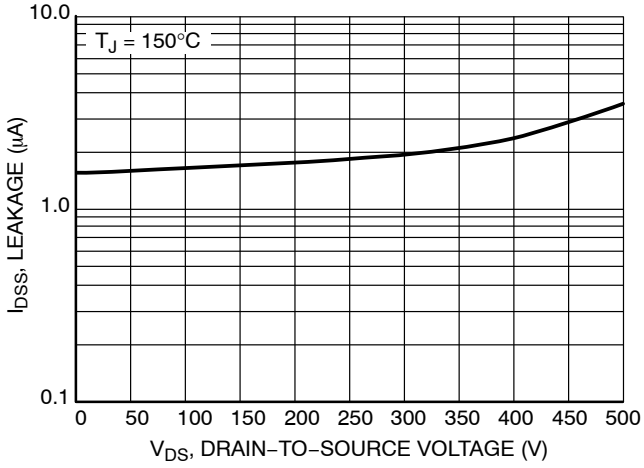


Figure 7. Drain−to−Source Leakage Current versus Voltage

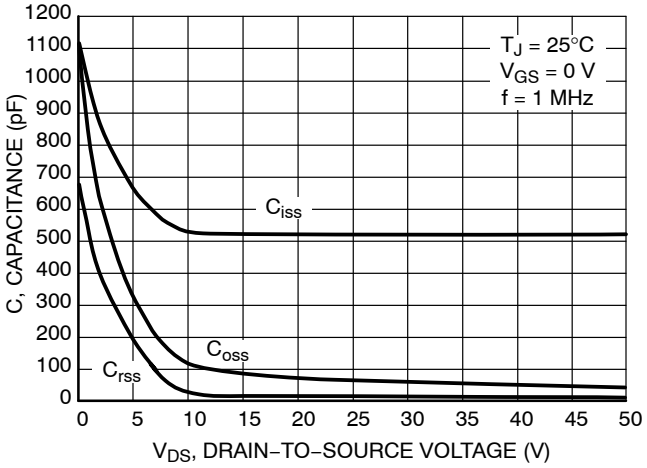


Figure 8. Capacitance Variation

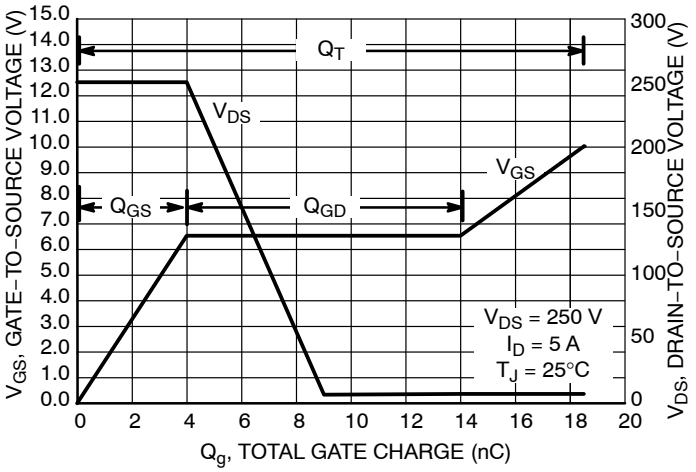


Figure 9. Gate−to−Source Voltage and Drain−to−Source Voltage versus Total Charge

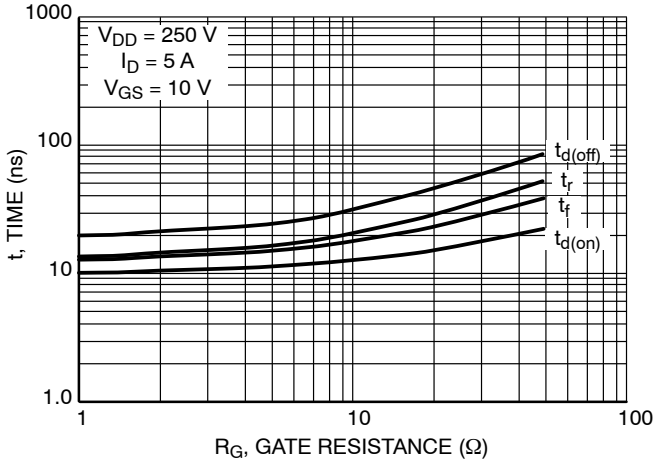


Figure 10. Resistive Switching Time Variation versus Gate Resistance

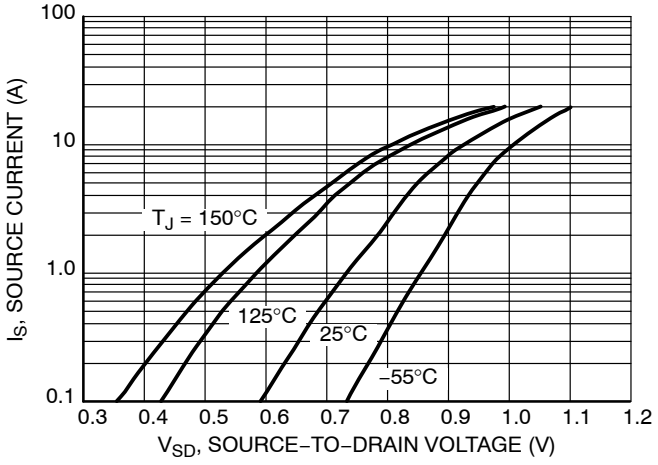


Figure 11. Diode Forward Voltage versus Current

TYPICAL CHARACTERISTICS

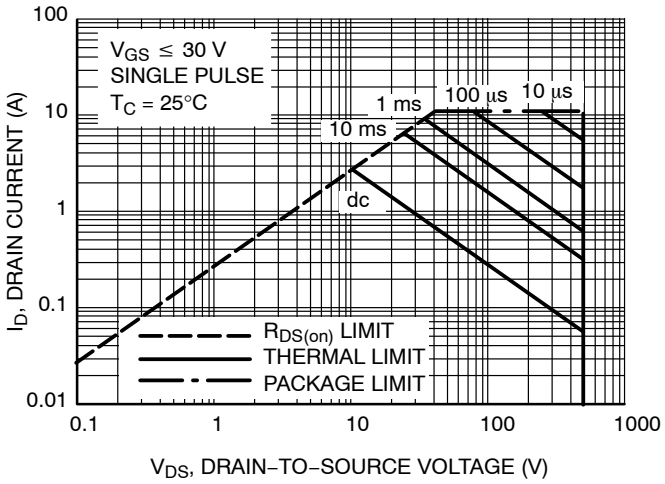


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDF05N50Z

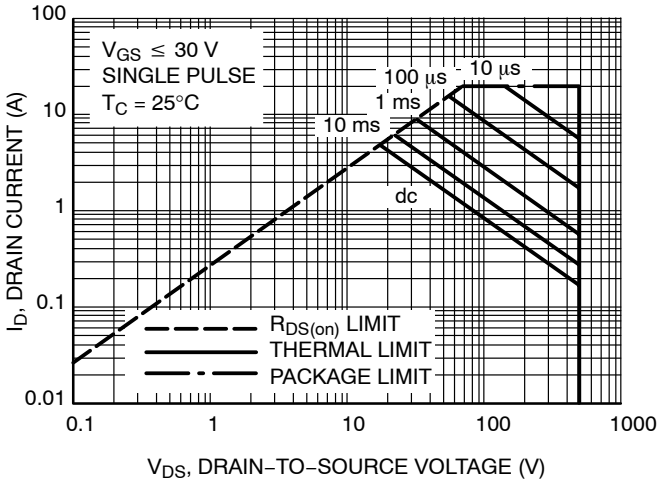


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDD05N50Z

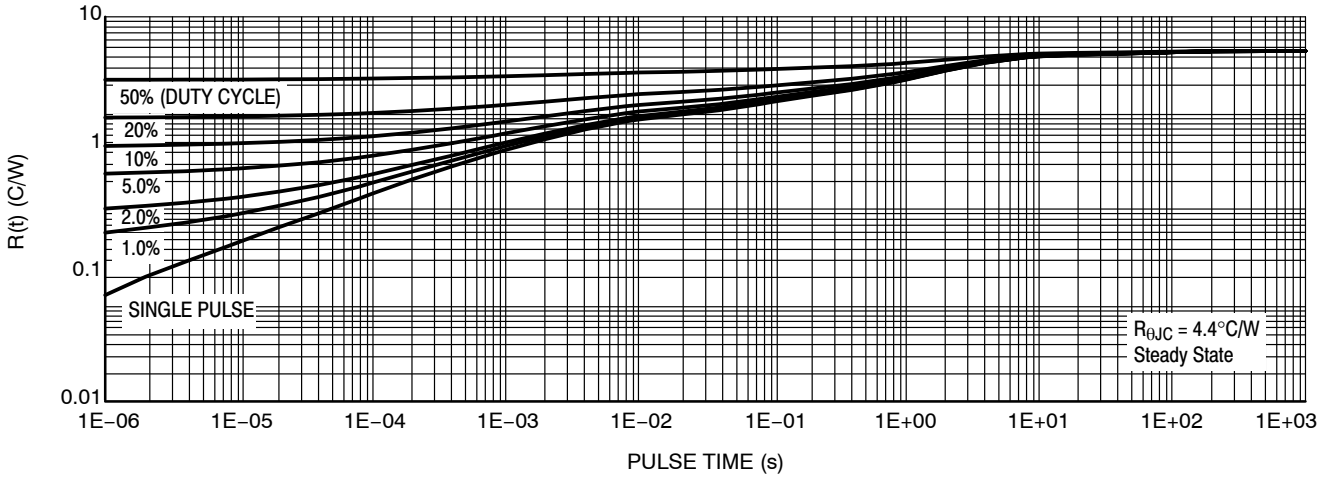


Figure 14. Thermal Impedance (Junction−to−Case) for NDF05N50Z

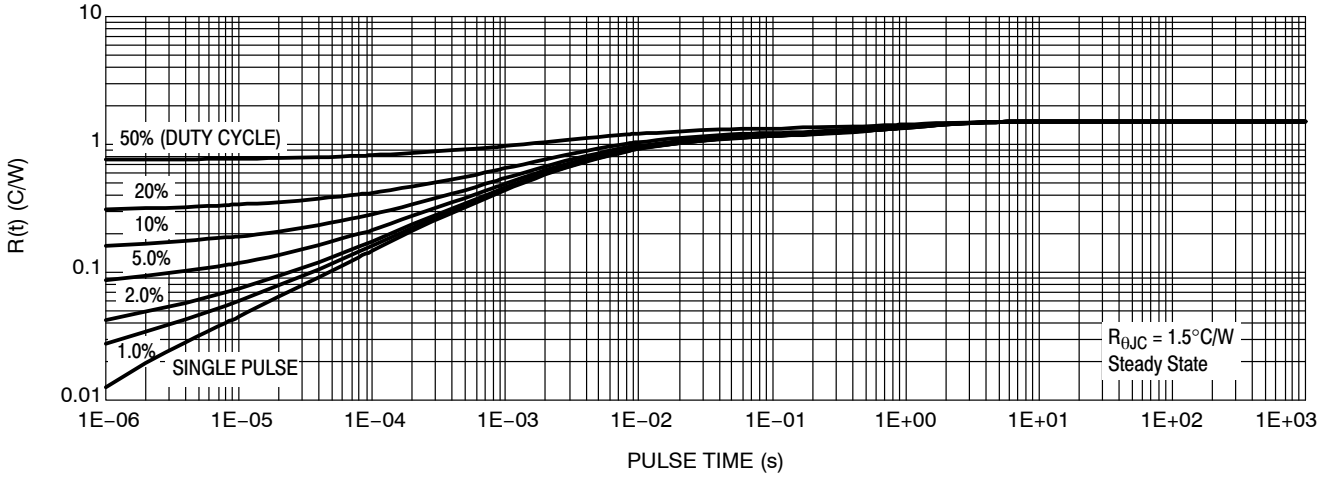


Figure 15. Thermal Impedance (Junction−to−Case) for NDD05N50Z

TYPICAL CHARACTERISTICS

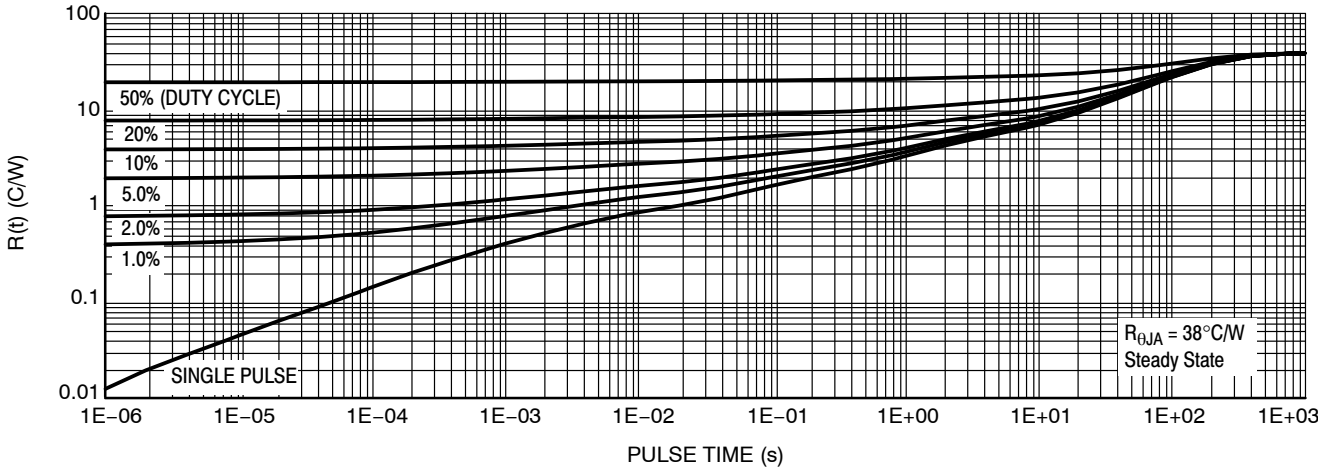


Figure 16. Thermal Impedance (Junction−to−Ambient) for NDD05N50Z

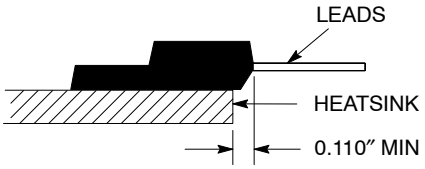


Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

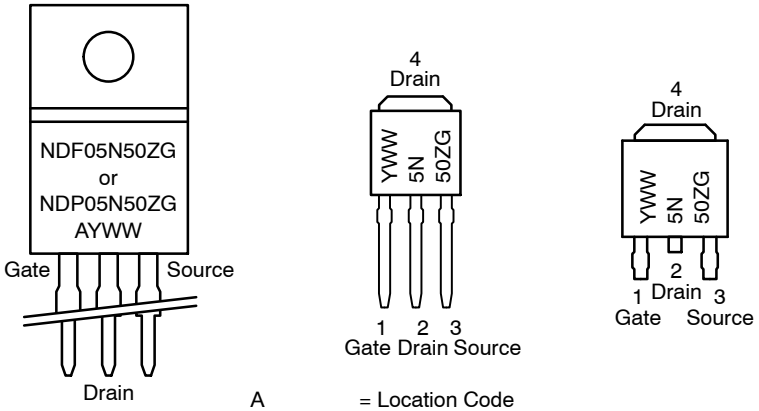
*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Order Number	Package	Shipping†
NDF05N50ZG	TO−220FP (Pb−Free)	50 Units / Rail
NDP05N50ZG	TO−220AB (Pb−Free)	50 Units / Rail (In Development)
NDD05N50Z−1G	IPAK (Pb−Free)	75 Units / Rail
NDD05N50ZT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

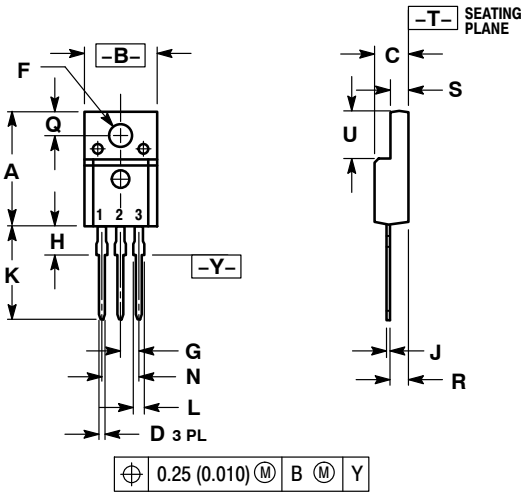
MARKING DIAGRAMS



A	= Location Code
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PACKAGE DIMENSIONS

TO−220 FULLPAK
CASE 221D−03
ISSUE K

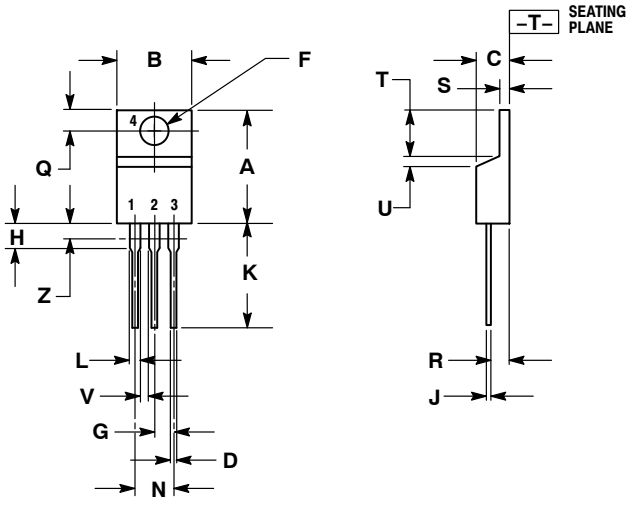


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

TO−220
CASE 221A−09
ISSUE AF



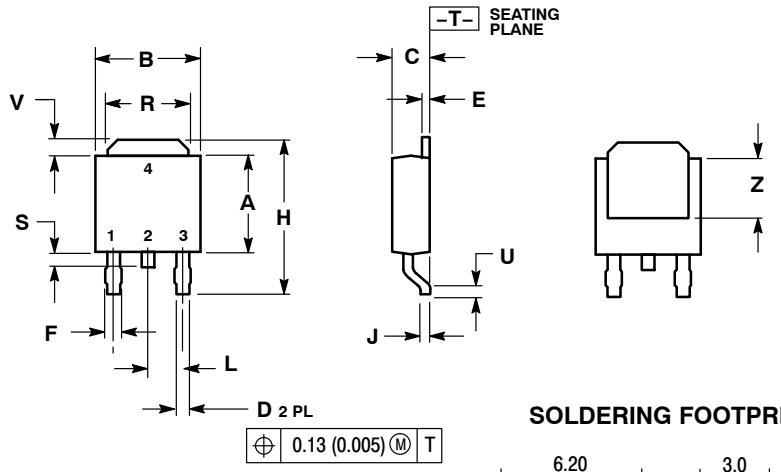
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

DPAK
CASE 369AA−01
ISSUE A

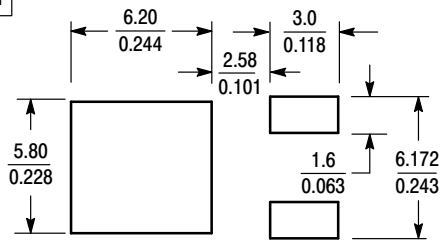


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

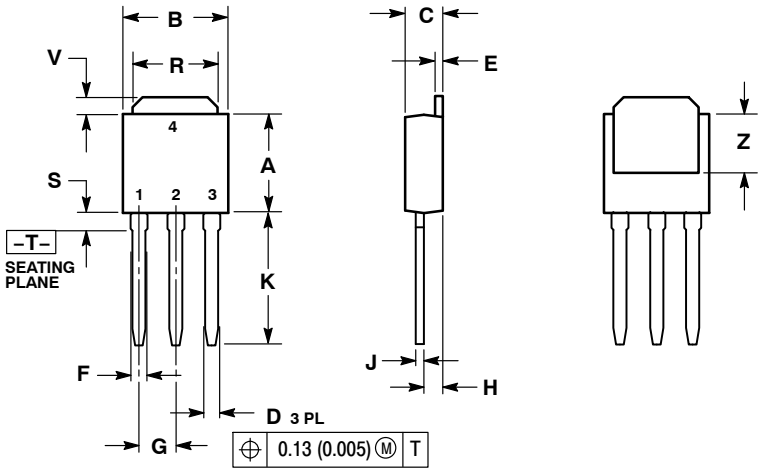
SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

IPAK
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative