REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS															
REV															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Sandra Rooney

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
96-06-12

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 1394 HIGH-SPEED SERIAL-BUS LINK-LAYER CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96770

SHEET 1 OF 19

DESC FORM 193
JUL 94

5962-E489-96

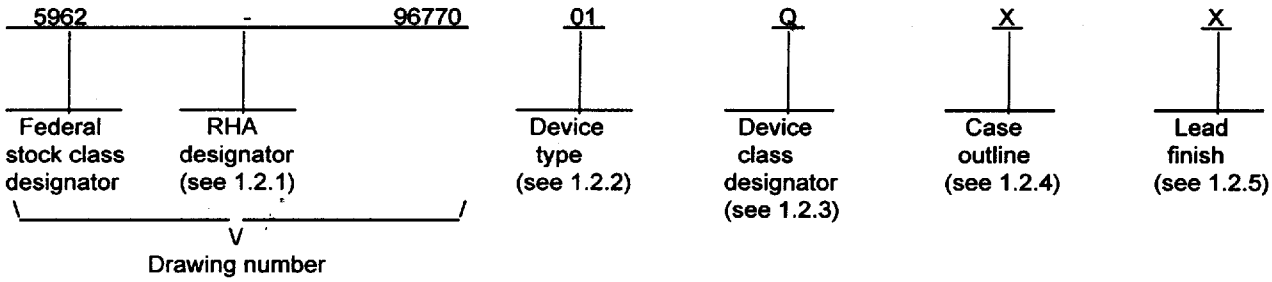
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0023466 6T6

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TSB12C01AM	1394 high-speed serial-bus link-layer controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Ceramic quad flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
Input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Input clamp current (I_{IK}) (V_I < 0.0 V or V_I > V_{CC})	±20 mA
Output clamp current (I_{OK}) (V_o < 0.0 V or V_o > V_{CC})	±20 mA
Continuous power dissipation (case X) at 25°C	2885 mW 3/
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction-to-case (Θ_{JC})	11°C/W
Thermal resistance, junction-to-air (Θ_{JA})	60°C/W
Junction temperature (T_J)	+175°C
Case temperature for 10 seconds: (T_C)	+260°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	+4.75 V dc to +5.25 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
High level input voltage range (V_{IH})	+2.0 V dc to V_{CC}
Low level input voltage range (V_{IL})	+0.0 V dc to +0.8 V
Clock frequency, BCLK	33 MHz
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ Above 25°C, derate at a factor of 19.2 mw/°C.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$I_{OH} = -4$ mA	All	1,2,3	V_{CC} - 0.8		V
Low level output voltage	V_{OL}	$I_{OL} = 4$ mA	All	1,2,3		0.5	V
Positive-going input threshold voltage	V_{IT+}		All	1,2,3		2	V
Negative-going input threshold voltage	V_{IT-}		All	1,2,3	0.8		V
Low-level input current	I_{IL}	$V_{IN} = GND$	All	1,2,3		-1.0	µA
High-level input current	I_{IH}	$V_{IN} = V_{CC}$	All	1,2,3		1.0	µA
High impedance-state output current 1/	I_{OZ}	$V_{OUT} = V_{CC}$ or GND	All	1,2,3		±10	µA
Input capacitance	C_{IN}	$V_{CC} = 5.0$ V, See 4.4.1b, $T_A = 25°C$	All	4		20.0	pF
Bidirectional capacitance	$C_{I/O}$					25.0	
Output capacitance	C_{OUT}					20.0	
Host-Interface Timing Requirements 2/							
Cycle time, BCLK	t_{c1}	$T_A = 25°C$, See figure 4	All	9	30		ns
Pulse duration, BCLK high	$t_{w1(H)}$	$T_A = 25°C$, See figure 4	All	9	10		ns
Pulse duration, BCLK low	$t_{w1(L)}$	$T_A = 25°C$, See figure 4	All	9	10		ns
Setup time, DATA (0:31) before BCLK↑	t_{su1}	$T_A = 25°C$, See figure 4	All	9	4		ns
Hold time, DATA (0:31) after BCLK↑	t_{h1}	$T_A = 25°C$, See figure 4	All	9	2		ns
Setup time, ADDR (0:7) before BCLK↑	t_{su2}	$T_A = 25°C$, See figure 4	All	9	12		ns
Hold time, ADDR(0:7) after BCLK↑	t_{h2}	$T_A = 25°C$, See figure 4	All	9	2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Setup time, $\overline{CS}$ before BCLK↑	t_{su3}	T_A = 25°C, See figure 4	All	9	12		ns
Hold time, $\overline{CS}$ after BCLK↑	t_{h3}	T_A = 25°C, See figure 4	All	9	2		ns
Setup time, $\overline{WR}$ before BCLK↑	t_{su4}	T_A = 25°C, See figure 4	All	9	12		ns
Hold time, $\overline{WR}$ after BCLK↑	t_{h4}	T_A = 25°C, See figure 4	All	9	2		ns
Host-Interface Switching Characteristics 2/							
Delay time, BCLK↑ to $\overline{CA}$	t_{d1}	C_L = 45 pF, See figure 4	All	9,10,11	4	16	ns
Delay time, BCLK↑ to $\overline{CA}$	t_{d2}	C_L = 45 pF, See figure 4	All	9,10,11	4	16	ns
Delay time, BCLK↑ to DATA(0:31) valid	t_{d3}	C_L = 45 pF, T_A = 25°C See figure 4	All	9	4	24	ns
Delay time, BCLK↑ to DATA(0:31) invalid	t_{d4}	C_L = 45 pF, T_A = 25°C See figure 4	All	9	4	24	ns
Phy-Interface Timing Requirements 2/							
Cycle time, SCLK	t_{c2}	T_A = 25°C, See figure 4	All	9	20.24	20.45	ns
Pulse duration, SCLK high	$t_{w2(H)}$	T_A = 25°C, See figure 4	All	9	9		ns
Pulse duration, SCLK low	$t_{w2(L)}$	T_A = 25°C, See figure 4	All	9	9		ns
Setup time, DATA(0:7) before SCLK↑	t_{su5}	T_A = 25°C, See figure 4	All	9	6		ns
Hold time, DATA(0:7) after SCLK↑	t_{h5}	T_A = 25°C, See figure 4	All	9	0		ns
Setup time, CTL(0:1) before SCLK↑	t_{su6}	T_A = 25°C, See figure 4	All	9	6		ns
Hold time, CTL(0:1) after SCLK↑	t_{h6}	T_A = 25°C, See figure 4	All	9	0		ns

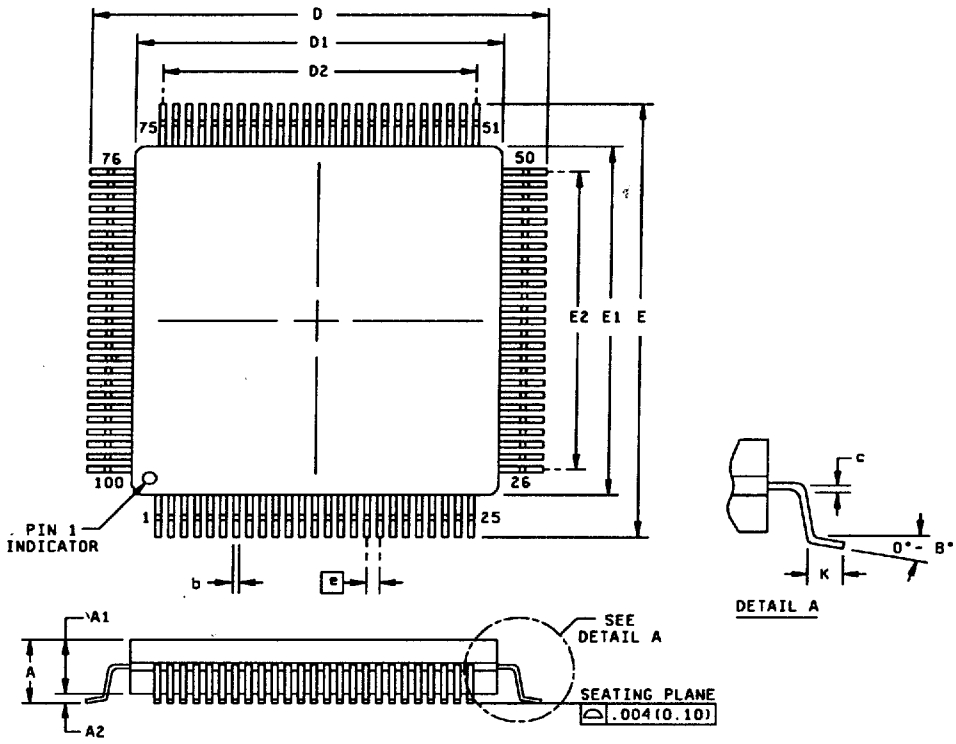
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.25\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Phy-Interface Switching Characteristics 2/							
Delay time, SCLK↑ to D(0:7) valid	t_{d5}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to D(0:7)	t_{d6}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to D(0:7) invalid	t_{d7}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to CTL(0:1) valid	t_{d8}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to CTL(0:1)	t_{d9}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to CTL(0:1) invalid	t_{d10}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Delay time, SCLK↑ to LREQ	t_{d11}	C_L = 45 pF, See figure 4 T_A = 25°C	All	9	3	14	ns
Miscellaneous Timing Requirements 2/							
Cycle time, CYCLEIN	t_{c3}	T_A = 25°C, See figure 4	All	9	124.99	125.01	µs
Pulse duration, CYCLEIN high	$t_{w3(H)}$	T_A = 25°C, See figure 4	All	9	62		µs
Pulse duration, CYCLEIN low	$t_{w3(L)}$	T_A = 25°C, See figure 4	All	9	62		µs
Miscellaneous Signal Switching Characteristics 2/							
Delay time, SCLK↑ to $\overline{TNT}$ low	t_{d12}	T_A = 25°C, See figure 4	All	9	4	18	ns
Delay time, SCLK↑ to $\overline{TNT}$ high	t_{d13}	T_A = 25°C, See figure 4	All	9	4	18	ns
Delay time, SCLK↑ to CYCLEOUT high	t_{d14}	T_A = 25°C, See figure 4	All	9	4	16	ns
Delay time, SCLK↑ to CYCLEOUT low	t_{d15}	T_A = 25°C, See figure 4	All	9	4	16	ns

1/ All outputs are in the high impedance state.

2/ All parameters are guaranteed but not tested at 25°C except t_{d1} and t_{d2}. t_{d1} and t_{d2} are tested at -55°C to 125°C.



Symbol	Dimensions			
	Min	Max	Min	Max
A		.160		4.07
A1	.140 NOM		3.56 NOM	
A2	.010		0.25	
b	.010 TYP		0.25 TYP	
c	.006 NOM		0.16 NOM	
D(E)	.875	.885	22.22	22.48
D1(E1)	.745	.755	18.92	19.18
D2(E2)	.600 TYP		15.25 TYP	
K	.020		0.51	
e	.025BSC		0.65BSC	

FIGURE 1. Case outline.

Device type	01				
Case outlines	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	34	$\overline{CS}$	67	LREQ
2	DATA16	35	$\overline{CA}$	68	$\overline{GND}$
3	DATA17	36	$\overline{WR}$	69	ISO
4	DATA18	37	$\overline{INT}$	70	GND
5	DATA19	38	$\overline{GND}$	71	NTBIHIZ
6	V_{CC}	39	$\overline{RESET}$	72	NTOUT
7	DATA20	40	GND	73	NTCLK
8	DATA21	41	GND	74	V_{CC}
9	DATA22	42	CYCLEIN	75	Reserved
10	DATA23	43	V_{CC}	76	POWERON
11	GND	44	CYCLEOUT	77	RAMEz
12	DATA24	45	GND	78	GND
13	DATA25	46	GND	79	GND
14	DATA26	47	GND	80	GND
15	DATA27	48	GRFEMP	81	GND
16	V_{CC}	49	CYDNE	82	DATA0
17	DATA28	50	CYST	83	DATA1
18	DATA29	51	GND	84	DATA2
19	DATA30	52	D7	85	DATA3
20	DATA31	53	D6	86	V_{CC}
21	GND	54	D5	87	DATA4
22	ADDR0	55	D4	88	DATA5
23	ADDR1	56	V_{CC}	89	DATA6
24	ADDR2	57	D3	90	DATA7
25	ADDR3	58	D2	91	GND
26	V_{CC}	59	D1	92	DATA8
27	ADDR4	60	D0	93	DATA9
28	ADDR5	61	GND	94	DATA10
29	ADDR6	62	CTL1	95	DATA11
30	ADDR7	63	CTL2	96	V_{CC}
31	GND	64	V_{CC}	97	DATA12
32	BCLK	65	SCLK	98	DATA13
33	V_{CC}	66	GND	99	DATA14
				100	DATA15

FIGURE 2. Terminal connections.

Host Bus Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR[0:7]	22-25 27-30	I	Address 0 through 7. Host bus address bus bits 0 through 7 that address the quadlet-aligned FIFOs and configuration registers. The two least significant address lines, 6 and 7, must be grounded.
$\overline{CA}$	35	O	Cycle acknowledge (active low). $\overline{CA}$ is a TSB12C01A control signal to the host bus. When asserted (low), access to the configuration registers or FIFO is complete.
$\overline{CS}$	34	I	Cycle start (active low). $\overline{CS}$ is a host bus control signal to enable access to the configuration register or FIFO.
DATA[0:31]	2-5 7-10 12-15 17-20 82-85 87-90 92-95 97-100	I/O	Data 0 through 31. DATA is a host bus data bus bits 1 through 31.
$\overline{TNT}$	37	O	Interrupt (active low). When $\overline{TNT}$ is asserted (low), the TSB12C01A notifies the host bus that an interrupt has occurred.
$\overline{WR}$	36	I	Read/$\overline{write}$ enable. When $\overline{WR}$ is deasserted (high) in conjunction with $\overline{CS}$, a read from the TSB12C01A is reguested. When $\overline{WR}$ is asserted (low) in conjuction with $\overline{CS}$, a write to the TSB12C01A is requested.

Phy Interface Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CTL1, CTL0	62, 63	I/O	Control 1 and control 0 of the phy-link control bus. CTL1 and CTL0 indicated the four operations that can occur in this interface (see annex J of the IEEE-1394 standard for more information about the four operations).
D[0-7]	52-55 57-60	I/O	Data 0 through data 7 of the phy-link data bus. Data is expected on D[0:1] for 100 Mb/s packets, D[0:3] for 200 Mb/s, and D[0:7] for 400Mb/s.
$\overline{TSO}$	69	I	Isolation barrier (active low). This $\overline{TSO}$ is asserted (low) when an isolation barrier is present.
LREQ	67	O	Link reguest. LREQ is a TSB12C01A output that makes bus reguests and accesses the phy layer.
SCLK	65	I	System clock. SCLK is a 49.152-MHz clock from the phy that generates the 24.576-MHz clock.

FIGURE 2. Terminal connections - continued.

Miscellaneous Signals Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCLK	32	I	Bus clock. BLCK is the host bus clock used in the host-interface module of the TSB12C01A. It is asynchronous to SCLK.
CYCLEIN	42	I	Cycle in. CYCLEIN is an optional external 8,000-Hz clock used as the cycle clock, and it should only be used when attached to the cycle-master node. It is enabled by the cycle source bit and should be tied hight when not used.
CYCLEOUT	44	O	Cycle out. CYCLEOUT is the TSB12C01A version of the cycle clock. It is based on the timer controls and received cycle-start messages.
CYDNE	49	O	Status of CyDne bit. When the RevAEn bit of the control register is set, CYDNE indicates the value of the CyDne bit of the interrupt register. When RevAEn is cleared, CYDNE is a 3-state output.
CYST	40	O	Status of CySt bit. When the RevAEn bit of the control register is set, CYST indicates the value of the CySt bit of the interrupt register. When RevAEn is cleared, CYST is a 3-state output.
GND	1, 11, 21, 31, 38, 40, 41, 45-47, 51, 61, 66, 68, 70, 78-81, 91		Ground reference
GRFEMP	48	O	Status of Empyt bit. When the RevAEn bit of the control register is set, GRFEMP indicates the value of the Empty bit of the GRF status register. When RevAEn is cleared, GRFEMP is a 3-state output.
RAMEz	77	I	RAM 3-state enable. When RAMEz is deasserted (low), FIFOs are enabled. When RAMEz is asserted, the FIFOs are 3-state outputs. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTBIHIZ	71	I	NAND-tree bidirectional 3-state output. When NTBIHIZ is deasserted (low), the bidirectional I/Os operate in a normal state. When BTBIHZ is asserted (high), the bidirectional I/Os are in the 3-state output mode. (This is a manufacturing test-mode condition and should be grounded under normal operating conditions.)
NTCLK	73	I	NAND clock input. The NAND-tree clock is used for V_{IH} and V_{IL} manufacturing tests. (This input should be grounded under notrmal operating conditions.)
RESET	39	I	Reset (active low). RESET is the asynchronous reset to the TSB12C01A.
POWERON	76	O	Power on indicator to phy interface. When active, POWERON has a clock output with 1/32 of the BCLK frequency and indicates to the phy interface that the TSB12C0A is powered.
V_{CC}	6, 16, 26, 33, 43, 56, 64, 74, 86, 96		5-V ±5% power supplies

FIGURE 2. Terminal connections - continued.

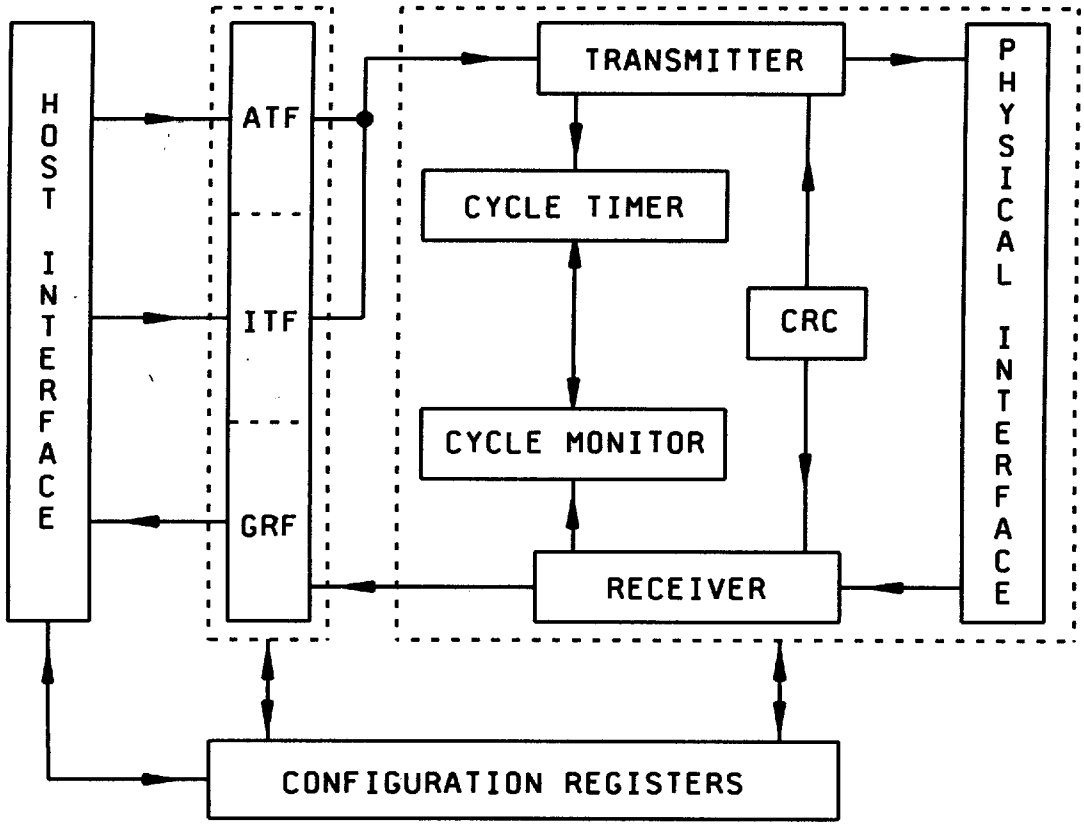
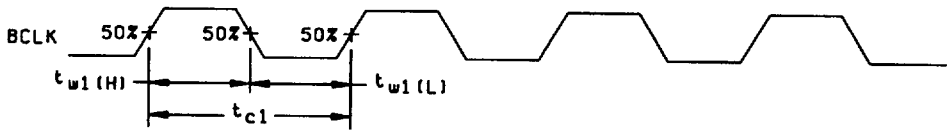
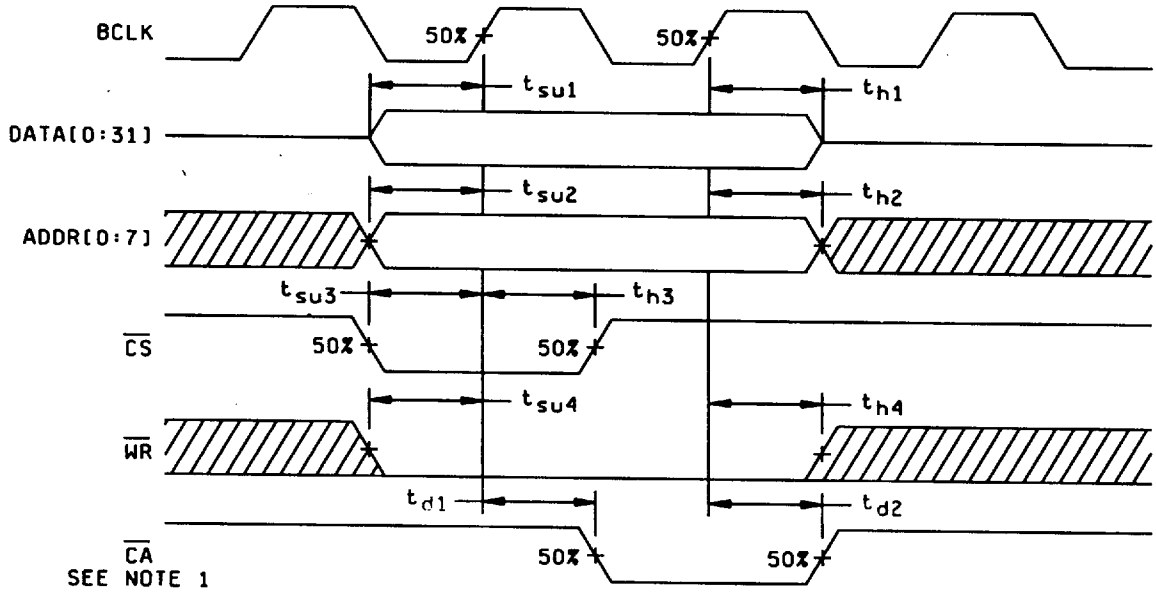


FIGURE 3. Block diagram.

BCLK Waveform



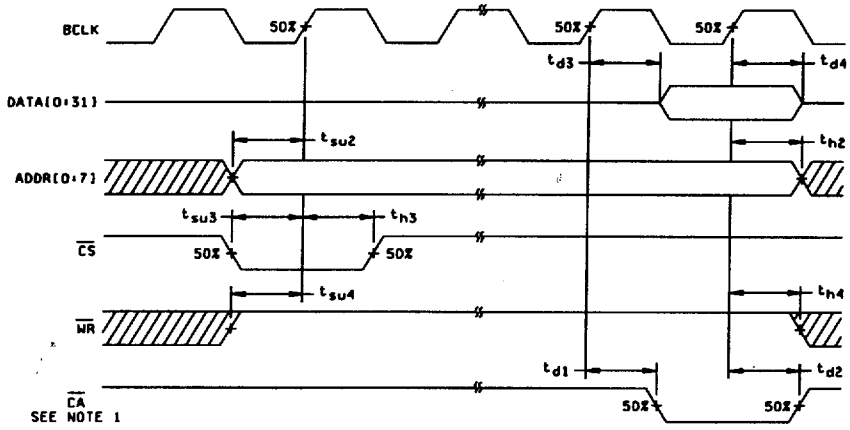
Host-Interface Write-Cycle Waveforms



1/ When back-to-back write cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of $\overline{CS}$ before $\overline{CA}$ is asserted (low) DATA[0:31], ADDR[0:7], and $\overline{WR}$ need to remain valid until $\overline{CA}$ is asserted (low).

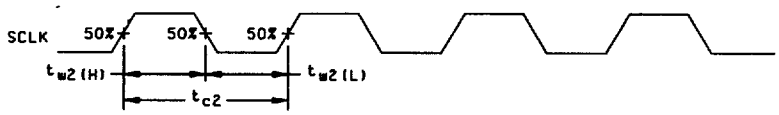
FIGURE 4. Timing waveforms.

Host-Interface Read-Cycle Waveform



1/ When back-to-back read cycles are done, a maximum of 9 BCLK cycles may be required after the falling edge of the $\overline{CS}$ before CA is asserted (low). ADDR[0:7] and WR need to remain valid until CA is asserted (low).

SCLK Waveform



TSB12C01A-to-Phy Layer Transfer Waveform

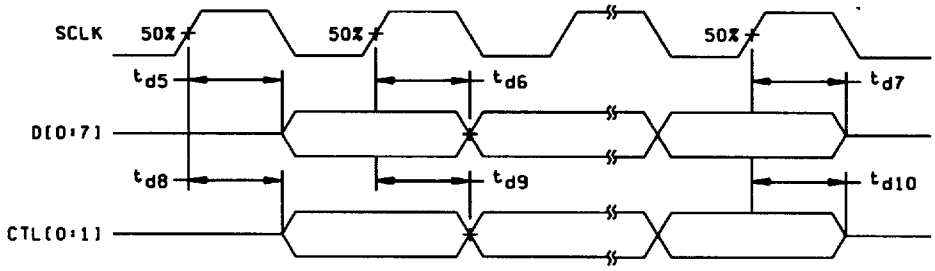
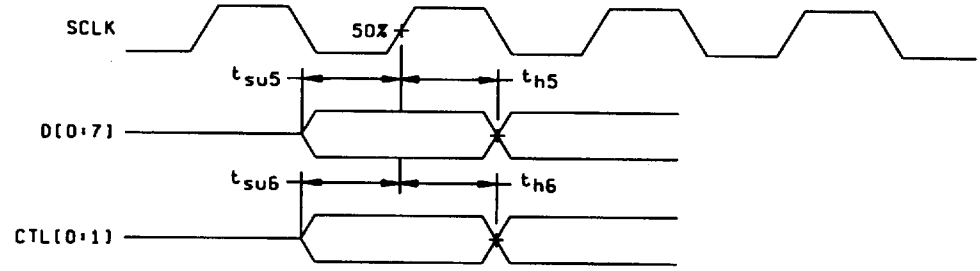
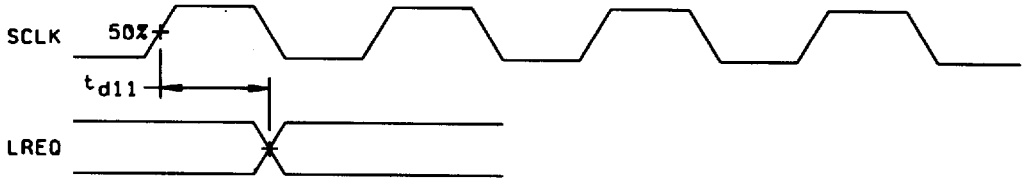


FIGURE 4. Timing Waveforms - Continued.

Phy-layer-to-TSB12C01A Transfer Waveform



TSB12C01A-Link-Request-to-Phy-Layer Waveform



Interrupt Waveform

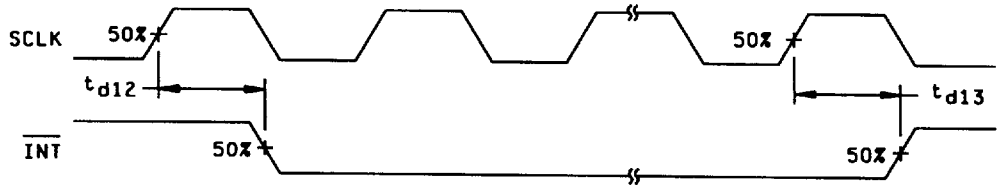


FIGURE 4. Timing Waveforms - Continued.

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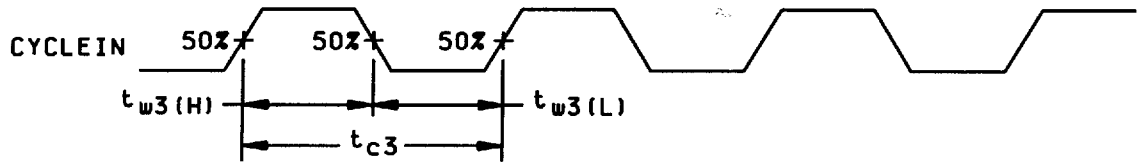
CYCLEIN Waveform



CYCLEIN and CYCLEOUT Waveforms

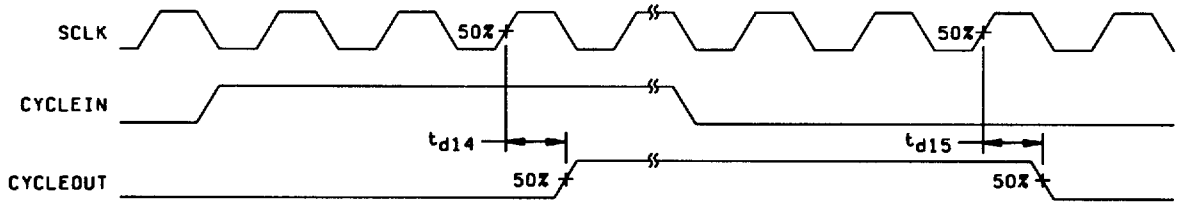


FIGURE 4. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, $C_{I/O}$, and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND. Sample size is five devices with no failures. Worst-case input, output, and bi-directional terminals shall be tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3 1/ 9, 10, 11	1, 2, 3 1/ 9, 10, 11	1, 2, 3 1/ 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3 9, 10, 11	1, 2, 3 9, 10, 11	1, 2, 3 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.