

August 2006

HI-8591

ARINC 429 LINE RECEIVER

DESCRIPTION

The HI-8591 is an ARINC 429 bus interface receiver designed to operate from a single 3.3 V or 5 V supply. The part is designed with high-impedance inputs to minimize bus loading, and has an exceptional input common-mode performance in excess of +/- 30V, making it immune to ground offsets around the aircraft. The RINA and RINB inputs of the standard HI-8591 may be connected directly to the ARINC 429 bus. To enable external lightning protection circuitry to be added, the HI-8591-40 variant is available. The HI-8591-40 requires only the addition of external 40 K Ω , 1/4 watt resistors in series with RINA and RINB to allow the part to meet the lightning protection requirements of DO-160D level 3.

The typical 10 volt differential ARINC 429 signal is translated and input to a window comparator and latch. The comparator levels are set just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

The TESTA and TESTB inputs bypass the analog inputs for testing purposes. Also if TESTA and TESTB are both taken high, the digital outputs are forced to zero.

See Holt Application Note AN-300 for more information on lightning protection.

FEATURES

- ARINC 429 line receiver interface in a small outline package
- 3.3V single rail supply voltage
- +/-30 V common-mode performance
- >140 KOhm input impedance
- Lightning protection simplified with the ability to add 40 KOhm external series resistors
- Receiver input hysteresis at least 2 volt
- Test inputs bypass analog inputs and force digital outputs to a one, zero or null state

PIN CONFIGURATIONS



HI-8591PSI, HI-8591PST & HI-8591PSM HI-8591PSI-40, HI-8591PST-40 & HI-8591PSM-40 8 - PIN PLASTIC NARROW BODY SOIC



HI-8591PCI, HI-8591PCT, HI-8591PCI-40 & HI-8591PCT-40 16- pin 4mm x 4mm Chip-scale package

SUPPLY VOLTAGES

VCC = 3.3V ± 10%, 5.0V ± 10%

FUNCTION TABLE

RINA	RINB	TESTA	TESTB	ROUTA	ROUTB
-1.25V to 1.25V	-1.25V to 1.25V	0	0	0	0
-3.25V to -6.5V	3.25V to 6.5V	0	0	0	1
3.25V to 6.5V	-3.25V to -6.5V	0	0	1	0
Х	Х	0	1	0	1
Х	Х	1	0	1	0
Х	Х	1	1	0	0

PIN DESCRIPTION TABLE

SYMBOL	FUNCTION	DESCRIPTION
VCC	SUPPLY	3.3V or 5V SUPPLY
TESTA	LOGIC INPUT	CMOS
RINB	ARINC INPUT	RECEIVER B INPUT
RINA	ARINC INPUT	RECEIVER A INPUT
GND	POWER	GROUND
ROUTA	LOGIC OUTPUT	RECEIVER CMOS OUTPUT A
ROUTB	LOGIC OUTPUT	RECEIVER CMOS OUTPUT B
TESTB	LOGIC INPUT	CMOS

FUNGTIONAL DESCRIPTION

RECEIVER

Figure 1 shows the general architecture of the ARINC 429 receiver. The receiver operates off the VCC supply only. The inputs RINA and RINB each require $140K\Omega$ of resistance between the ARINC bus and comparator. This resistance is completely on-chip for the HI-8591. In contrast, the HI-8591-40 has 100 K Ω on-chip and requires an external $40K\Omega$, $\frac{1}{4}$ watt resistor on each of the ARINC 429 input pins. The HI-8591-40 device is typically chosen for applications where lightning protection is a requirement.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between V.C. and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0 V and a Null amplitude of 3.3 V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins. If TESTA and TESTB are both One, the HI-8591 outputs are pulled low. This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for system self-test purposes.





Figure 2 shows a possible application of the HI-8591 interfacing an ARINC 429 bus input to a 3.3V ASIC or FPGA. In this example a HI-8586 ARINC 429 line driver is used to take 3.3V logic outputs and generate the necessary 10V differential signal for driving an ARINC 429 bus.



HOLT INTEGRATED CIRCUITS 2

ABSEDEUTE:MAXIMUMIRANINGS

Voltages referenced to Ground

Supply voltages VCC0.3V to +7V
ARINC input - pins 3 & 4 Voltage at either pin+120V to -120V
DC current per input pin ±10mA
Power dissipation at 25°C plastic DIP0.7W ceramic DIP0.5W
Solder Temperature275°C for 10 sec
Storage Temperature65°C to +150°C

DC ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Supply Voltages VCC3.3V to 5V ± 10%
Temperature Range Industrial Screening40°C to +85°C Hi-Temp Screening55°C to +125°C Military Screening55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

OPERATING TEMPERATURE RANGE,	VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
ARINC input voltage one or zero null common mode	V _{DIN} V _{NIN} V _{COM}	Differential volt., pins 3 & 4 """" with respect to ground	6.5 - -30.0	10 - -	13 2.5 +30.0	volts volts volts
logic input voltage high low	V _{IH} V _{IL}		70% VCC -	-	- 30% VCC	volts volts
ARINC input resistance RINA to RINB RINA or RINB to GND RINA or RINB to VCC	R DIFF R GND R VCC	Supplies floating "" ""	- - -	140 140 100	- - -	ΚΩ ΚΩ ΚΩ
logic input current source sink	lıH lı∟	V _{IN} = 2.0V V _{IN} = 0.8V	-	-	20.0 20.0	μΑ μΑ
logic output drive voltage one zero	V _{OH1} V _{OH2} V _{OL1}	VCC = $5V \pm 10\%$ I _{OH} = $5mA$ VCC = $3.3V \pm 10\%$ I _{OH} = $1.5mA$ VCC = $5V \pm 10\%$ I _{OH} = $5mA$	2.4 2.4 -	-	0.5	V V V
Current drain operating	ICC1	pins 2, 8 = 0V; pins 3, 4 open	-	1.5	5.0	mA

HI-8591

AC ELECTRICAL CHARAGE TERISTICS OPERATING TEMPERATURE RANGE, VCC = 3.3V ± 10% or 5.0V ± 10% UNLESS OTHERWISE STATED

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
Receiver propagation delay		defined in Figure 3, C _I = 50pF				
Output high to low	t phlr	VCC = 3.3V ± 10%	-	600	1000	ns
		VCC = 5.0V ± 10%	-	600	900	ns
Output low to high	t plhr	VCC = 3.3V ± 10%	-	600	1000	ns
		VCC = 5.0V ± 10%	-	600	900	ns
TEST pin propagation delay		defined in Figure 4, C _I = 50pF				
Output high to low	t pth	VCC = 3.3V ± 10%	-	-	100	ns
		VCC = 5.0V ± 10%	-	-	60	ns
Output low to high	t ptl	VCC = 3.3V ± 10%	-	-	100	ns
		VCC = 5.0V ± 10%	-	-	60	ns
Receiver output transition times		VCC = 3.3V or 5.0V ± 10%				
Output high to low	t _{fr}		-	15	50	ns
Output low to high	t rr		-	15	50	ns
Input capacitance (1)						
ARINC differential	C _{AD}		-	5	10	рF
ARINC single ended to Ground	C _{AS}		-	-	10	рF
Logic	CIN		-	-	10	pF

Notes: 1. Guaranteed but not tested



HOLT INTEGRATED CIRCUITS

查询"HI-8591PSM-40"供应商 ORDERING INFORMATION

HI	-	8591	ХХ	Х	Х	- XX
				Т	Т	

PART	INPUT SERIES RESISTANCE				
NUMBER	BUILT-IN	REQUIRED EXTERNALLY			
No dash number	140 Kohm	0			
-40	100 Kohm	40 K	ohm		
PART NUMBER	LEAD FINISH	AD NISH			
Blank	Tin / Lead (Sn / Pb) \$	Solder		
F	100% Matte	e Tin (Pb-	free, RoH	IS compliant)	
NUMBER	RANGE	FURE	FLOW	BURN IN	
I	-40°C TO	+85°C	I	NO	
Т	-55°C TO ·	+125°C	Т	NO	
М	-55°C TO	+125°C	М	YES	
 PART NUMBER	PACKAGE DESCRIPT	PACKAGE DESCRIPTION			
PC	8 PIN PLASTIC 4 X 4 mm CHIP SCALE (not available with "M" f				
PD	8 PIN PLASTIC DIP (not available with "M" flow)				
PS	8 PIN PLASTIC NARROW BODY SOIC				
CR	8 PIN CERE	3 PIN CERDIP (not available Pb-free)			

inches (millimeters)



HOLT INTEGRATED CIRCUITS 6

HI-8591 PACKAGE DIMENSIONS

