查询"ADA4898-2"供应商

High Voltage, Low Noise, Low Distortion, Unity-Gain Stable, High Speed Op Amp

ADA4898-1/ADA4898-2

FEATURES

Ultralow noise
- **0.9 nV/√Hz**
- **2.4 pA/√Hz**
- **1.2 nV/√Hz at 10 Hz**

Ultralow distortion: −93 dBc at 500 kHz
Wide supply voltage range: ±5 V to ±16 V
High speed
- **−3 dB bandwidth: 65 MHz (G = +1)**
- **Slew rate: 55 V/µs**

Unity gain stable
Low input offset voltage: 160 µV maximum
Low input offset voltage drift: 1 µV/°C
Low input bias current: −0.1 µA
Low input bias current drift: 2 nA/°C
Supply current: 8 mA
Power-down feature for single 8-lead package

APPLICATIONS

Instrumentation
Active filters
DAC buffers
SAR ADC drivers
Optoelectronics

GENERAL DESCRIPTION

The ADA4898 is an ultralow noise and distortion, unity gain stable, voltage feedback op amp that is ideal for use in 16-bit and 18-bit systems with power supplies from ±5 V to ±16 V. The ADA4898 features a linear, low noise input stage and internal compensation that achieves high slew rates and low noise.

With the wide supply voltage range, low offset voltage, and wide bandwidth, the ADA4898 is extremely versatile, and it features a cancellation circuit that reduces input bias current.

The ADA4898 is available in an 8-lead SOIC package that features an exposed metal paddle to improve power dissipation and heat transfer to the negative supply plane. This EPAD offers a significant thermal relief over traditional plastic packages. The ADA4898 is rated to work over the extended industrial temperature range of −40°C to +105°C.

CONNECTION DIAGRAM

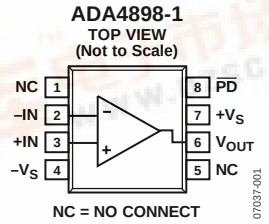

Figure 1. Single 8-Lead ADA4898-1 SOIC_N_EP (RD-8-1)

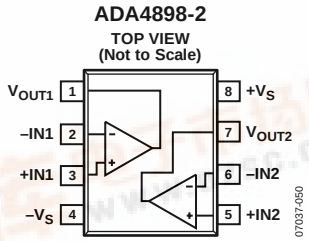

Figure 2. Dual 8-Lead ADA4898-2 SOIC_N_EP (RD-8-1)

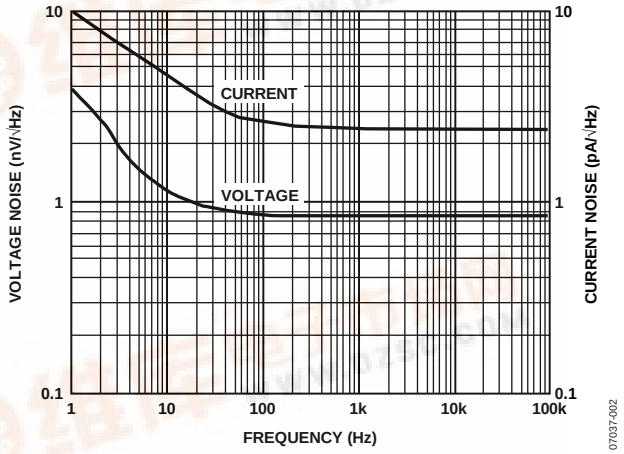

Figure 3. Input Voltage Noise and Current Noise vs. Frequency

Rev. C

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REVISION HISTORY

1/10—Rev. B to Rev. C

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5/08—Revision 0: Initial Release

SPECIFICATIONS

±15 V SUPPLY

T_A = 25°C, G = +1, R_F = 0 Ω, R_G open, R_L = 1 kΩ to GND (for G > 1, R_F = 100 Ω), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 100 mV p-p		65		MHz
	V_{OUT} = 2 V p-p		14		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p		3.3		MHz
Slew Rate	V_{OUT} = 5 V step		55		V/µs
Settling Time to 0.1%	V_{OUT} = 5 V step		85		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion SFDR	f = 100 kHz, V_{OUT} = 2 V p-p		−116		dBc
	f = 500 kHz, V_{OUT} = 2 V p-p		−93		dBc
	f = 1 MHz, V_{OUT} = 2 V p-p		−79		dBc
Input Voltage Noise	f = 1 kHz		0.9		nV/√Hz
Input Current Noise	f = 1 kHz		2.4		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	R_F = 1 kΩ, see Figure 43		20	125	µV
Input Offset Voltage Drift	R_F = 1 kΩ, see Figure 43		1		µV/°C
Input Bias Current	R_F = 1 kΩ, see Figure 43		−0.1	−0.4	µA
Input Bias Offset Current	R_F = 1 kΩ, see Figure 43		0.03	0.3	µA
Input Bias Current Drift	R_F = 1 kΩ, see Figure 43		2		nA/°C
Open-Loop Gain	V_{OUT} = ±5 V	99	103		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		5		kΩ
	Common mode		30		MΩ
Input Capacitance	Differential mode		3.2		pF
	Common mode		2.5		pF
Input Common-Mode Voltage Range	See Figure 43		±11		V
Common-Mode Rejection Ratio	V_{CM} = ±2 V	−103	−126		dB
$\overline{PD}$ (POWER-DOWN) PIN (ADA4898-1)					
$\overline{PD}$ Input Voltages	Chip powered down		≤−14		V
	Chip enabled		≥−13		V
$\overline{PD}$ Turn On Time	V_{OUT} = 100 mV p-p		100		ns
$\overline{PD}$ Turn Off Time	V_{OUT} = 100 mV p-p		20		µs
Input Leakage Current	$\overline{PD}$ = +V_S		0.1		µA
	$\overline{PD}$ = −V_S		−0.2		µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L // (R_F + R_G) = 500 Ω, see Figure 43	−11.0 to +11.8	−11.7 to +12.1		V
	R_L // (R_F + R_G) = 1 kΩ, see Figure 43	−12.5 to +12.5	−12.8 to +12.7		V
Linear Output Current	f = 100 kHz, SFDR = −70 dBc, R_L = 150 Ω		40		mA
Short-Circuit Current	Sinking/sourcing		150		mA
Off Isolation	f = 1 MHz, $\overline{PD}$ = −V_S		80		dB
POWER SUPPLY					
Operating Range		±4.5		±16.5	V
Quiescent Current per Amplifier	$\overline{PD}$ = +V_S		7.9	8.7	mA
	$\overline{PD}$ = −V_S		0.1	0.3	mA
Positive Power Supply Rejection Ratio	+V_S = 15 V to 17 V, −V_S = −15 V	−98	−107		dB
Negative Power Supply Rejection Ratio	+V_S = 15 V, −V_S = −15 V to −17 V	−100	−114		dB

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±5 V SUPPLY

T_A = 25°C, G = +1, R_F = 0 Ω, R_G open, R_L = 1 kΩ to GND (for G > 1, R_F = 100 Ω), unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 100 mV p-p		57		MHz
	V_{OUT} = 2 V p-p		12		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p		3		MHz
Slew Rate	V_{OUT} = 2 V step		50		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		90		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion SFDR	f = 100 kHz, V_{OUT} = 2 V p-p		−110		dBc
	f = 500 kHz, V_{OUT} = 2 V p-p		−95		dBc
	f = 1 MHz, V_{OUT} = 2 V p-p		−78		dBc
Input Voltage Noise	f = 1 kHz		0.9		nV/√Hz
Input Current Noise	f = 1 kHz		2.4		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	R_F = 1 kΩ, see Figure 43		30	160	µV
Input Offset Voltage Drift	R_F = 1 kΩ, see Figure 43		1		µV/°C
Input Bias Current	R_F = 1 kΩ, see Figure 43		−0.1	−0.5	µA
Input Bias Offset Current	R_F = 1 kΩ, see Figure 43		0.05	0.3	µA
Input Bias Current Drift	R_F = 1 kΩ, see Figure 43		2		nA/°C
Open-Loop Gain	V_{OUT} = ±1 V	87	94		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		5		kΩ
	Common mode		30		MΩ
Input Capacitance	Differential mode		3.2		pF
	Common mode		2.5		pF
Input Common-Mode Voltage Range	See Figure 43		−3 to +2.5		V
Common-Mode Rejection Ratio	ΔV_{CM} = 1 V p-p	−102	−120		dB
$\overline{PD}$ (POWER-DOWN) PIN (ADA4898-1)					
$\overline{PD}$ Input Voltages	Chip powered down		≤−4		V
	Chip enabled		≥−3		V
$\overline{PD}$ Turn On Time	V_{OUT} = 100 mV p-p		100		ns
$\overline{PD}$ Turn Off Time	V_{OUT} = 100 mV p-p		20		µs
Input Leakage Current	$\overline{PD}$ = +V_S		0.1		µA
	$\overline{PD}$ = −V_S		−2		µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L // (R_F + R_G) = 500 Ω, see Figure 43	±3.1	±3.2		V
	R_L // (R_F + R_G) = 1 kΩ, see Figure 43	±3.3	±3.4		V
Linear Output Current	f = 100 kHz, SFDR = −70 dBc, R_L = 150 Ω		8		mA
Short-Circuit Current	Sinking/sourcing		150		mA
Off Isolation	f = 1 MHz, $\overline{PD}$ = −V_S		80		dB
POWER SUPPLY					
Operating Range		±4.5		±16.5	V
Quiescent Current Per Amplifier	$\overline{PD}$ = +V_S		7.5	8.4	mA
	$\overline{PD}$ = −V_S		0.1	0.2	mA
Positive Power Supply Rejection Ratio	+V_S = 5 V to 7 V, −V_S = −5 V	−95	−100		dB
Negative Power Supply Rejection Ratio	+V_S = 5 V, −V_S = −5 V to −7 V	−97	−104		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Power Dissipation	See Figure 4
Differential Mode Input Voltage	±1.5 V
Common-Mode Input Voltage	±11.4 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface that is thermally connected to a copper plane, with zero airflow.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
Single 8-Lead SOIC_N_EP on a 4-Layer Board	47	29	°C/W
Dual 8-Lead SOIC_N_EP on a 4-Layer Board	42	29	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4898 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4898. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the output load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 4 shows the maximum power dissipation vs. the ambient temperature for the single and dual 8-lead SOIC_N_EP on a JEDEC standard 4-layer board, with its underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

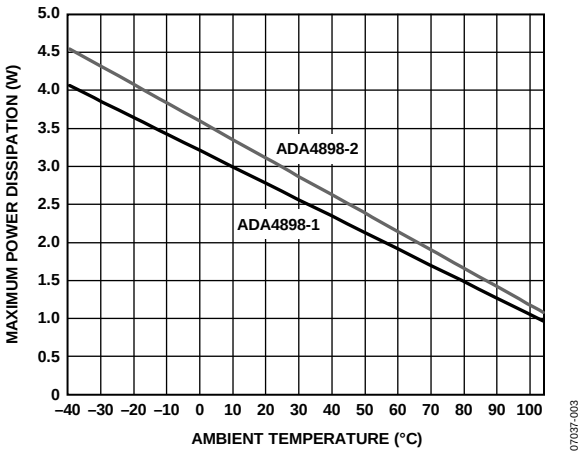

Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

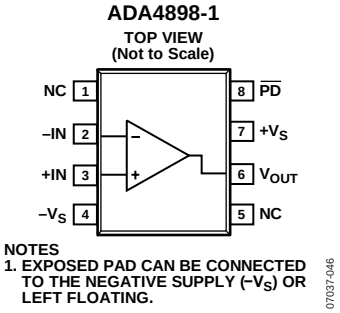

Figure 5. Single 8-Lead SOIC_N_EP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
5	NC	No Connect.
6	V_{OUT}	Output.
7	$+V_S$	Positive Supply.
8	$\overline{PD}$	Power Down Not.
	EP	Exposed Pad. Can be connected to the negative supply ($-V_S$) or can be left floating.

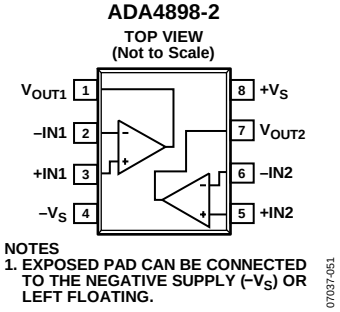

Figure 6. Dual 8-Lead SOIC_N_EP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT1}	Output 1.
2	–IN1	Inverting Input 1.
3	+IN1	Noninverting Input 1.
4	$-V_S$	Negative Supply.
5	+IN2	Noninverting Input 2.
6	–IN2	Inverting Input 2.
7	V_{OUT2}	Output 2.
8	$+V_S$	Positive Supply.
	EP	Exposed Pad. Can be connected to the negative supply ($-V_S$) or can be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

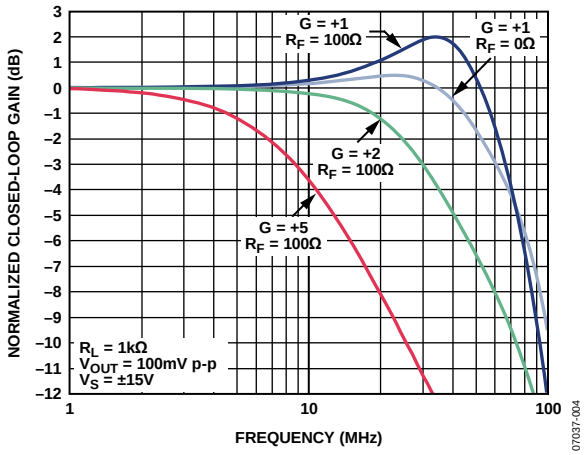

Figure 7. Small Signal Frequency Response for Various Gains

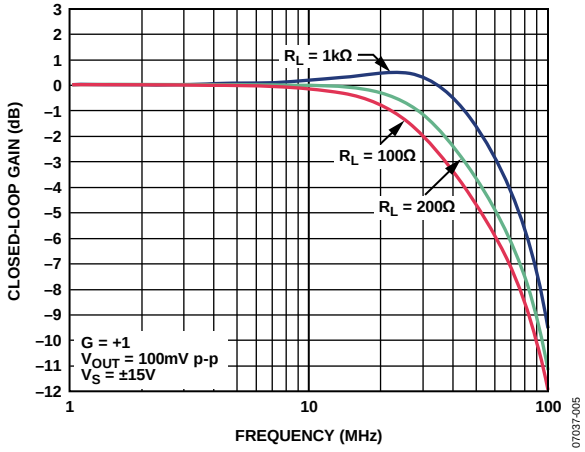

Figure 8. Small Signal Frequency Response for Various Loads

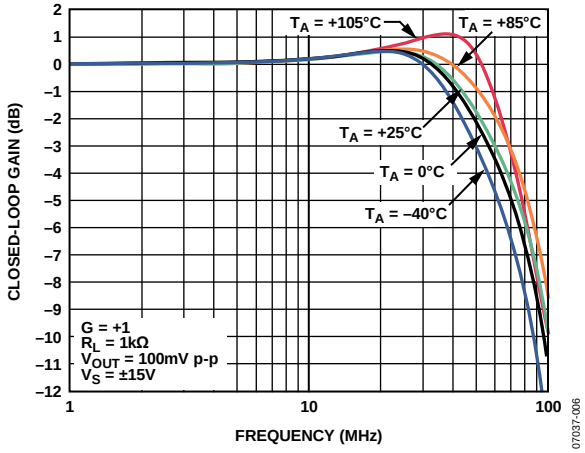

Figure 9. Small Signal Frequency Response for Various Temperatures

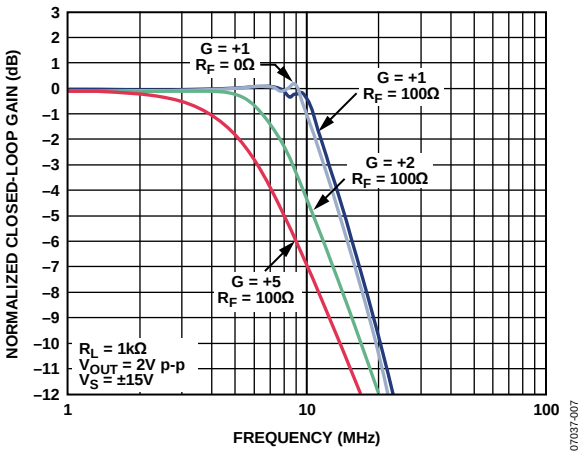

Figure 10. Large Signal Frequency Response for Various Gains

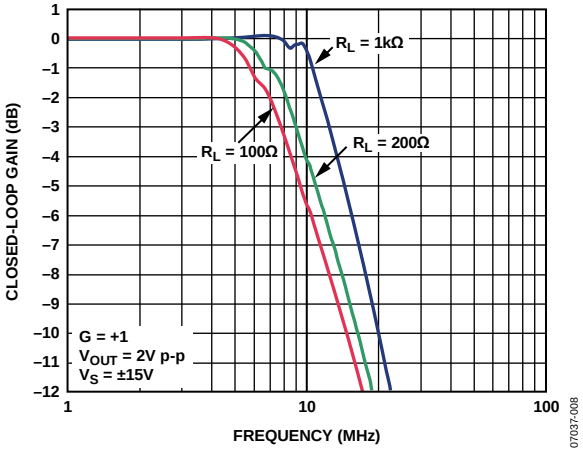

Figure 11. Large Signal Frequency Response for Various Loads

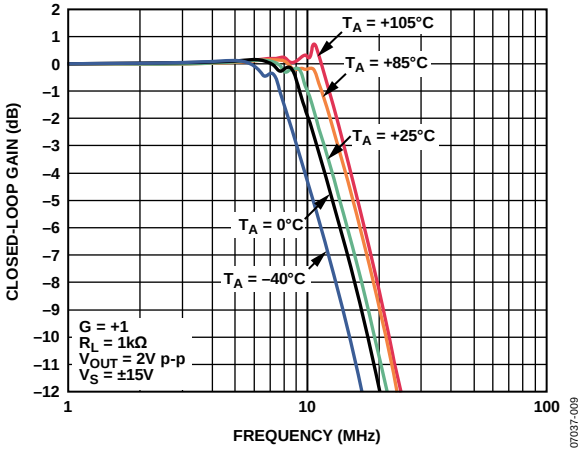

Figure 12. Large Signal Frequency Response for Various Temperatures

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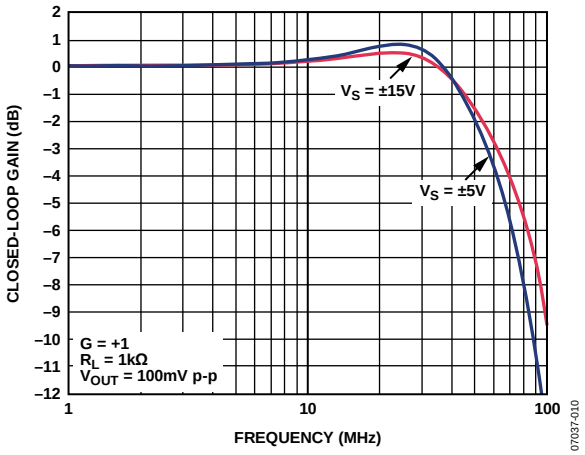

Figure 13. Small Signal Frequency Response for Various Supply Voltages

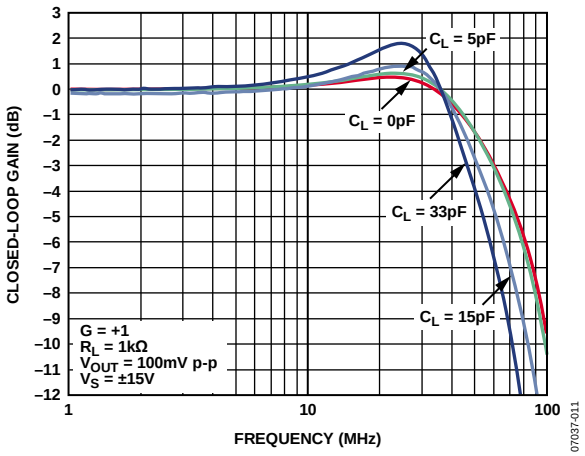

Figure 14. Small Signal Frequency Response for Various Capacitive Loads

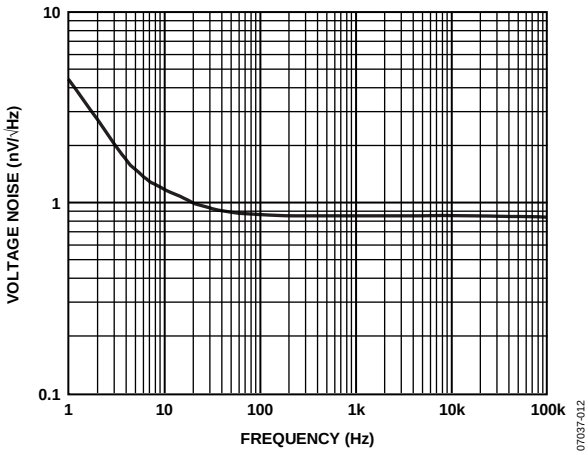

Figure 15. Voltage Noise vs. Frequency

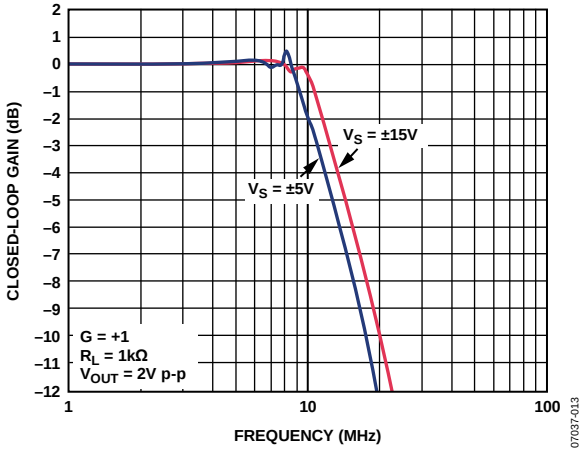

Figure 16. Large Signal Frequency Response for Various Supply Voltages

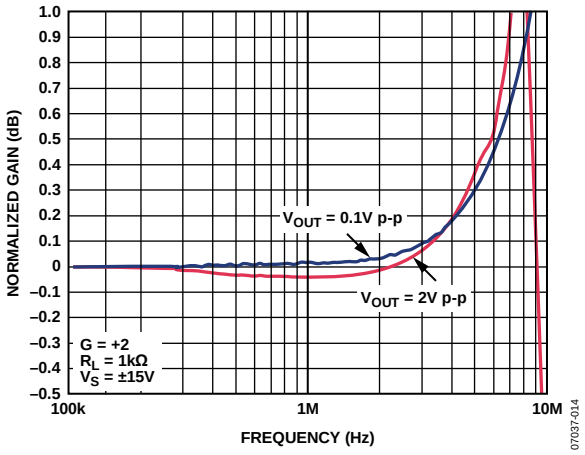

Figure 17. 0.1 dB Flatness for Various Output Voltages

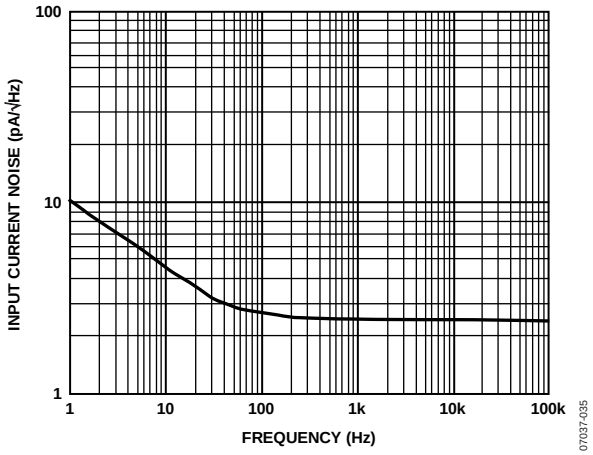

Figure 18. Input Current Noise vs. Frequency

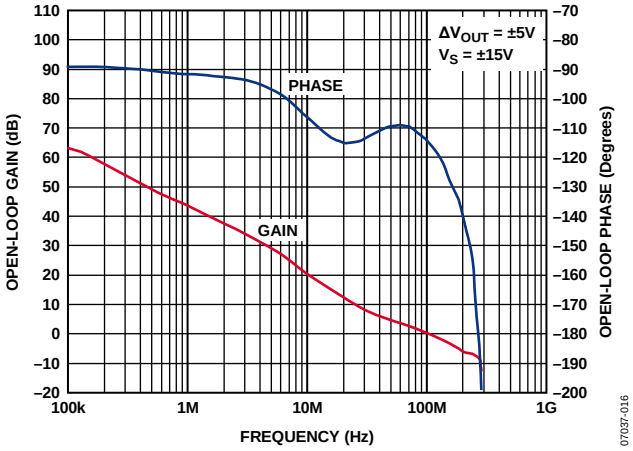

Figure 19. Open-Loop Gain and Phase vs. Frequency

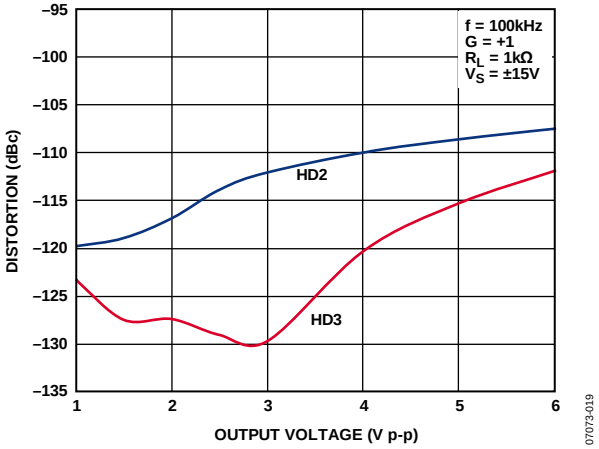

Figure 22. Harmonic Distortion vs. Output Amplitude

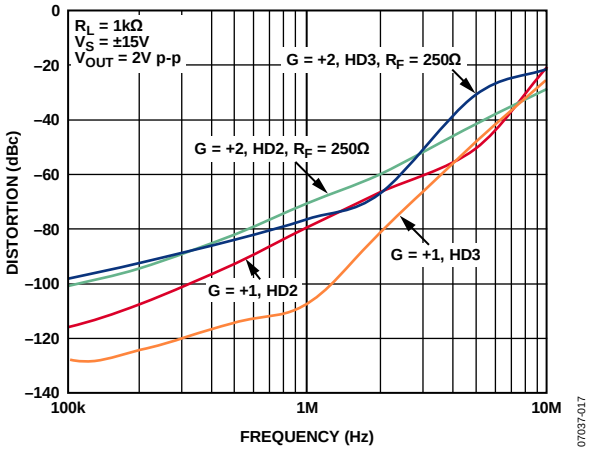

Figure 20. Harmonic Distortion vs. Frequency and Gain

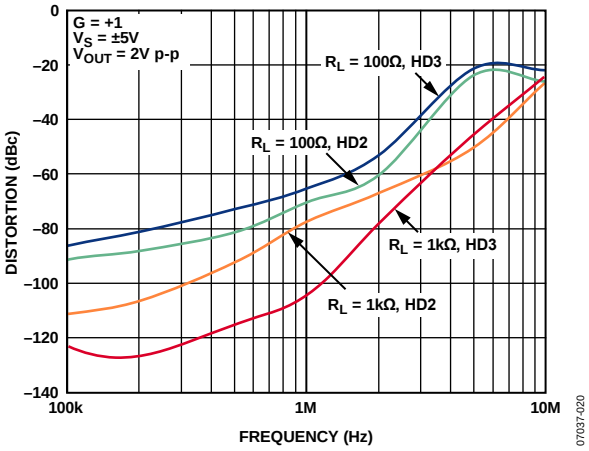

Figure 23. Harmonic Distortion vs. Frequency and Loads

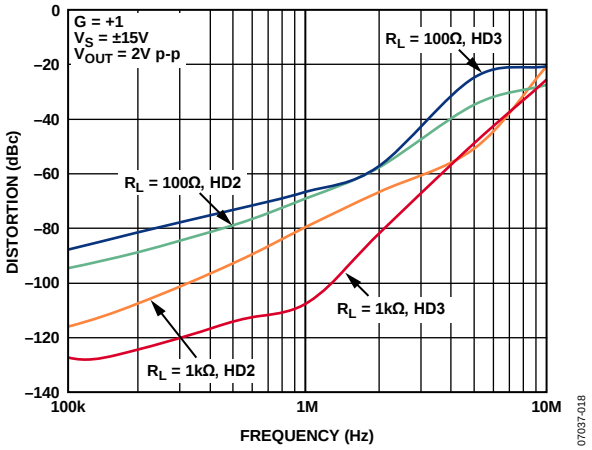

Figure 21. Harmonic Distortion vs. Frequency and Loads

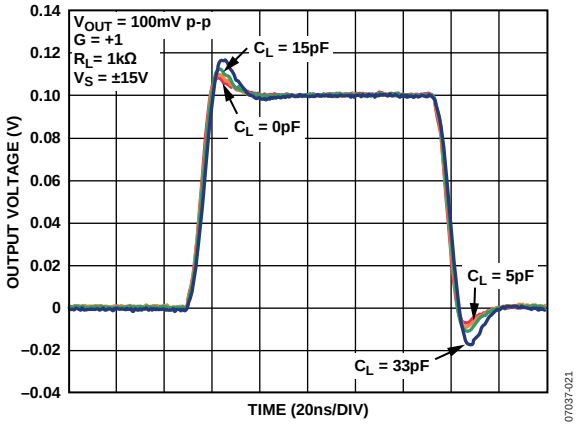

Figure 24. Small Signal Transient Response for Various Capacitive Loads

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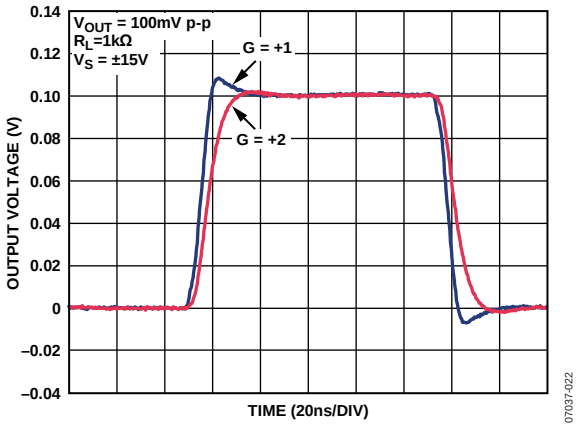

Figure 25. Small Signal Transient Response for Various Gains

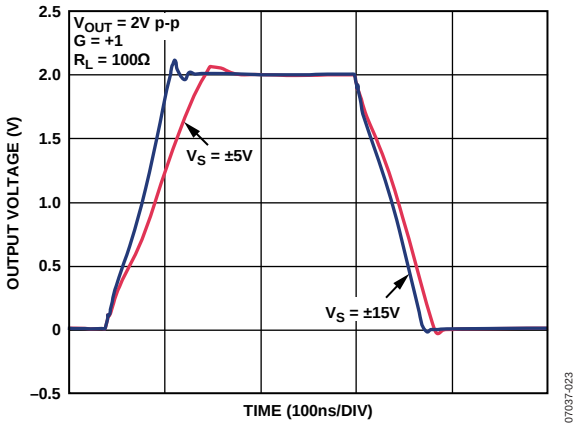

Figure 26. Large Signal Transient Response for Various Supply Voltages, R_L = 100 Ω

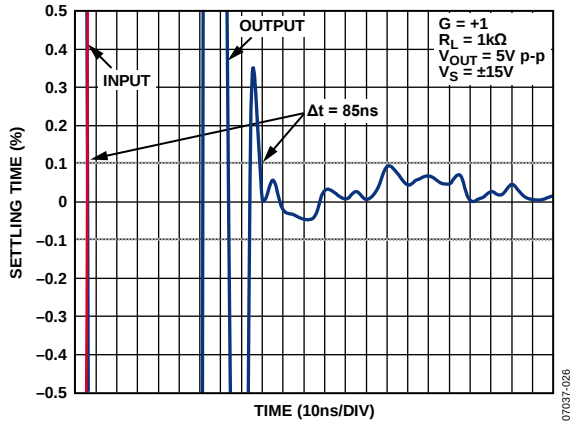

Figure 27. Settling Time

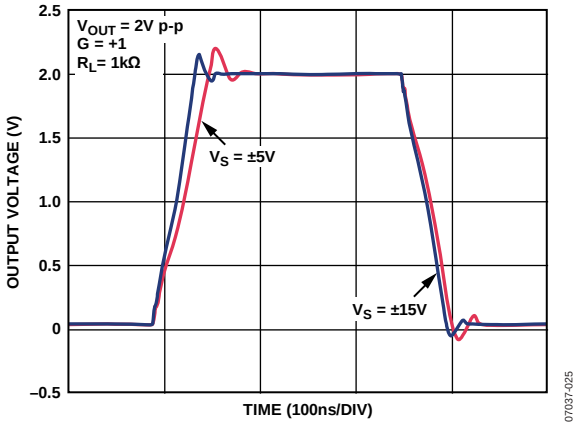

Figure 28. Large Signal Transient Response for Various Supply Voltages, R_L = 1 kΩ

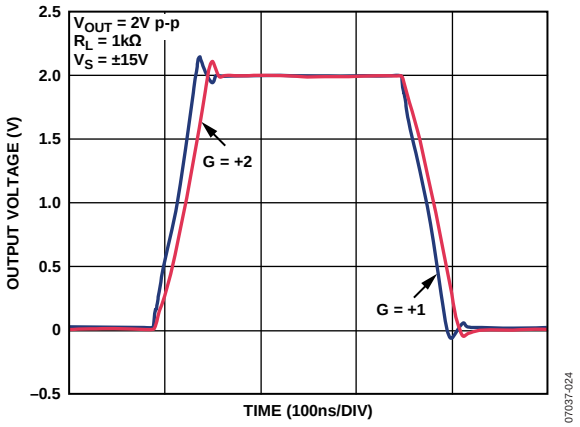

Figure 29. Large Signal Transient Response for Various Gains

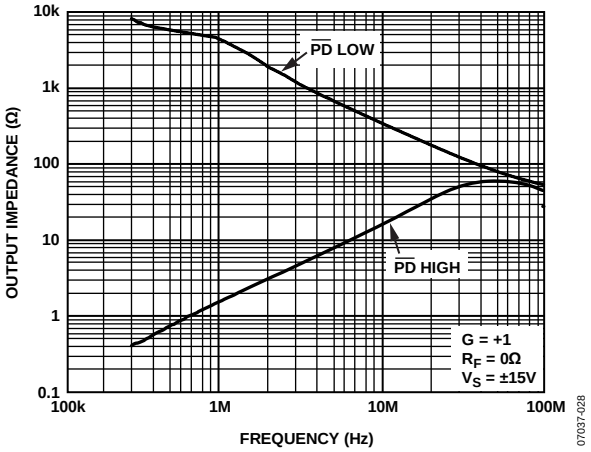

Figure 30. Output Impedance vs. Frequency

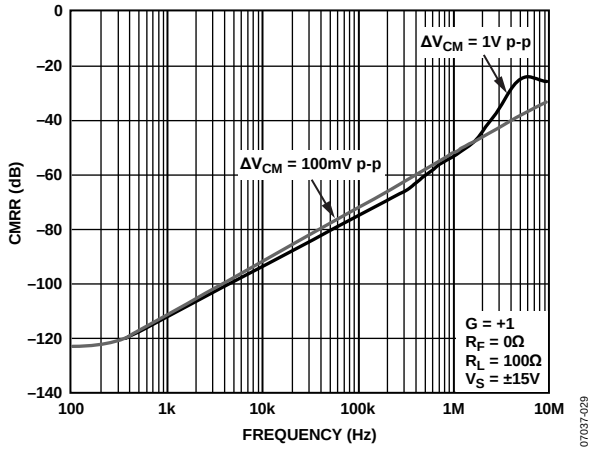

Figure 31. Common-Mode Rejection Ratio (CMRR) vs. Frequency

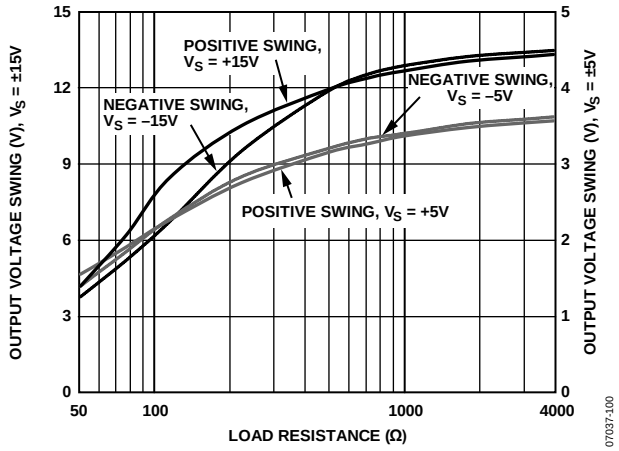

Figure 34 Output Swing vs. Load, G = +2, Load = R_L // (R_F + R_G)

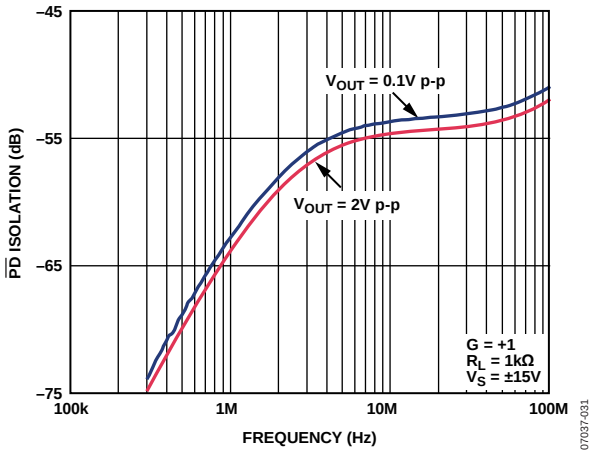

Figure 32. $\overline{PD}$ Input to Output Isolation vs. Frequency

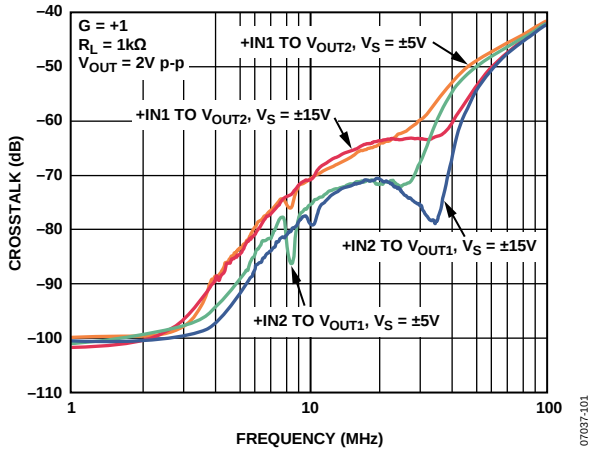

Figure 35. Crosstalk vs. Frequency

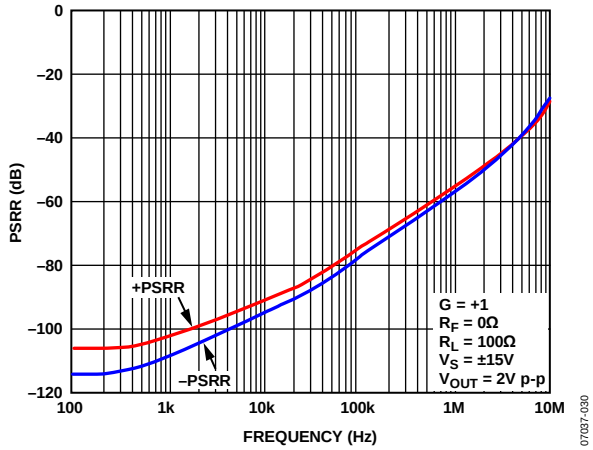

Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency

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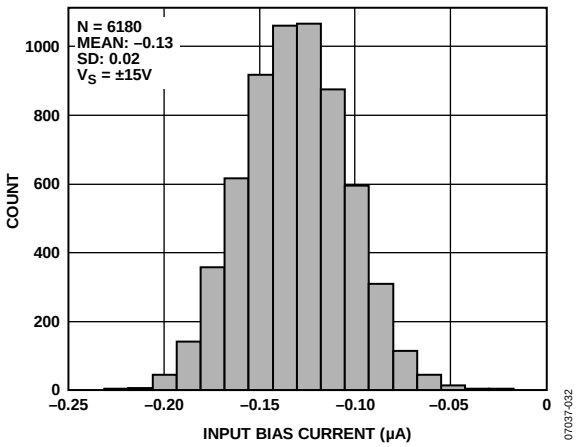

Figure 36. Input Bias Current Distribution

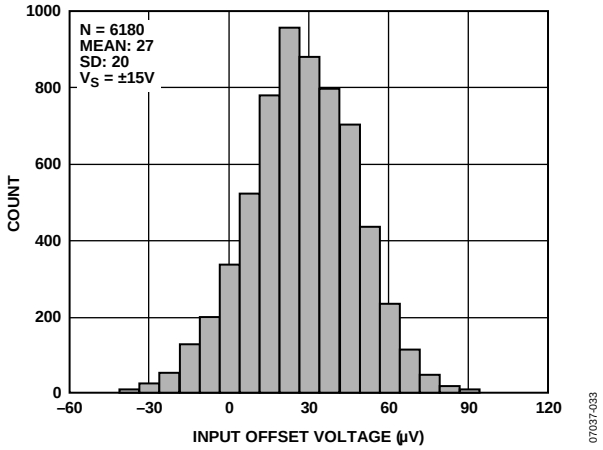

Figure 37. Input Offset Voltage Distribution, $V_S = \pm 15$ V

TEST CIRCUITS

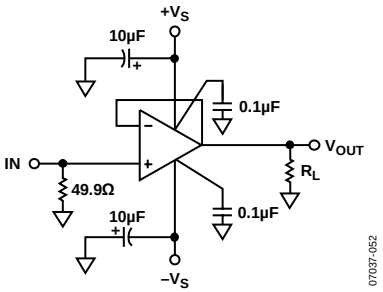

Figure 38. Typical Noninverting Load Configuration

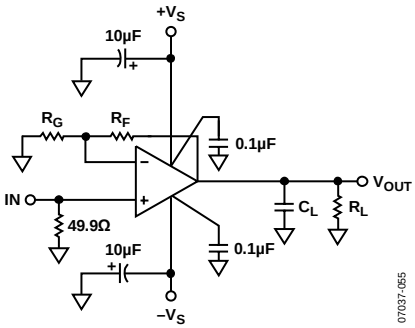

Figure 41. Typical Capacitive Load Configuration

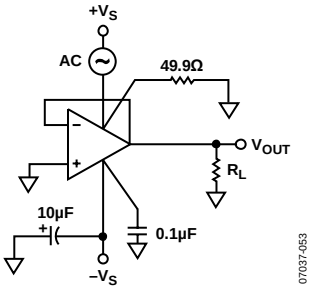

Figure 39. Positive Power Supply Rejection

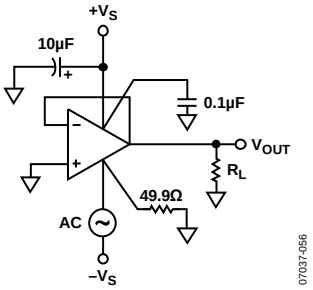

Figure 42. Negative Power Supply Rejection

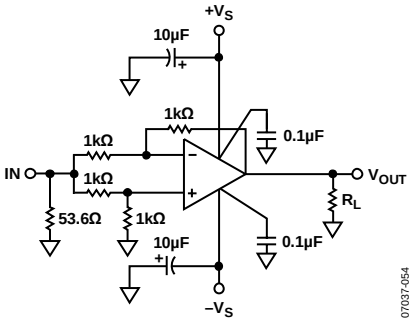

Figure 40. Common-Mode Rejection

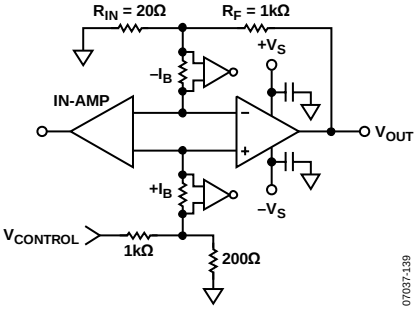

Figure 43.DC Test Circuit

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THEORY OF OPERATION

The ADA4898 is a voltage feedback op amp that combines unity gain stability with 0.9 nV/√Hz input noise. It employs a highly linear input stage that can maintain greater than −90 dBc (at 2 V p-p) distortion out to 600 kHz while in a unity-gain configuration. This rare combination of unity gain stability, low input-referred noise, and extremely low distortion is the result of Analog Devices, Inc., proprietary op amp architecture and high voltage bipolar processing technology.

The simplified ADA4898 topology, shown in Figure 44, is a single gain stage with a unity gain output buffer. It has over 100 dB of open-loop gain and maintains precision specifications, such as CMRR, PSRR, and offset, to levels that are normally associated with topologies having two or more gain stages.

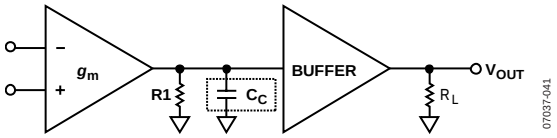

Figure 44. Topology

$\overline{PD}$ (POWER-DOWN) PIN FOR THE ADA4898-1

The $\overline{PD}$ pin saves power by decreasing the quiescent power dissipated in the device. It is very useful when power is an issue and the device does not need to be turned on at all times. The response of the device is rapid when going from power-down mode to full power operation mode. Note that $\overline{PD}$ does not put the output in a high-Z state, which means that the ADA4898 is not recommended for use as a multiplexer. Leaving the $\overline{PD}$ pin floating keeps the amplifier in full power operation mode.

Table 7. Power-Down Voltage Control

$\overline{PD}$ Pin	±15 V	±10 V	±5 V
Power-Down Mode	≤−14 V	≤−9 V	≤−4 V

0.1 Hz TO 10 Hz NOISE

Figure 45 shows the 0.1 Hz to 10 Hz voltage and current noise of the ADA4898. The peak-to-peak noise voltage is below 0.5 µV. Figure 46 shows the circuit used to measure the low frequency noise. It uses a band-pass filter of approximately 0.1 Hz and 10 Hz and a high gain stage feeding into an instrumentation amplifier.

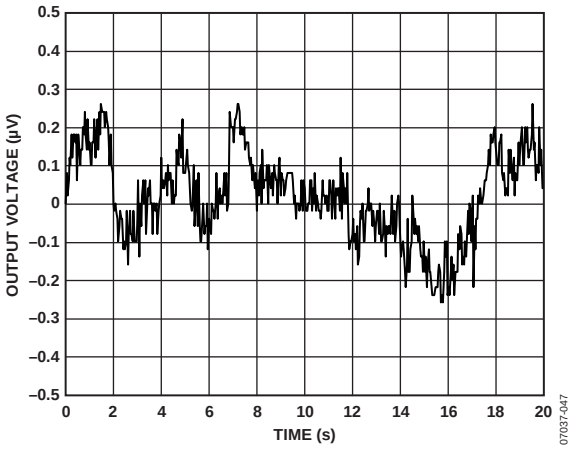

Figure 45. 0.1 Hz to 10 Hz Noise

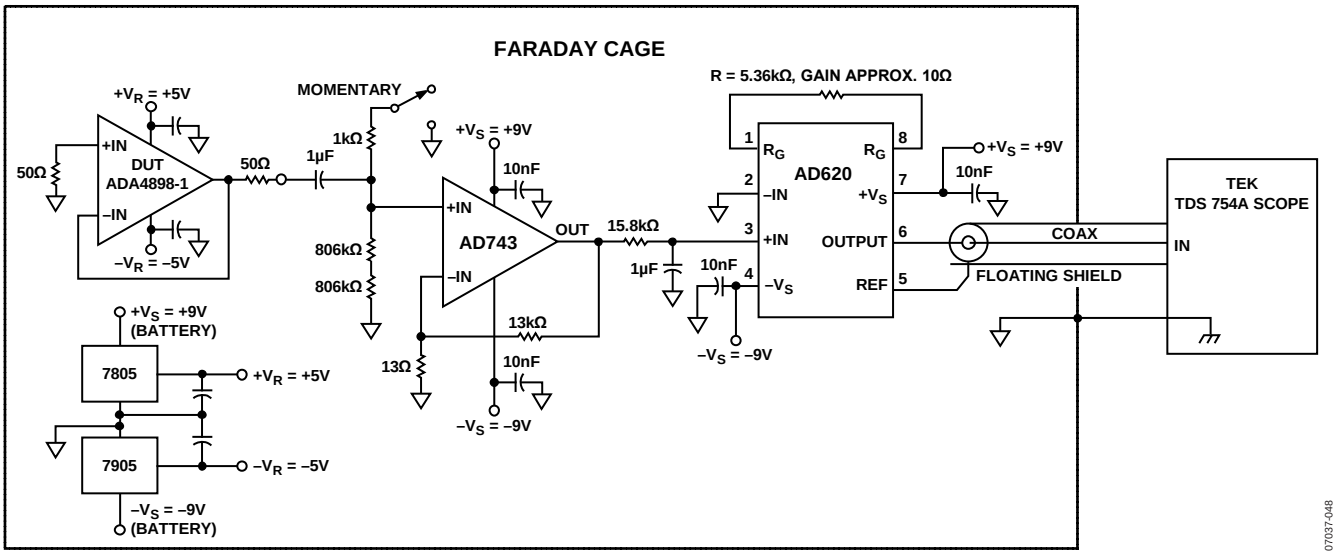

Figure 46. Low Frequency Noise Circuit

APPLICATIONS INFORMATION

HIGHER FEEDBACK RESISTOR GAIN OPERATION

The ADA4898 schematic for the noninverting gain configuration shown in Figure 47 is nearly a textbook example. The only exception is the feedback capacitor in parallel with the feedback resistor, R_F, but this capacitor is recommended only when using a large R_F value (>300 Ω). Figure 48 shows the difference between using a 100 Ω resistor and a 1 kΩ feedback resistor. Due to the high input capacitance in the ADA4898 when using a higher feedback resistor, more peaking appears in the closed-loop gain. Using the lower feedback resistor resolves this issue; however, when running at higher supplies (±15 V) with an R_F of 100 Ω, the system draws a lot of extra current into the feedback network. To avoid this problem, a higher feedback resistor can be used with a feedback capacitor in parallel. Figure 48 shows the effect of placing a feedback capacitor in parallel with a larger R_F. In this gain-of-2 configuration, $R_F = R_G = 1$ kΩ and $C_F = 2.7$ pF. When using C_F, the peaking drops from 6 dB to less than 2 dB.

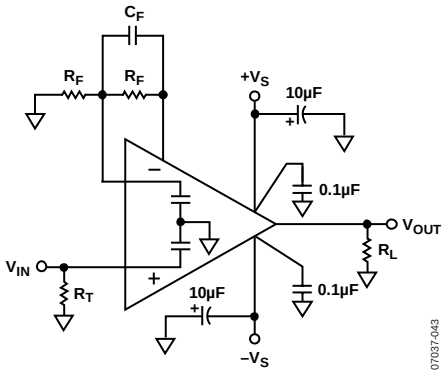

Figure 47. Noninverting Gain Schematic

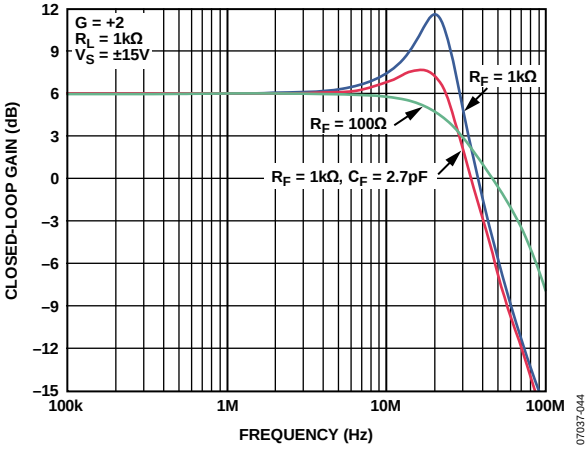

Figure 48. Small Signal Frequency Response for Various Feedback Impedances

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 8 provides a useful reference for determining various gains and associated performance. R_F is set to 100 Ω for gains greater than 1. A low feedback R_F resistor value reduces peaking and minimizes the contribution to the overall noise performance of the amplifier.

Table 8. Gains and Recommended Resistor Values Associated with Them (Conditions: V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ, R_T = 49.9 Ω)

Gain	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz), V_{OUT} = 100 mV p-p	Slew Rate (V/µs), V_{OUT} = 2 V Step	ADA4898 Voltage Noise (nV/√Hz), RTO	Total System Noise (nV/√Hz), RTO
+1	0	N/A	65	55	0.9	1.29
+2	100	100	30	50	1.8	3.16
+5	100	24.9	9	45	4.5	7.07

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NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources, and then determine if each source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities were used rather than actual voltages to leave bandwidth out of the expressions. Noise spectral density, which is generally expressed in nV/√Hz, is equivalent to the noise in a 1 Hz bandwidth.

The noise model shown in Figure 49 has six individual noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally specified as referring to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO) and then divide by the noise gain to obtain the RTI noise.

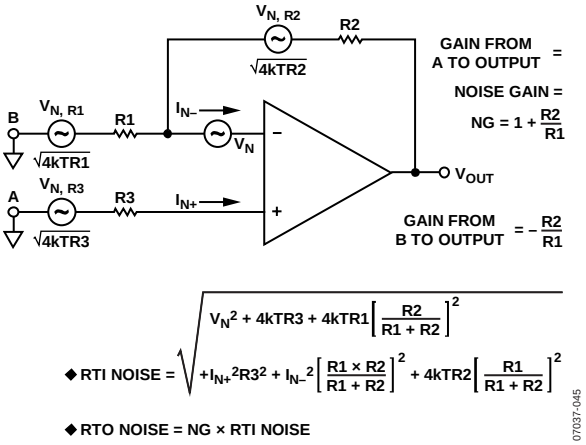


Figure 49. Op Amp Noise Analysis Model

All resistors have a Johnson noise that is calculated by

$$\sqrt{(4kBTR)}$$

where:
k is Boltzmann's constant (1.38×10^{-23} J/K).
B is the bandwidth in Hertz.
T is the absolute temperature in Kelvin.
R is the resistance in ohms.

A simple relationship that is easy to remember is that a 50 Ω resistor generates a Johnson noise of 1 nV/√Hz at 25°C.

In applications where noise sensitivity is critical, care must be taken not to introduce other significant noise sources to the amplifier. Each resistor is a noise source. Attention to the following areas is critical to maintain low noise performance: design, layout, and component selection. A summary of noise performance for the amplifier and associated resistors is shown in Table 8.

CIRCUIT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4898 board yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

PCB LAYOUT

Because the ADA4898 has a small signal bandwidth of 65 MHz, it is essential that high frequency board layout techniques be employed. All ground and power planes under the pins of the ADA4898 should be cleared of copper to prevent the formation of parasitic capacitance between the input pins to ground and the output pins to ground. A single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground plane is not cleared from under the mounting pads.

POWER SUPPLY BYPASSING

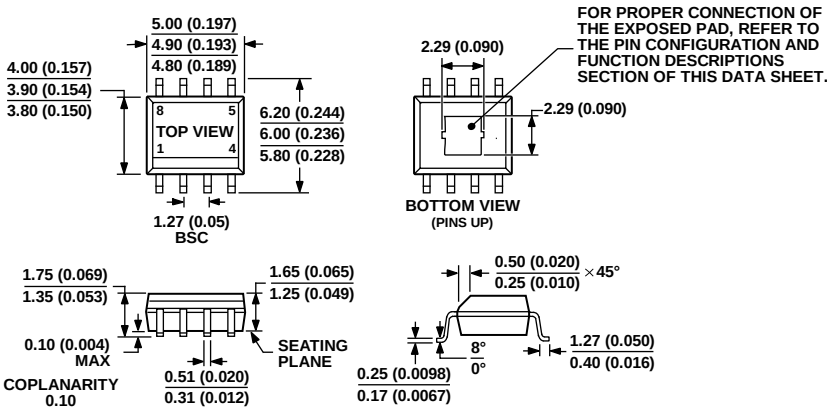
Power supply bypassing for the ADA4898 has been optimized for frequency response and distortion performance. Figure 47 shows the recommended values and location of the bypass capacitors. Power supply bypassing is critical for stability, frequency response, distortion, and PSR performance. The 0.1 µF capacitors shown in Figure 47 should be as close to the supply pins of the ADA4898 as possible. The 10 µF electrolytic capacitors should be adjacent to, but not necessarily close to, the 0.1 µF capacitors. The capacitor between the two supplies helps improve PSR and distortion performance. In some cases, additional paralleled capacitors can help improve frequency and transient response.

GROUNDING

Ground and power planes should be used where possible. Ground and power planes reduce the resistance and inductance of the power planes and ground returns. The returns for the input and output terminations, bypass capacitors, and R_G should all be kept as close to the ADA4898 as possible. The output load ground and the bypass capacitor grounds should be returned to the same point on the ground plane to minimize parasitic trace inductance, ringing, and overshoot and to improve distortion performance.

The ADA4898 package features an exposed paddle. For optimum electrical and thermal performance, solder this paddle to a negative supply plane.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-A A

CONTROLLING DIMENSIONS ARE IN MILLIMETER; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

072808A

Figure 50. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP] (RD-8-1)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4898-1YRDZ	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	1
ADA4898-1YRDZ-R7	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	1,000
ADA4898-1YRDZ-RL	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	2,500
ADA4898-2YRDZ	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	1
ADA4898-2YRDZ-R7	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	1,000
ADA4898-2YRDZ-RL	−40°C to +105°C	8-Lead SOIC_N_EP	RD-8-1	2,500

[1] Z = RoHS Compliant Part.

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NOTES

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NOTES

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