



September 1983
Revised January 2005

MM74HC125/MM74HC126 3-STATE Quad Buffers

General Description

The MM74HC125 and MM74HC126 are general purpose 3-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM74HC125 require the 3-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM74HC126 require the control input to be low to put the output into high impedance.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC)
- Fanout of 15 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC125SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC125MTCX-NL		Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC125N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC126M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC126MX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC126SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC126MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC126MTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC126N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

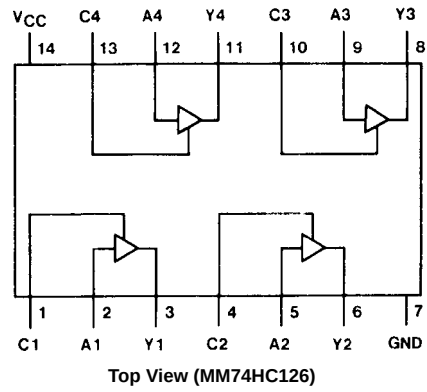
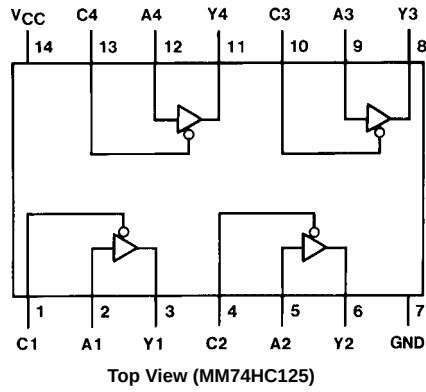
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. (Tape and Reel not available in N14A.)
Pb-Free package per JEDEC J-STD-020B.

MM74HC125/MM74HC126 3-STATE Quad Buffers

MM74HC125/MM74HC126

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



Truth Tables

Inputs		Output Y
A	C	
H	L	H
L	L	L
X	H	Z

Inputs		Output Y
A	C	
H	H	H
L	H	L
X	L	Z

MM74HC125/MM74HC126

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 45 pF$, $t_r = t_f = 6 ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to HIGH Level	$R_L = 1 k\Omega$	13	25	ns
t_{PHZ}	Maximum Output Disable Time from HIGH Level	$R_L = 1 k\Omega$ $C_L = 5 pF$	17	25	ns
t_{PZL}	Maximum Output Enable Time to LOW Level	$R_L = 1 k\Omega$	18	25	ns
t_{PLZ}	Maximum Output Disable Time from LOW Level	$R_L = 1 k\Omega$ $C_L = 5 pF$	13	25	ns

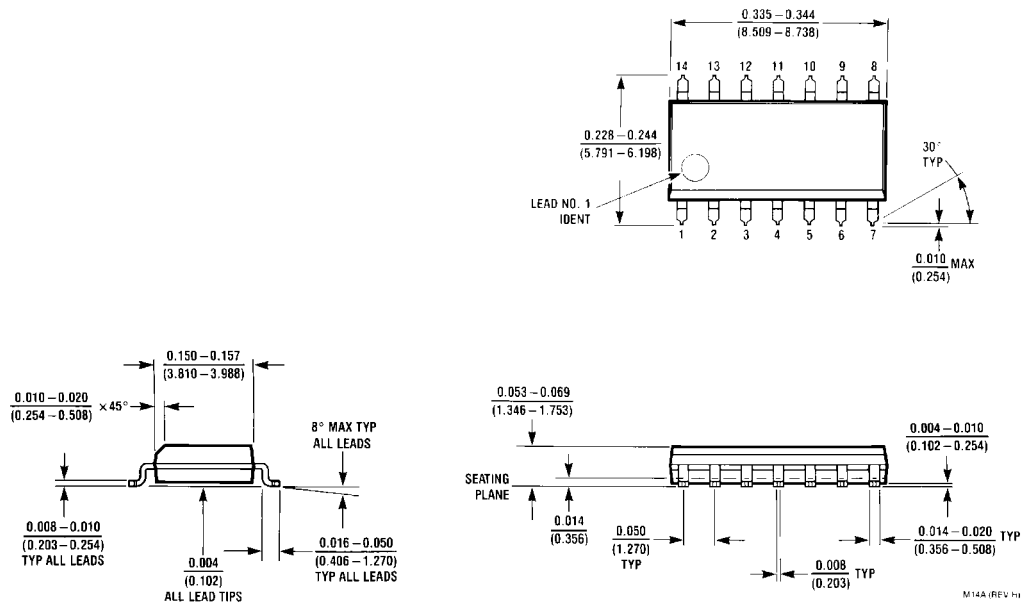
AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50 pF$, $t_r = t_f = 6 ns$ (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = −40 to 85°C	T _A = −40 to 125°C	Units
				Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay Time		2.0V	40	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay Time	C _L = 150 pF	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	39	ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	R _L = 1 kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	R _L = 1 kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t _{PZL} , t _{PZH}	Maximum Output Enable Time	C _L = 150 pF R _L = 1 kΩ	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time	C _L = 50 pF	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C _{IN}	Input Capacitance			5	10	10	10	pF
C _{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						
		Enabled		45				pF
		Disabled		6				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

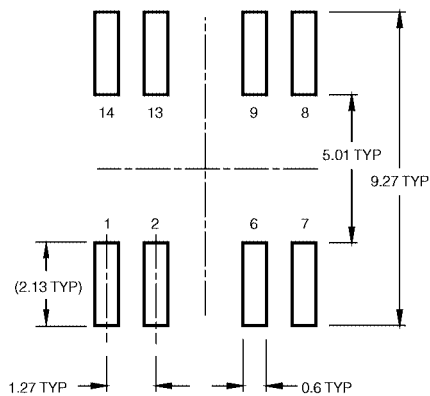
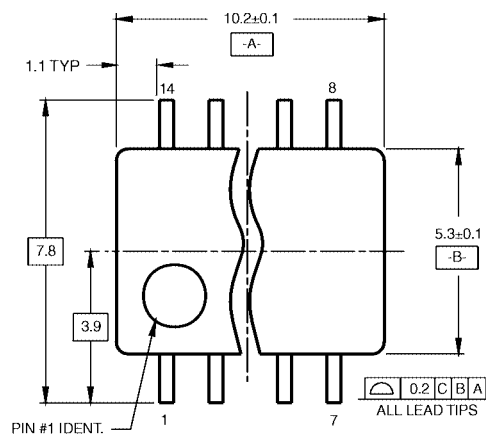
Physical Dimensions inches (millimeters) unless otherwise noted



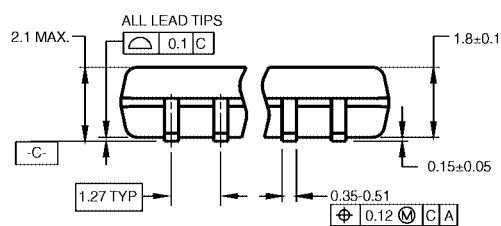
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

MM74HC125/MM74HC126

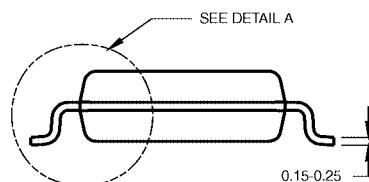
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

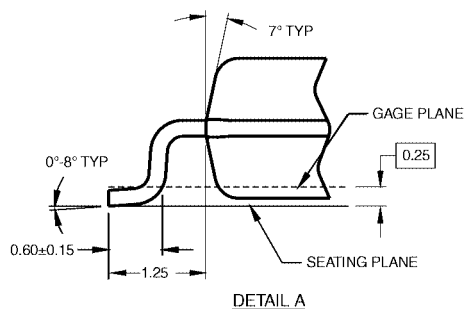


DIMENSIONS ARE IN MILLIMETERS



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

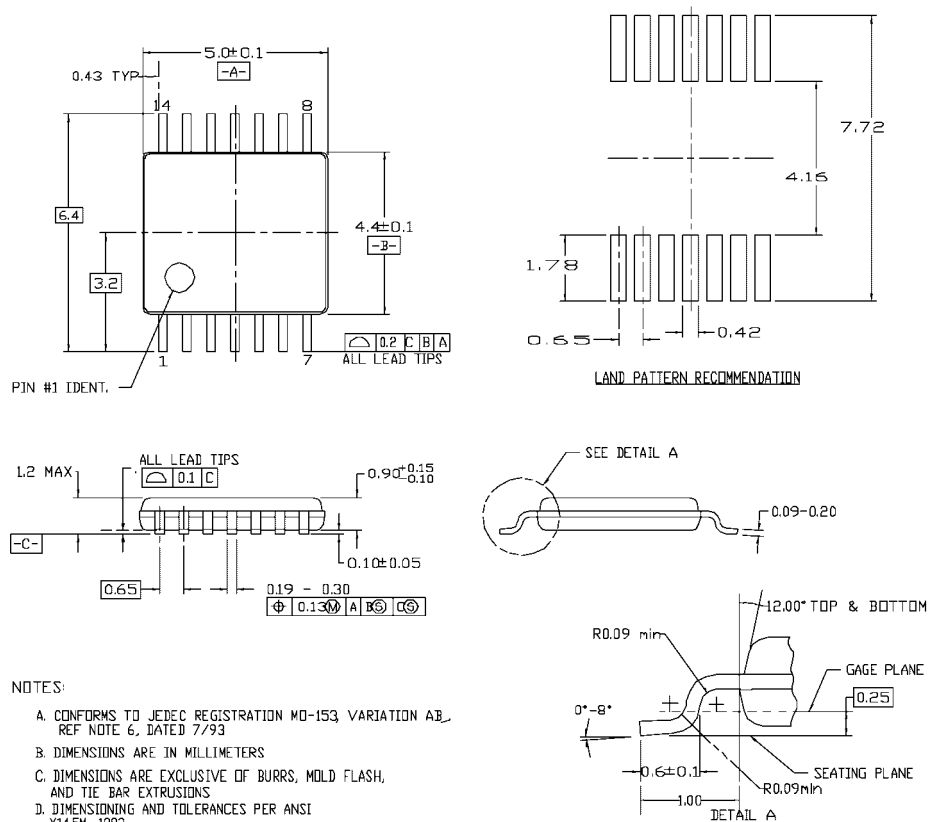
M14DRevB1



DETAIL A

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



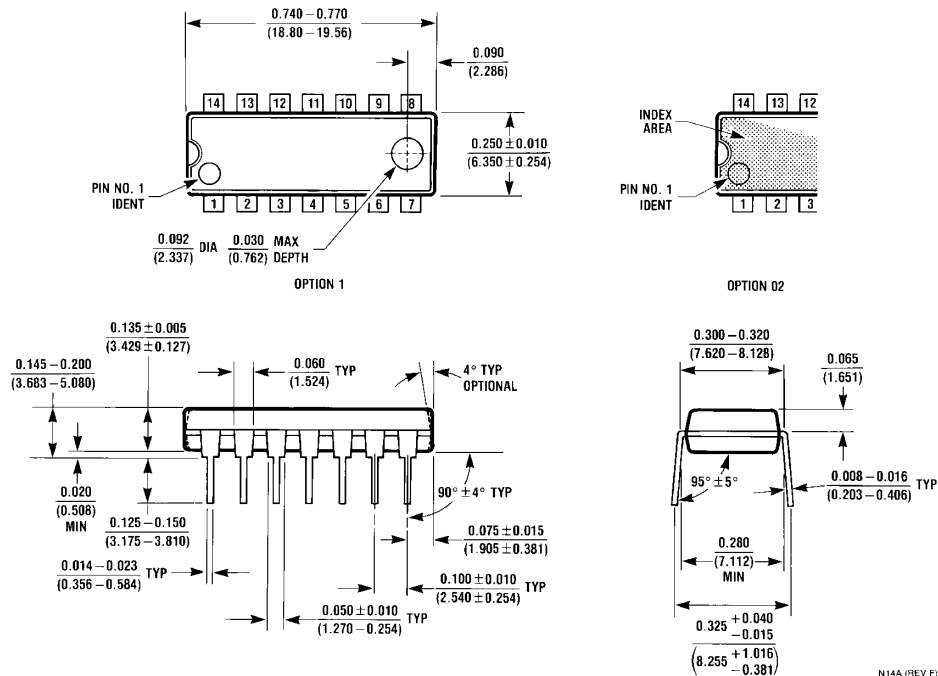
NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
- DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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