"SN75ALS056"

- **Suitable for IEEE Standard 896 Applications†**
- **SN75ALS056 is an Octal Transceiver**
- **SN75ALS057 is a Quad Transceiver**
- **High-Speed Advanced Low-Power Schottky (ALS) Circuitry**
- **Low Power Dissipation:**
  52.5 mW/Channel Max
- **High-Impedance pnp Inputs**
- **Logic-Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**
- **Designed to Be a Faster, Lower-Power Functional Equivalent of National DS3896, DS3897**

SN75ALS056 . . . DW OR N PACKAGE
(TOP VIEW)

A1	1	20	B1
A2	2	19	B2
A3	3	18	B3
A4	4	17	B4
V_CC	5	16	GND
A5	6	15	B5
A6	7	14	B6
A7	8	13	B7
A8	9	12	B8
$\overline{CS}$	10	11	T/$\overline{R}$

SN75ALS057 . . . DW OR N PACKAGE
(TOP VIEW)

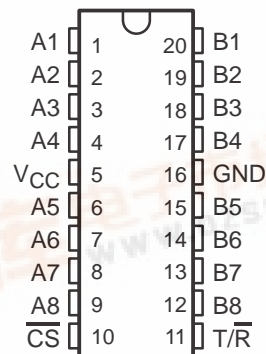|			
D1	1	20	B1
R1	2	19	E1
D2	3	18	B2
R2	4	17	E2
V_CC	5	16	GND
D3	6	15	B3
R3	7	14	E3
D4	8	13	B4
R4	9	12	E4
$\overline{TE}$	10	11	$\overline{RE}$

description

The SN75ALS056 is an eight-channel, monolithic, high-speed, advanced low-power Schottky (ALS) device designed for two-way data communication in a densely populated backplane. The SN75ALS057 is a four-channel version with independent driver-input (Dn) and receiver-output (Rn) pins and a separate driver disable for each driver (En).
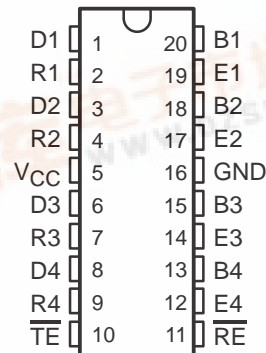
These transceivers feature open-collector driver outputs with series Schottky diodes to reduce capacitive loading to the bus. By using a 2-V pullup termination on the bus, the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet.

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TEXAS INSTRUMENTS

SN75ALS056, SN75ALS057
TRAPEZOIDAL-WAVEFORM INTERFACE BUS TRANSCEIVERS

logic symbol†

SN75ALS056

Pin	Signal		Label		Pin	Signal
11	T/R̄	3EN1 (A-B)				
		3EN2 (B-A)				
10	CS	G3				
1	A1	▷ 1 ◇		20	B1	
		▽ 2				
2	A2			19	B2	
3	A3			18	B3	
4	A4			17	B4	
6	A5			15	B5	
7	A6			14	B6	
8	A7			13	B7	
9	A8			12	B8	

SN75ALS057

Pin	Signal	Label	Pin	Signal
10	T̄Ē	EN1 (D-B)		
11	R̄Ē	EN2 (B-R)		
1	D1	& ▷ 1 ◇	20	B1
19	E1			
2	R1	▽ 2		
3	D2		18	B2
17	E2			
4	R2			
6	D3		15	B3
14	E3			
7	R3			
8	D4		13	B4
12	E4			
9	R4			
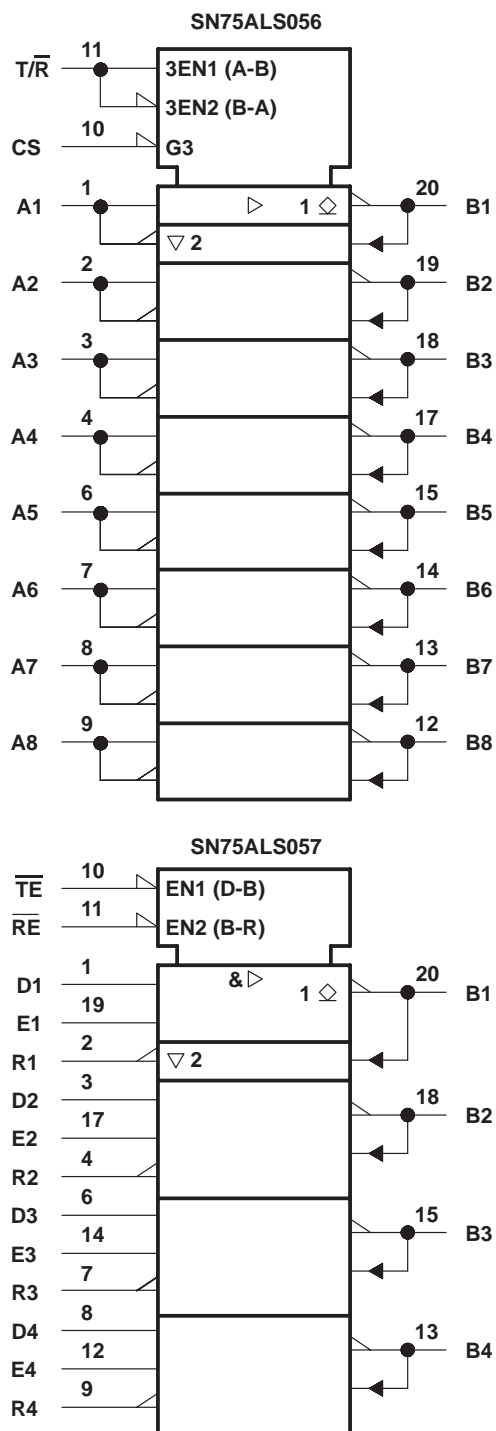
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

"SN75ALS056"

logic diagram (positive logic)

SN75ALS056

SN75ALS057

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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Function Tables

SN75ALS056
TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{\text{CS}}$	T/$\overline{\text{R}}$	A ↔ B
L	H	T(A B)
L	L	R(B A)
H	X	D

SN75ALS057
TRANSMIT/RECEIVE

CONTROLS			CHANNELS			
$\overline{\text{TE}}$	$\overline{\text{RE}}$	En	D	B	B	R
L	L	L	D			R
L	L	H	T			R
L	H	L	D			D
L	H	H	T			D
H	L	X	D			R
H	H	X	D			D

H = high level, L = low level, R = receive, T = transmit,
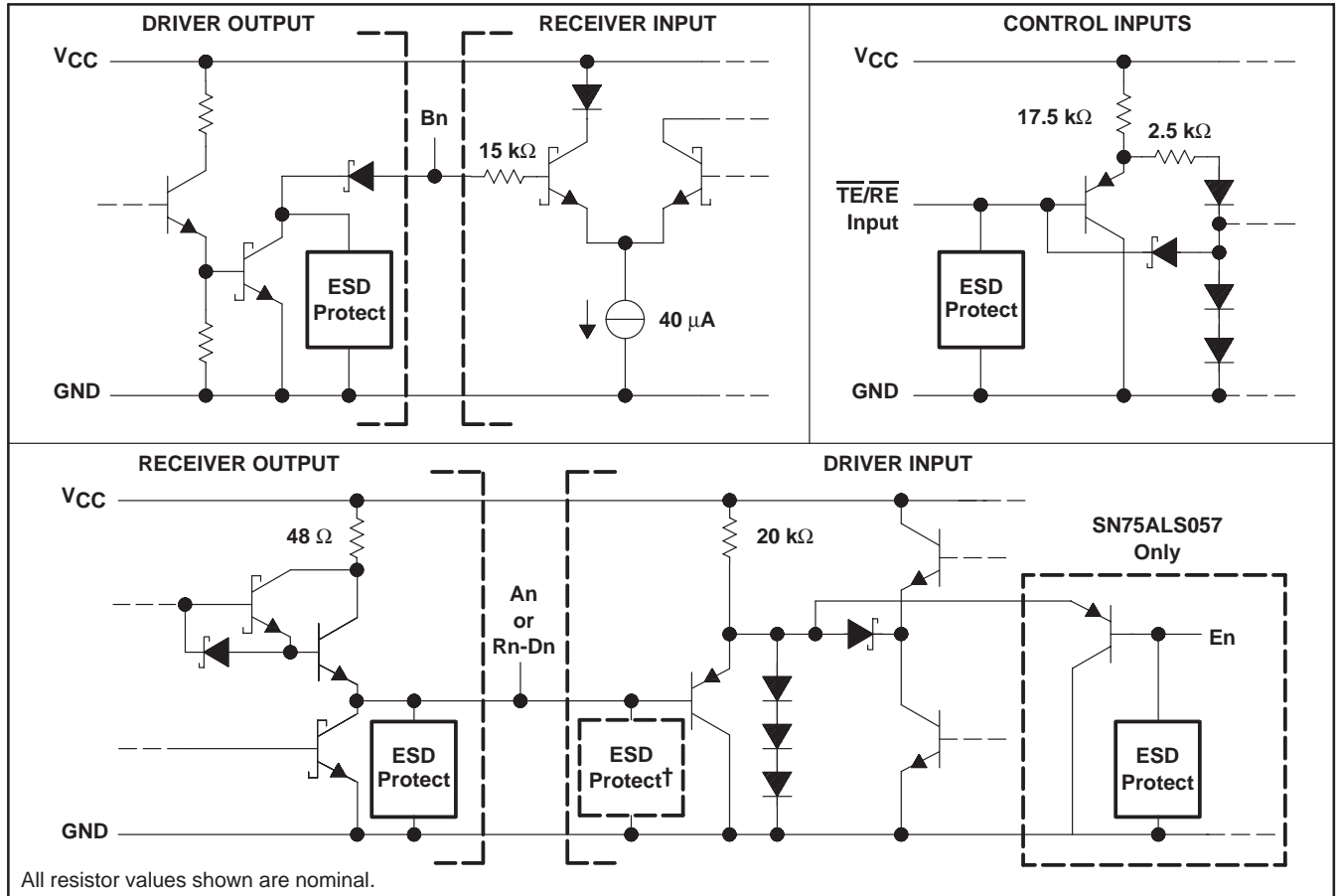D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs

All resistor values shown are nominal.

† Additional ESD protection is on the SN75ALS057, which has separate receiver-output and driver-input pins.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) .... 6 V
Control input voltage, V_I .... 5.5 V
Driver input voltage, V_I .... 5.5 V
Driver output voltage, V_O .... 2.5 V
Receiver input voltage, V_I .... 2.5 V
Receiver output voltage, V_O .... 5.5 V
Continuous total power dissipation .... See Dissipation Rating Table
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package .... 260 °C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN75ALS056 MIN	SN75ALS056 TYP†	SN75ALS056 MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$	$I_I = -18$ mA			−1.5	V
V_{IT}	Receiver input threshold voltage at Bn		1.405		1.69	V
V_{OH}	High-level output voltage at An	Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8V, $I_{OH} = -400$ µA	2.4			V
V_{OL}	Low-level output voltage An	Bn at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, $I_{OL} = 16$ mA			0.5	V
	Low-level output voltage Bn	An at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, $V_L = 2$ V, $R_L = 18.5$ Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current An, T/$\overline{R}$ or $\overline{CS}$	$V_I = V_{CC}$			40	µA
	High-level input current Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, An at 0.8 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$	$V_I = 0.4$ V			−400	µA
I_{OS}	Short-circuit output current at An	An at 0, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current				75	mA
$C_{O(B)}$	Driver output capacitance			4.5		pF

† Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

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"SN75ALS056"

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN75ALS057			UNIT
				MIN	TYP†	MAX	
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_{IT}	Receiver input threshold voltage at Bn			1.41		1.69	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -400$ µA	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 16$ mA			0.5	V
		Bn	Dn at 2 V, En at 2 V, $\overline{TE}$ at 0.8 V, $V_L = 2$ V, $R_L = 18.5$ Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	$V_I = V_{CC}$			40	µA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, En at 0.8 V, $\overline{TE}$ at 0.8 V			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		$V_I = 0.4$ V			−400	µA
I_{OS}	Short-circuit output current at Rn		Rn at 0, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−40		−120	mA
I_{CC}	Supply current					40	mA
$C_{O(B)}$	Driver output capacitance				4.5		pF

† Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS056 DRIVER			UNIT
					MIN	TYP†	MAX	
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{CS}$	Bn	An and $T/\overline{R}$ at 2 V, $V_L = 2$ V, $R_L1 = 18$ Ω, $C_L = 30$ pF, R_L2 not connected, See Figure 2			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output						20	
t_{PLH2}	Propagation delay time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, $V_L = 2$ V, $R_L1 = 18$ Ω, R_L2 not connected, $C_L = 30$ pF, See Figure 2,			19	ns
t_{PHL2}	Propagation delay time high-to-low-level output						18	
t_{PLH3}	Propagation delay time, low-to-high-level output	$T/\overline{R}$	Bn	$V_{I(An)} = 5$ V, CS at 0.8 V, $R_L1 = 18$ Ω, $C_L = 30$ pF, R_L2 not connected, $V_L = 2$ V, See Figure 3,			25	ns
t_{PHL3}	Propagation delay time, high-to-low-level output						35	
t_{TLH}	Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 2 V, $V_L = 2$ V, $C_L = 30$ pF, $R_L1 = 18$ Ω, R_L2 not connected, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

† Typical values are at $V_{CC} = 5$ V, $T_A = 25$°C

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SN75ALS056, SN75ALS057
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS056 RECEIVER		UNIT
					MIN	MAX	
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ1}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		20	ns
t_{PZL1}	Output enable time to low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ1}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		17	ns
t_{PZH1}	Output enable time to high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $VI_{(Bn)}$ = 0, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
t_{PLZ2}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		8	ns
t_{PZH2}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, V_L = 5 V, See Figure 6	3		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 DRIVER			UNIT
					MIN	TYP[†]	MAX	
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_L2 not connected, R_L1 = 18 Ω, See Figure 2, C_L = 30 pF			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output						20	
t_{PLH2}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2			19	ns
t_{PHL2}	Propagation delay time, high-to-low-level output						18	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, $\overline{TE}$ at 0.8 V, R_L1 = 18 Ω,, R_L2 not connected, C_L = 30 pF, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 RECEIVER		UNIT
					MIN	MAX	
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ2}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 30 pF, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		17	ns
t_{PZH2}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 30 pF, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	$\overline{TE}$ at 2 V, $\overline{RE}$ at 0.8 V, V_L = 0, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 6	3		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 DRIVER PLUS RECEIVER		UNIT
					MIN	MAX	
t_{PLH6}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, $R_L1 = 390\ \Omega$, $R_L2 = 1.6\ k\Omega$, $C_L = 30\ pF$, See Figure 7		40	ns
t_{PHL6}	Propagation delay time, high-to-low-level output					40	

PARAMETER MEASUREMENT INFORMATION
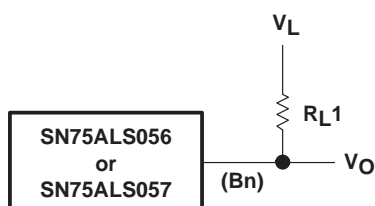
Figure 1. Driver Low-Level-Output-Voltage Test Circuit

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PARAMETER MEASUREMENT INFORMATION
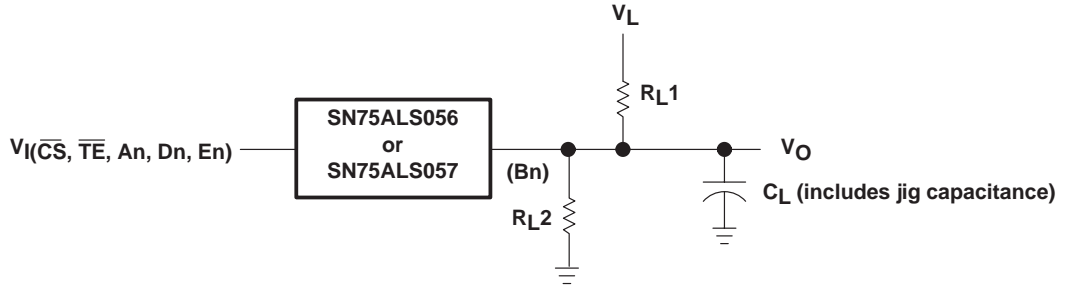
TEST CIRCUIT
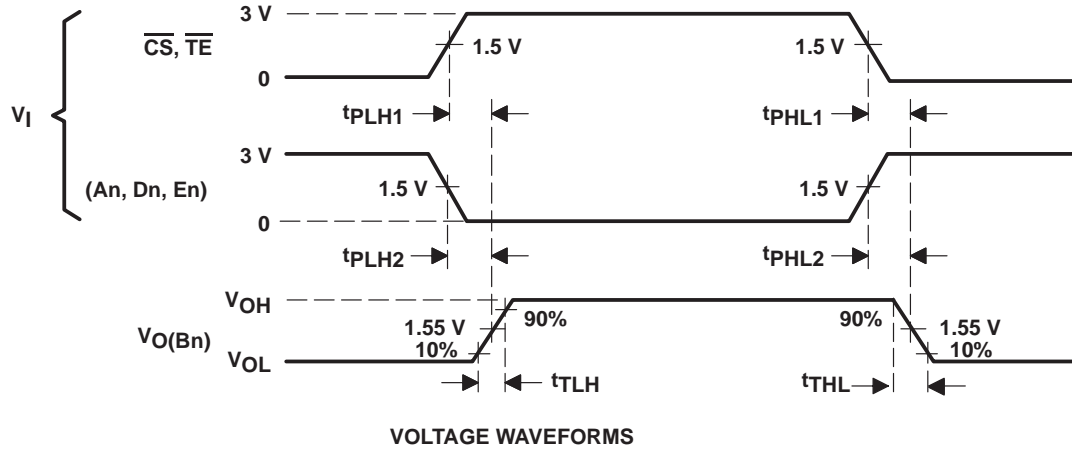
VOLTAGE WAVEFORMS

NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
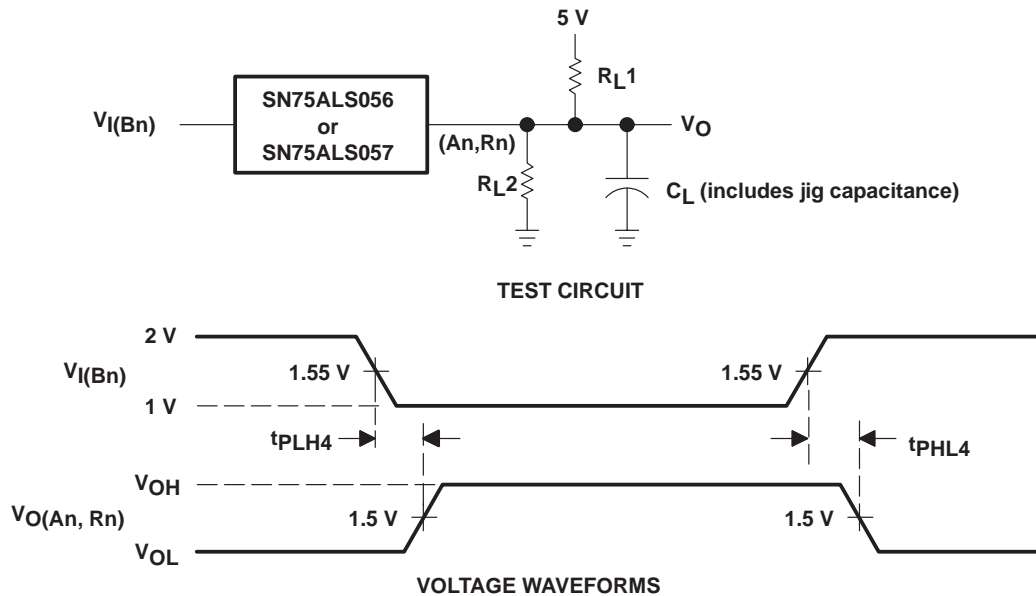

TEST CIRCUIT

VOLTAGE WAVEFORMS
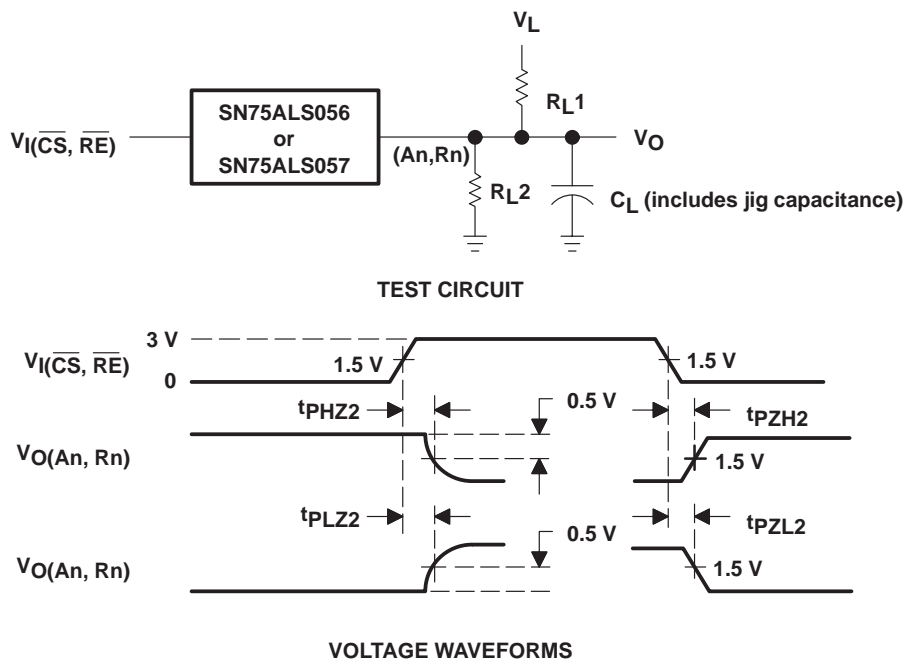
NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 3. Propagation Delay From T/R̄ to An or Bn Test Circuit and Voltage Waveforms

"SN75ALS056"

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 4. Receiver Test Circuit and Voltage Waveforms

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 5. Propagation Delay From $\overline{CS}$ to An or $\overline{RE}$ to Rn Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

t_W is increased until the output voltage
fall just reaches 2 V.

t_W is increased until the output voltage rise
just reaches 0.8 V.

VOLTAGE WAVEFORMS

NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%
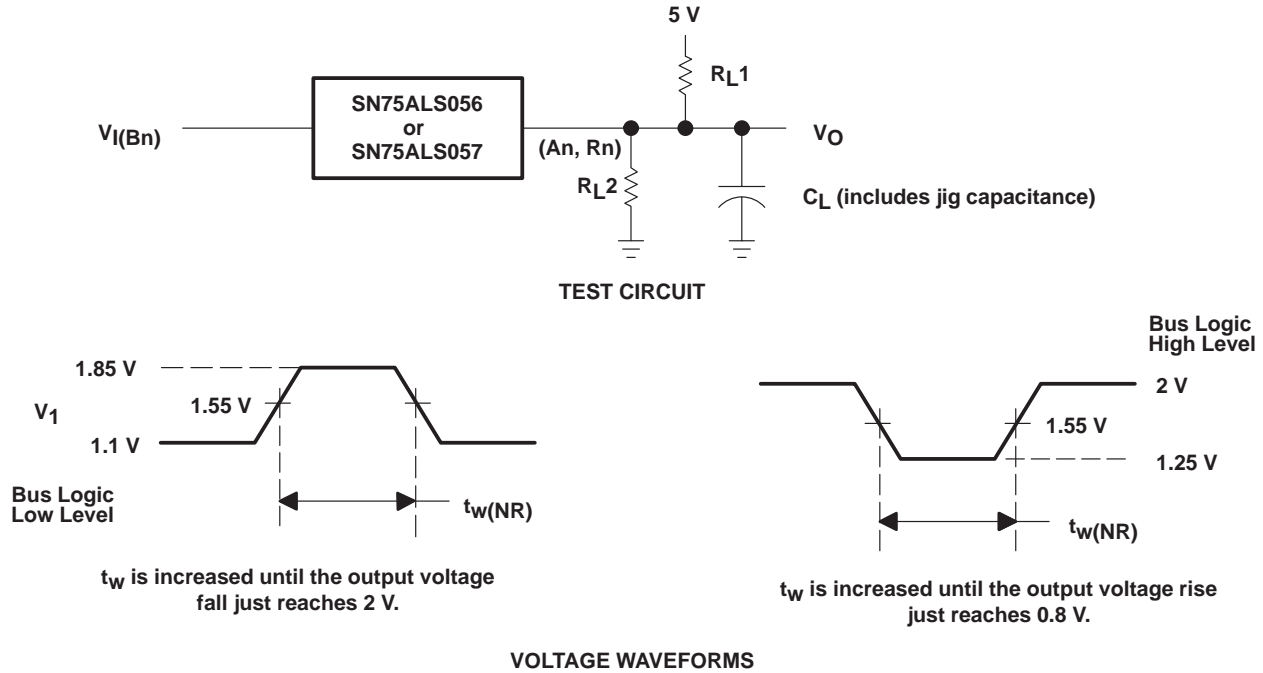
Figure 6. Receiver Noise-Immunity Test Circuit and Voltage Waveforms

TEST CIRCUIT

VOLTAGE WAVEFORMS

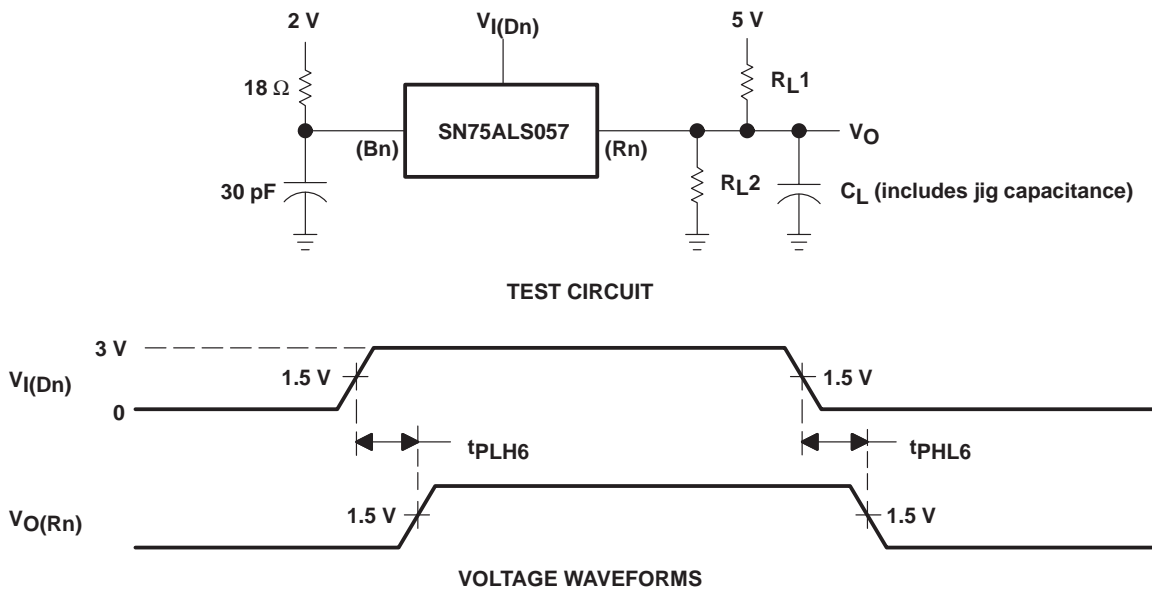NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 7. Driver Plus Receiver Delay-Times Test Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75ALS056DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS056DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS056DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS056DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS056DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS056N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS056NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS057DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS057N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS057NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
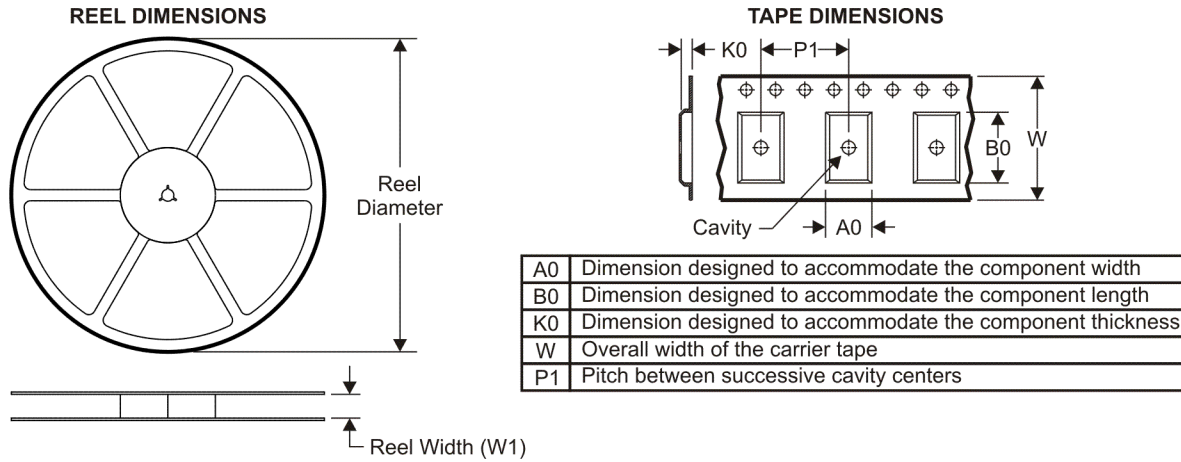
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS056DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1
SN75ALS057DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS056DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN75ALS057DWR	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE
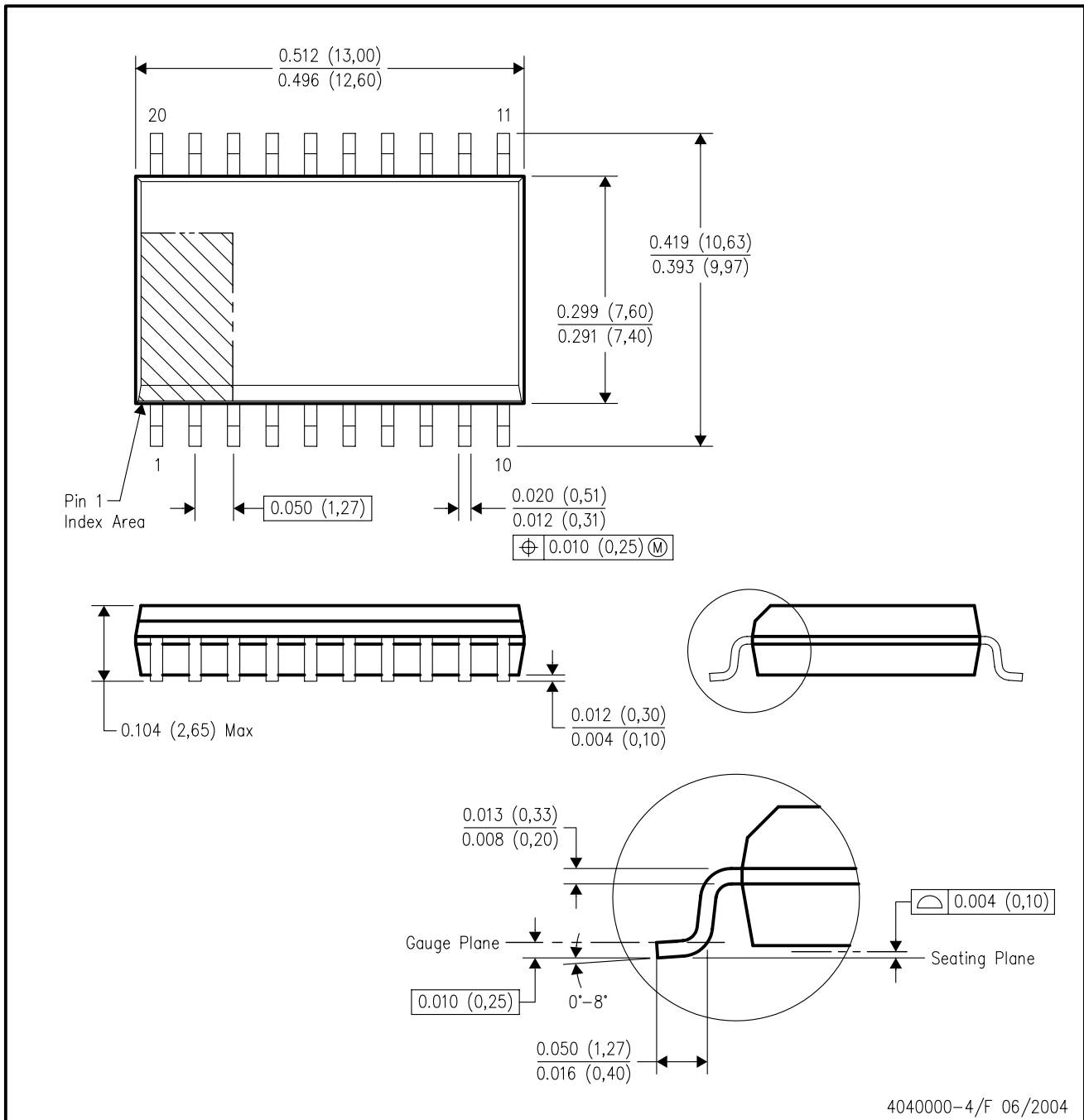
0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
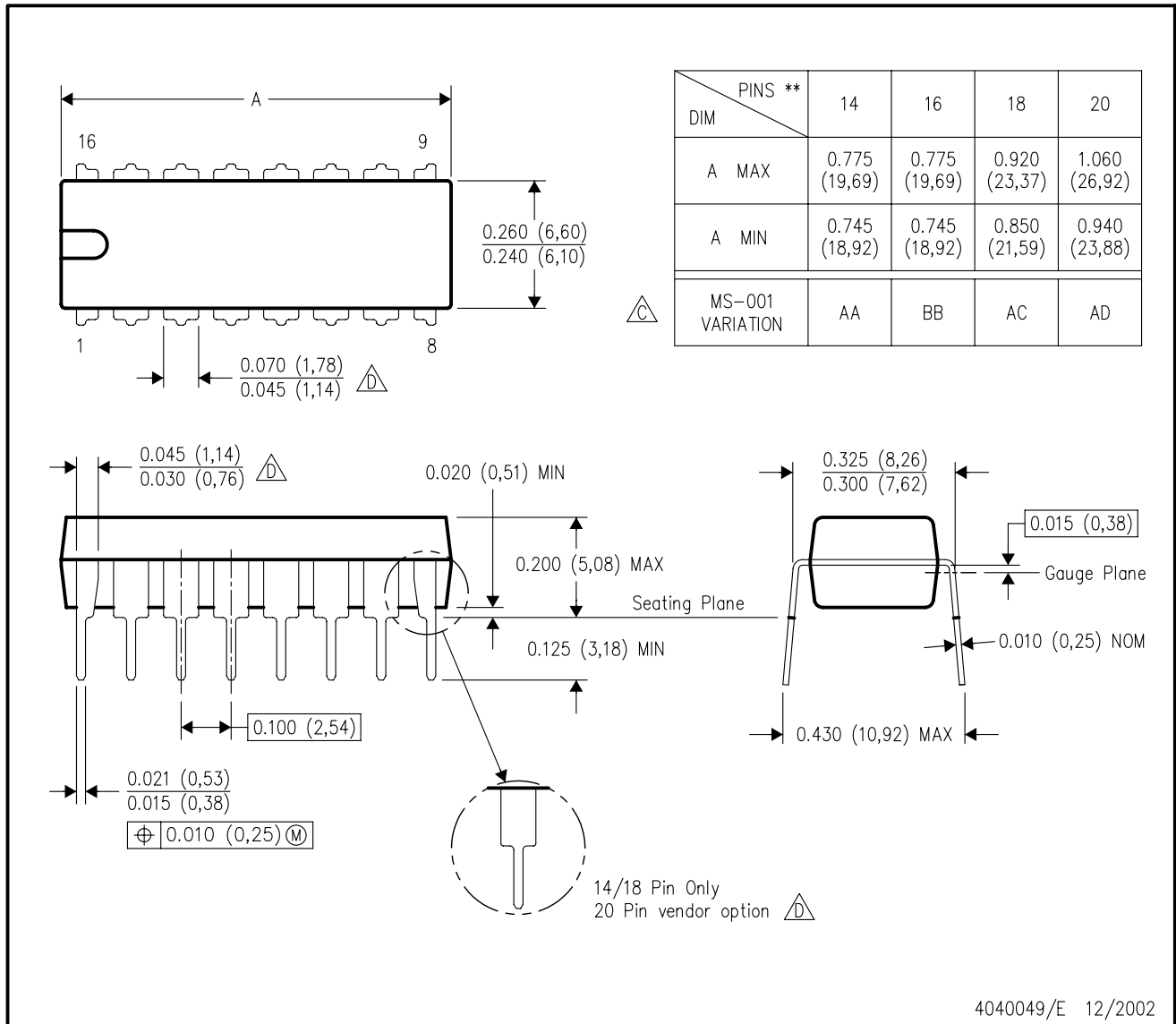0.016 (0,40)

4040000−4/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D.   Falls within JEDEC MS−013 variation AC.

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N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION ⟨C⟩	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) ⟨D⟩

0.045 (1,14) ⟨D⟩
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Gauge Plane

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⟨D⟩

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
   ⟨C⟩   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   ⟨D⟩   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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