



## **100302 Low Power Quint 2-Input OR/NOR Gate**

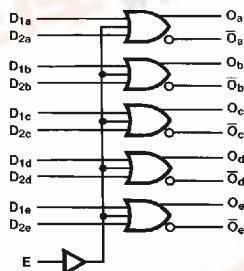
## **General Description**

The 100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 k $\Omega$  pull-down resistors and all outputs are buffered.

## Features

- 43% power reduction of the 100102
  - 2000V ESD protection
  - Pin/function compatible with 100102
  - Voltage compensated operating range =  
-4.2V to -5.7V
  - Available to MIL-STD-883
  - Available to industrial grade temperature range

## Logic Symbol



TL/F/10580-1

Pin Names	Description
$D_{na}$ - $D_{ne}$	Data Inputs
E	Enable Input
$O_a$ - $O_e$	Data Outputs
$\bar{O}_a$ - $\bar{O}_e$	Complementary Data Outputs

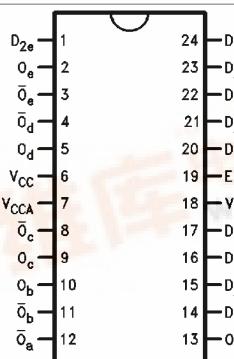
## Truth Table

D <sub>1X</sub>	D <sub>2X</sub>	E	O <sub>X</sub>	$\bar{O}_X$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level

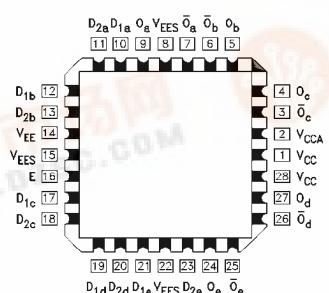
## Connection Diagrams

24-Pin DIP/SOIC



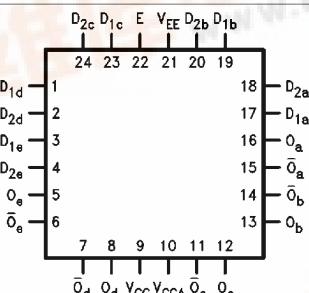
TL/F/10580-2

28-Pin PCC



TL/F/10580-4

### **24-Pin Quad Cerpak**



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### Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Maximum Junction Temperature ( $T_J$ )

Ceramic	$+175^{\circ}\text{C}$
Plastic	$+150^{\circ}\text{C}$

$V_{EE}$  Pin Potential to

Ground Pin	$-7.0\text{V}$ to $+0.5\text{V}$
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Input Voltage (DC)

$V_{EE}$  to  $+0.5\text{V}$

Output Current (DC Output HIGH)

$-50\text{ mA}$

ESD (Note 2)

$\geq 2000\text{V}$

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

### Recommended Operating Conditions

Case Temperature ( $T_C$ )

Commercial	$0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
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Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
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Military	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
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Supply Voltage ( $V_{EE}$ )

$-5.7\text{V}$  to  $-4.2\text{V}$

### Commercial Version

### DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$  to  $-5.7\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$ ,  $T_C = 0^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions		
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$	Loading with $50\Omega$ to $-2.0\text{V}$	
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV			
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$	Loading with $50\Omega$ to $-2.0\text{V}$	
$V_{OLC}$	Output LOW Voltage			-1610	mV			
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs		
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs		
$I_{IL}$	Input LOW Current	0.50			$\mu\text{A}$	$V_{IN} = V_{IL(\text{Min})}$		
$I_{IH}$	Input HIGH Current			240	$\mu\text{A}$	$V_{IN} = V_{IH(\text{Max})}$		
$I_{EE}$	Power Supply Current	-45	-36	-20	mA	Inputs Open		

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### DIP AC Electrical Characteristics

$V_{EE} = -4.2\text{V}$  to  $-5.7\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	$T_C = 0^{\circ}\text{C}$		$T_C = +25^{\circ}\text{C}$		$T_C = +85^{\circ}\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.50	1.25	ns	<i>Figures 1 and 2</i> (Note 1)
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.70	1.90	0.70	1.90	0.80	2.00	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.20	0.40	1.20	0.40	1.20	ns	<i>Figures 1 and 2</i>

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

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### Commercial Version (Continued)

#### SOIC, PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.50	1.05	0.50	1.05	0.50	1.15	ns	<i>Figures 1 and 2</i> (Note 2)
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.70	1.80	0.70	1.80	0.80	1.90	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.40	1.10	0.40	1.10	0.40	1.10	ns	<i>Figures 1 and 2</i>
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PCC Only (Note 1)
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		310		310		310	ps	PCC Only (Note 1)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PCC Only (Note 1)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		250		250		250	ps	PCC Only (Note 1)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Enable to Output Path		330		330		330	ps	PCC Only (Note 1)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Enable to Output Path		280		280		280	ps	PCC Only (Note 1)

**Note 1:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ( $t_{OSHL}$ ), or LOW to HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

### Industrial Version

#### PCC DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$  (Note 3)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}(Max)$ or $V_{IL}(Min)$	Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620			
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}(Min)$ or $V_{IL}(Max)$	Loading with $50\Omega$ to $-2.0V$
$V_{OLC}$	Output LOW Voltage		-1565		-1610			
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for ALL Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for ALL Inputs	
$I_{IL}$	Input LOW Current	0.05		0.05		$\mu A$	$V_{IN} = V_{IL}(Min)$	
$I_{IH}$	Input HIGH Current		300		240	$\mu A$	$V_{IN} = V_{IH}(Max)$	
$I_{EE}$	Power Supply Current	-45	-20	-45	-20	mA	Inputs Open	

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under the "worst case" conditions.

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### Industrial Version (Continued)

#### PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.40	1.05	0.50	1.05	0.50	1.15	ns	<i>Figures 1 and 2</i> (Note 1)
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.70	1.80	0.70	1.80	0.80	1.90	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.30	1.10	0.40	1.10	0.40	1.10	ns	<i>Figures 1 and 2</i>

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

### Military Version

#### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$  (Note 3)

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions		Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}(Max)$ or $V_{IL}(Min)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3	
		-1085	-870	mV	$-55^\circ C$				
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}(Max)$ or $V_{IL}(Min)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3	
		-1830	-1555	mV	$-55^\circ C$				
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}(Max)$ or $V_{IL}(Min)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3	
		-1085		mV	$-55^\circ C$				
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}(Max)$ or $V_{IL}(Min)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3	
			-1555	mV	$-55^\circ C$				
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4	
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4	
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IH}(Max)$	1, 2, 3		
$I_{IH}$	Input HIGH Current		240	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IL}(Min)$	1, 2, 3		
			340	$\mu A$	$-55^\circ C$				
$I_{EE}$	Power Supply Current	-48	-17	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	1, 2, 3		

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

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### Military Version (Continued)

#### AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	0.30	1.80	0.40	1.50	0.40	1.70	ns	<i>Figures 1 and 2</i>	1, 2, 3, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay Enable to Output	0.60	2.60	0.80	2.30	0.80	2.80	ns		
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns	<i>Figures 1 and 2</i>	4

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

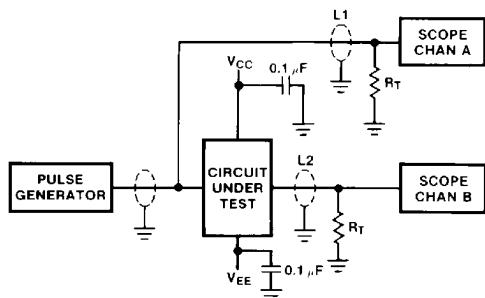
**Note 2:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.

**Note 4:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

**Note 5:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

#### Test Circuitry



TL/F/10580-5

**Notes:**

$V_{CC}, V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

L1 and L2 = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

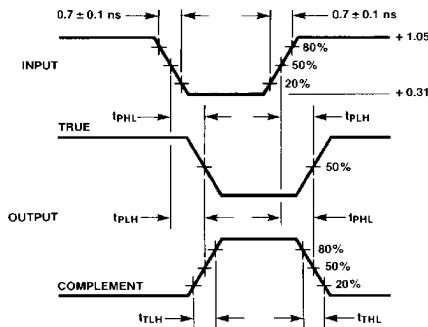
Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with  $50\Omega$  to GND

$C_L$  = Fixture and stray capacitance  $\leq 3 pF$

FIGURE 1. AC Test Circuit

#### Switching Waveforms



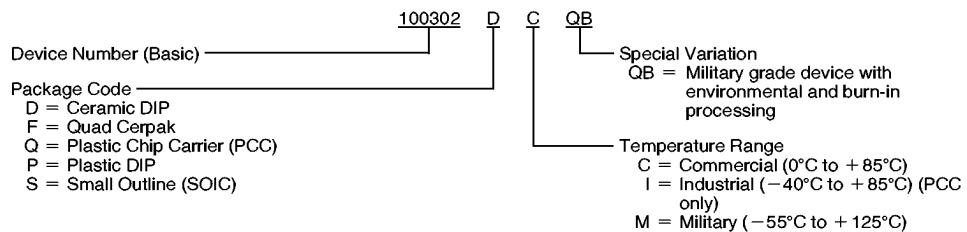
TL/F/10580-6

FIGURE 2. Propagation Delay and Transition Times

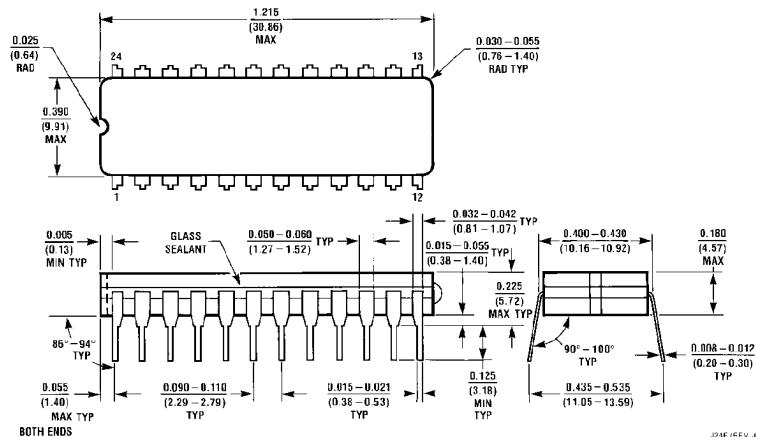
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### Ordering Information

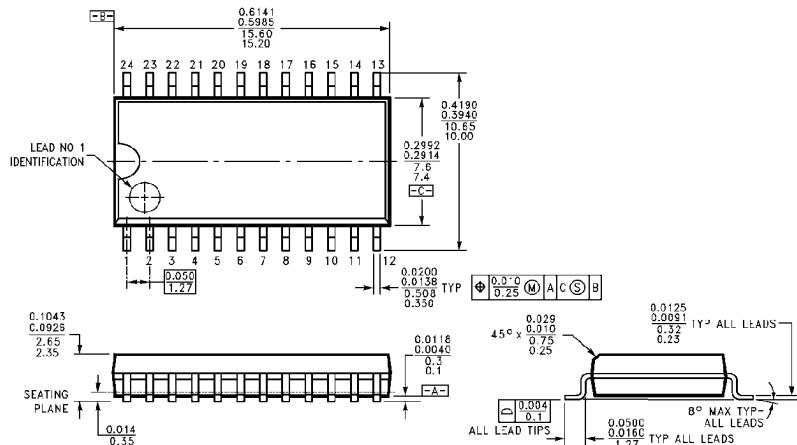
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



### Physical Dimensions inches (millimeters)



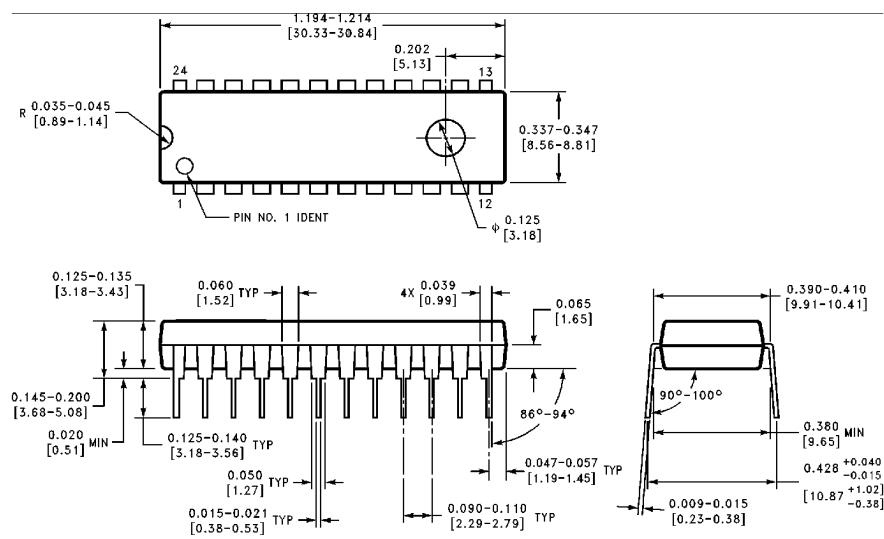
24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)  
NS Package Number J24E



24-Lead Molded Package (0.300" Wide) (S)  
NS Package Number M24B

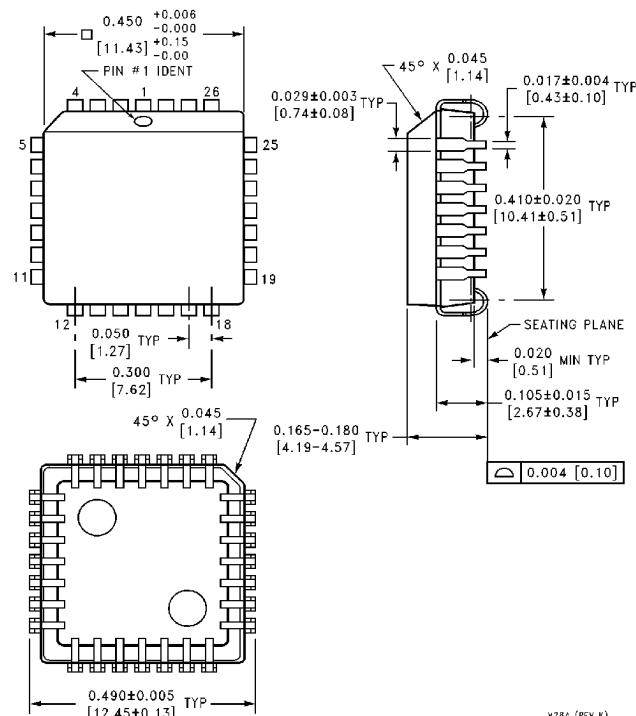
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**Physical Dimensions** inches (millimeters) (Continued)



N24E (REV A)

**24-Lead Plastic Dual-In-Line Package (P)  
NS Package Number N24E**



V28A (REV K)

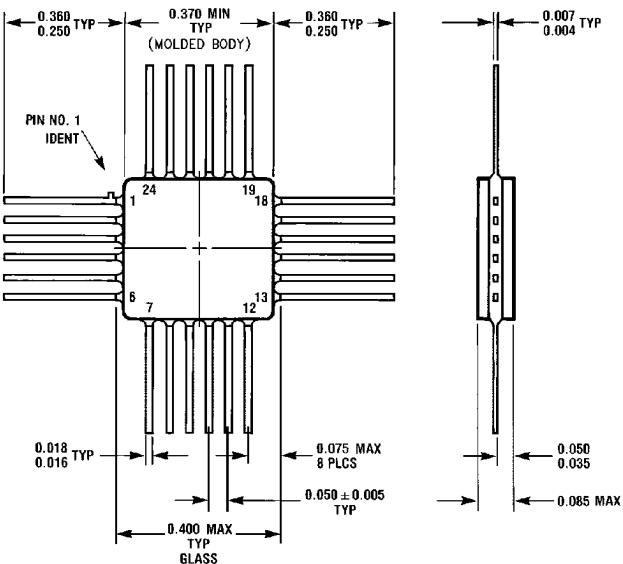
**28-Lead Plastic Chip Carrier (Q)  
NS Package Number V28A**

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## 100302 Low Power Quint 2-Input OR/NOR Gate

### Physical Dimensions inches (millimeters) (Continued)

Lit. # 114901



W24B (REV D)

24-Lead Quad Cerpak (F)  
NS Package Number W24B

#### LIFE SUPPORT POLICY

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