Product Brief

Bipolar Integrated Technology Inc.

HIPPI Interface Chip Set

(32-Bit)

B2020 - HIPPI Source Interface Chip
B2021 - HIPPI Destination Interface Chip

The B2020 and B2021 are BIT's implementation of the single chip Parallel HIPPI Source and Destination Interfaces. They provide the data path and control logic and the drivers and receivers for a complete 32-bit Parallel HIPPI link.

Features:

- Functional compliance with ANSI X3T9.3 HIPPI-PH Specifications Rev. 8.0.
- Excellent timing characteristics allowing for ease of design.
- Efficient power and thermal characteristics.
- 32-bit data channel.
- Single channel data rate of 800 megabits per second.
- Data and control signal sequencing in accordance with the HIPPI Physical Framing Hierarchy.
- Automatic division of data into HIPPI bursts.
- Automatic LLRC and LLRC parity generation.
- Automatic LLRC and parity checking.
- Capable of handling up to 65,535 look-ahead ready pulses.
- Differential 10K ECL HIPPI link interface.
- Single-ended TTL host interface.
- Seamless interface to external FIFO's.
- Self-test diagnostic modes of operation.
- Maximum Request/Connection latency of 600 ns (not counting destination host response time).
- Maximum data latency of 400 ns.
- 225-lead pin-grid-array package.

General Description:

The B2020 and B2021 provide complete functionality for interfacing a source host device to a destination host device across a 32-bit Parallel HIPPI link.

The B2020 is designed to receive data and parity from a source FIFO and control information from the source FIFO and source host logic. It automatically controls the interconnect, request/connection, and data transmission sequences to operate within the HIPPI specifications. It blocks the received data and parity into HIPPI bursts, automatically generates the Length/Longitudinal Redundancy (LLRC) check word and the LLRC parity, and transmits the data, parity, and source-to-destination control signals across the HIPPI link. It receives and synchronizes the destination-to-source control signals and uses them for interconnect, connect, and source data flow control.

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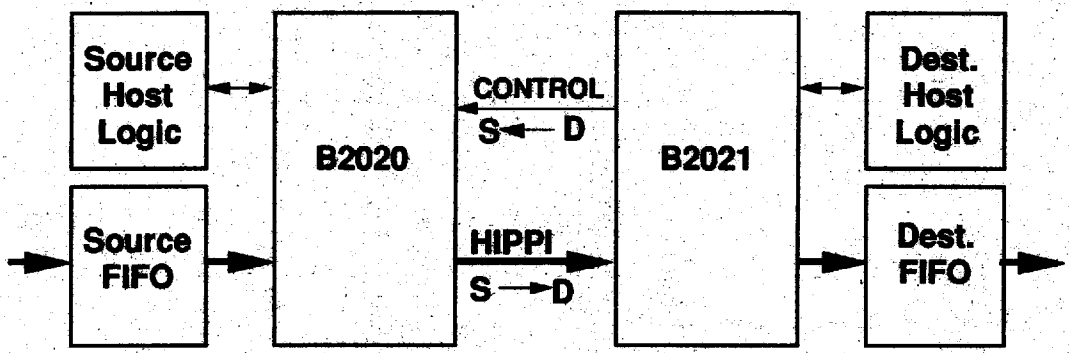
BIT HIPPI Interface Chip Set



32-Bit Parallel HIPPI Link

Functional Description:

The B2021 is designed to receive HIPPI data, parity, and source-to-destination control signals and synchronize them to the destination clock. It uses the control signals to determine how to treat the received data and parity and automatically checks the parity of HIPPI I-Field, burst, and LLRC data and checks the LLRC word at the end of each burst. It also keeps track of the number of burst sized buffers available at the destination and generates the appropriate number of look-ahead ready pulses to the source for data flow control. It communicates with the destination host logic in performing the HIPPI request/ connection sequences and in controlling the reception of data and parity into the destination FIFO. The destination synchronization circuit contains an elastic buffer that allows the received HIPPI signals to slip, jitter, or drift back and forth with relation to the destination clock without losing data or control information.

These chips are fabricated with BIT's unique VLSI process that allows for a high level of density and integration while consuming power levels comparable to BICMOS processes.

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