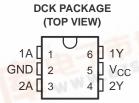
## SN74LVC2G06-EP DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES660-JUNE 2006

#### **FEATURES**

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication
     Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Supports 5-V V<sub>CC</sub> Operation
- Max t<sub>nd</sub> of 4.6 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### **DESCRIPTION/ORDERING INFORMATION**

This dual inverter buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The output of the SN74LVC2G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>	COM	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOT (SC-70) - DCK	Tape and reel	SN74LVC2G06MDCKREP	СТО

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	
5 th 124	Н

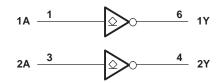


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#### **LOGIC DIAGRAM (POSITIVE LOGIC)**



### **Absolute Maximum Ratings**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (2)	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high-imp	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>				V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>				°C/W
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

 <sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
 (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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## Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT	
V	Complement	Operating	1.65	5.5	V	
$V_{CC}$	Supply voltage	Data retention only	1.5	1.5		
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
V	High level input veltege	$V_{CC}$ = 2.3 V to 2.7 V	1.7		V	
$V_{IH}$	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
V	Low-level input voltage	$V_{CC}$ = 2.3 V to 2.7 V		0.7	V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		0.8	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
$V_{I}$	Input voltage		0	5.5	V	
$V_{O}$	Output voltage		0	5.5	V	
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA	
		V <sub>CC</sub> = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5		
T <sub>A</sub>	Operating free-air temperature		-55	125	°C	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CON	NDITIONS	V <sub>cc</sub>	MIN TYP(1)	MAX	UNIT	
		I <sub>OL</sub> = 100 μA		1.65 V to 5.5 V		0.1		
		I <sub>OL</sub> = 4 mA		1.65 V		0.45		
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		I <sub>OL</sub> = 8 mA		2.3 V	0.3			
V <sub>OL</sub>		I <sub>OL</sub> = 16 mA		3 V	0.4		V	
		I <sub>OL</sub> = 24 mA		3 V		0.55		
		I <sub>OL</sub> = 32 mA		4.5 V	0.55			
I	A inputs	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V		±5	μΑ	
I <sub>off</sub>		$V_I$ or $V_O = 5.5 \text{ V}$		0		±10	μΑ	
I <sub>CC</sub>		$V_I = 5.5 \text{ V or GND},$	I <sub>O</sub> = 0	1.65 V to 5.5 V		10	μΑ	
$\Delta I_{CC}$		One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μΑ	
Ci		$V_I = V_{CC}$ or GND		3.3 V	3.5		pF	

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

## SN74LVC2G06-EP DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

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### **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		$V_{CC}$ = 2.5 V $\pm$ 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INFOT)		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Y	1.8	9.1	0.9	5.7	0.9	4.6	0.7	3.9	ns

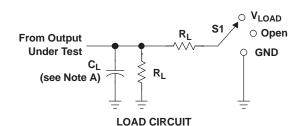
## **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	2	2	3	4	pF

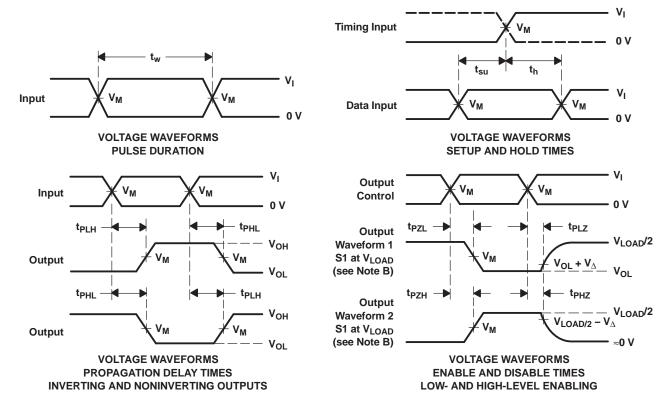


# PARAMETER MEASUREMENT INFORMATION (Open Drain)



TEST	<b>S</b> 1
t <sub>PZL</sub> (see Notes E and F)	$V_{LOAD}$
t <sub>PLZ</sub> (see Notes E and G)	$V_{LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	$V_{LOAD}$

	IN	INPUT V <sub>I</sub> t <sub>r</sub> /t <sub>f</sub>			_		
V <sub>CC</sub>	VI			V <sub>LOAD</sub>	CL	$R_L$	$oldsymbol{V}_{\Delta}$
1.8 V $\pm$ 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤ <b>2.5</b> ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	V <sub>CC</sub>	≤ <b>2.5</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	<b>500</b> Ω	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. Since this device has open-drain outputs, t<sub>PLZ</sub> and t<sub>PZL</sub> are the same as t<sub>pd</sub>.
  - F. t<sub>PZL</sub> is measured at V<sub>M</sub>.
  - G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

#### PACKAGE OPTION ADDENDUM

2-Feb-2009

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins P	ackage Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC2G06MDCKREP	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM
V62/06640-01XE	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC2G06-EP:

Catalog: SN74LVC2G06

Automotive: SN74LVC2G06-Q1

NOTE: Qualified Version Definitions:

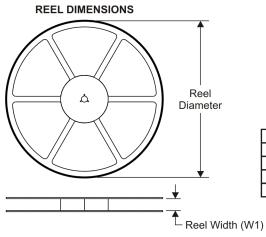
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects



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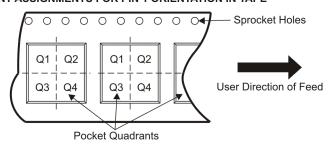
#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

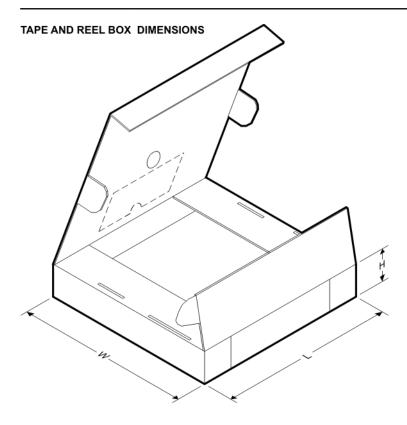
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G06MDCKREP	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3





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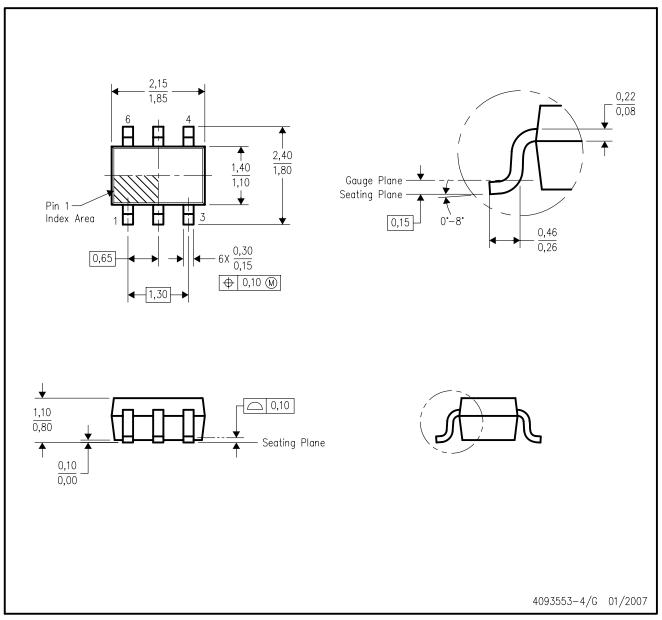


#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G06MDCKREP	SC70	DCK	6	3000	203.0	203.0	35.0

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE

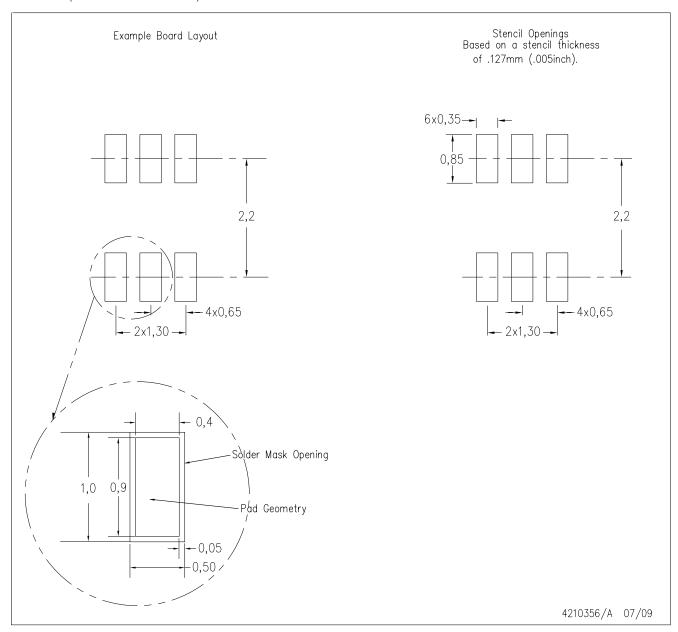


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.



## DCK (R-PDSO-G6)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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