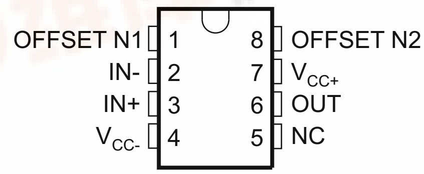
FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree[(1)]**
- **Outstanding Combination of DC Precision and AC Performance:**
  - **Unity-Gain Bandwidth . . . 13 MHz Typ**
  - **V_n . . . 3.3 nV/√Hz at f = 10 Hz Typ, 2.5 nV/√Hz at f = 1 kHz Typ**
  - **V_{IO} . . . 100 µV Max**
  - **A_{VD} . . . 45 V/µV Typ With R_L = 2 kΩ, 19 V/µV Typ With R_L = 600 Ω**
- **Available in Standard-Pinout Small-Outline Package**
- **Output Features Saturation Recovery Circuitry**
- **Macromodels and Statistical information**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



DESCRIPTION

The TLE2027 contains innovative circuit design expertise and high-quality process control techniques to produce a level of ac performance and dc precision previously unavailable in single operational amplifiers. Manufactured using TI's state-of-the-art Excalibur process, these devices allow upgrades to systems that use lower-precision devices.

In the area of dc precision, the TLE2027 offers maximum offset voltages of 100 µV, common-mode rejection ratio of 131 dB (typ), supply voltage rejection ratio of 144 dB (typ), and dc gain of 45 V/µV (typ).

The ac performance of the TLE2027 is highlighted by a typical unity-gain bandwidth specification of 15 MHz, 55° of phase margin, and noise voltage specifications of 3.3 nV/√Hz and 2.5 nV/√Hz at frequencies of 10 Hz and 1 kHz, respectively.

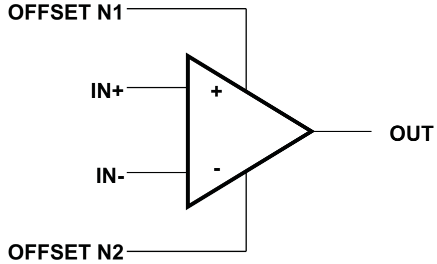
The TLE2027 is available in a wide variety of packages, including the industry-standard 8-pin small-outline version for high-density system applications. The device is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION[(1)]

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES
		SMALL OUTLINE[(2)] (D)
–55°C to 125°C	100 µV	TLE2027MDREP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The D package is available taped and reeled with 2500 units/reel.

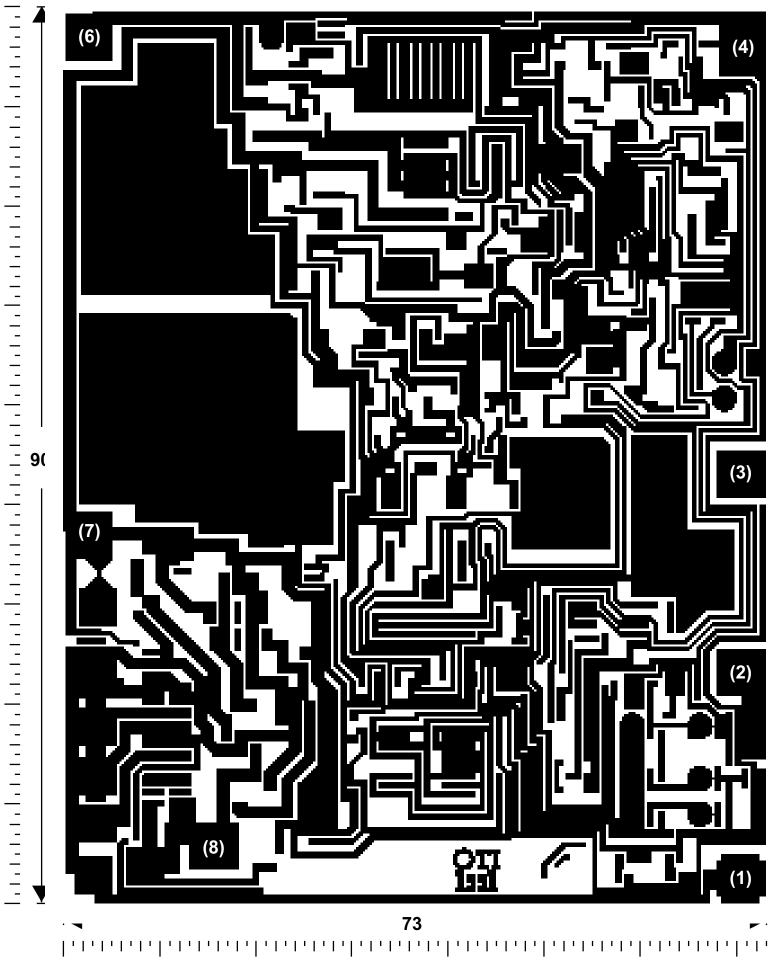
SYMBOL

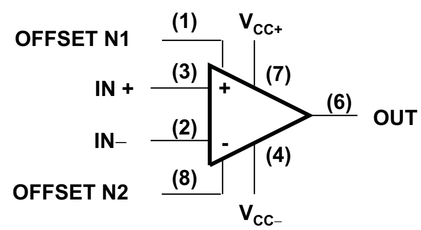


TLE202XY CHIP INFORMATION

This chip, when properly assembled, displays characteristics similar to the TLE202xC. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Chip Thickness: 15 Mils Typical

Bonding Pads: 4 × 4 Mils Minimum

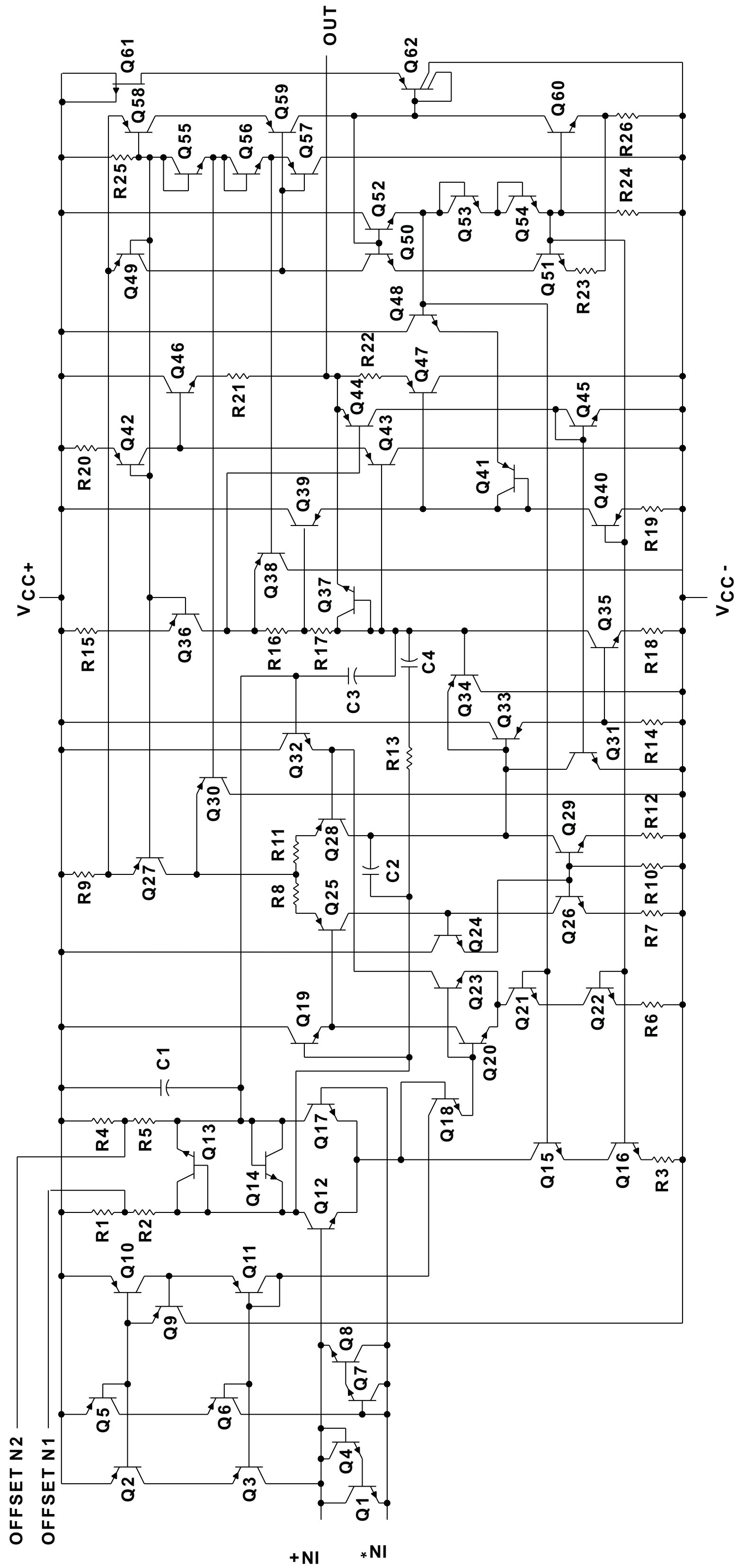
$T_J$max = 150°C

Tolerances Are ±10%.

All Dimensions Are in Mils.

Pin (4) is Internally Connected to Backside of Chip.

EQUIVALENT SCHEMATIC



ACTUAL DEVICE COMPONENT COUNT	
Transistors	61
Resistors	26
epiFET	1
Capacitors	4

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			19	V
V_{CC-}	Supply voltage			–19	V
V_{ID}	Differential input voltage(3)			±1.2	V
V_I	Input voltage range (any input)			$V_{CC\pm}$	
I_I	Input current (each input)			±1	mA
I_O	Output current			±50	mA
	Total current into V_{CC+}			50	mA
	Total current out of V_{CC-}			50	mA
	Duration of short-circuit current at (or below) 25°C(4)		Unlimited		
	Continuous total power dissipation		See Dissipation Rating Table		
T_A	Operating free-air temperature range		–55	125	°C
T_{stg}	Storage temperature range(5)		–65	150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s	D package		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
(3) Differential voltages are at IN+ with respect to IN–. Excessive current flows if a differential input voltage in excess of approximately ±1.2 V is applied between the inputs, unless some limiting resistance is used.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
(5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced product packaging.

Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW	145 mW

Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±4	±19	V
V_{IC}	Common-mode input voltage	$T_A = 25°C$	–11	11	V
		T_A = Full range(1)	–10.3	10.3	
T_A	Operating free-air temperature		–55	125	°C

(1) Full range is –55°C to 125°C.

Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		20	100	μV
			Full range			200	
$α_{VIO}$	Temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 50 Ω	Full range		0.4		μV/°C
	Input offset voltage long-term drift (2)	V_{IC} = 0, R_S = 50 Ω	25°C		0.006		μV/mo
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	25°C		6	90	nA
			Full range			150	
I_{IB}	Input bias current	V_{IC} = 0, R_S = 50 Ω	25°C		15	90	nA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	–11 to 11	–13 to 13		V
			Full range	–10.3 to 10.3			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 600 Ω	25°C	10.5	12.9		V
			Full range	10			
		R_L = 2 kΩ	25°C	12	13.2		
			Full range	11			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 600 Ω	25°C	–10.5	–13		V
			Full range	–10			
		R_L = 2 kΩ	25°C	–12	–13.5		
			Full range	–11			
A_{VD}	Large-signal differential voltage amplification	V_O = ±11 V, R_L = 2 kΩ	25°C	5	45		V/μV
		V_O = ±10 V, R_L = 2 kΩ	Full range	2.5			
		V_O = ±10 V, R_L = 1 kΩ	25°C	3.5	38		
			Full range	1.8			
		V_O = ±10 V, R_L = 600 Ω	25°C	2	19		
C_i	Input capacitance		25°C		8		pF
z_o	Open-loop output impedance	I_O = 0	25°C		50		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	100	131		dB
			Full range	96			
k_{SVR}	Supply-voltage rejection ratio ($ΔV_{CC\pm}/ΔV_{IO}$)	$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	25°C	94	144		dB
		$V_{CC\pm}$ = ±4 V to ±18 V, R_S = 50 Ω	Full range	90			
I_{CC}	Supply current	V_O = 0, No load	25°C		3.8	5.3	mA
			Full range			5.6	

(1) Full range is –55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

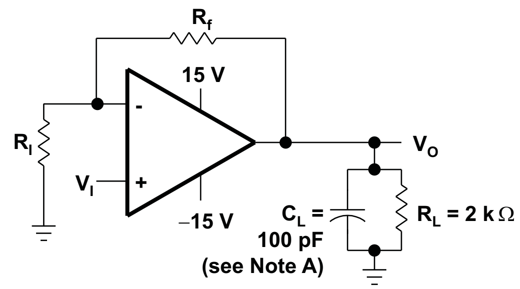
Operating Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		1.7	2.8		V/µs
		R_L = 2 kΩ, C_L = 100 pF, T_A = –55°C to 125°C, See Figure 1		1			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω	f = 10 Hz		3.3		nV/√Hz
			f = 1 kHz		2.5		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			50		nV
I_n	Equivalent input noise current	f = 10 Hz			1.5		pA/√Hz
		f = 1 kHz			0.4		
THD	Total harmonic distortion	V_O = 10 V, A_{VD} = 1 (1)			<0.002%		
B_1	Unity-gain bandwidth (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF			13		MHz
B_{OM}	Maximum output-swing bandwidth	R_L = 2 kΩ			30		kHz
φ_m	Phase margin at unity gain (see Figure 3)	R_L = 2 kΩ, C_L = 100 pF			55°		

(1) Measured distortion of the source used in the analysis was 0.002%.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

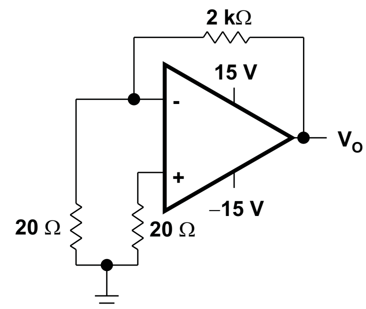
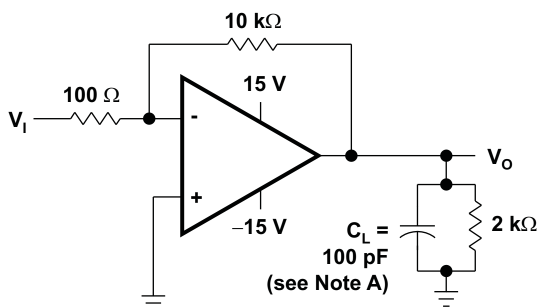
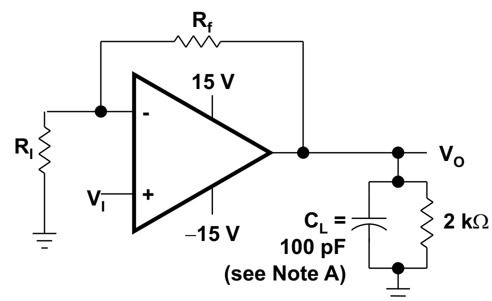


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

DEVICE INFORMATION

Typical Values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

Initial Estimates of Parameter Distributions

In the ongoing program of improving data sheets and supplying more information to our customers, Texas Instruments has added an estimate of not only the typical values but also the spread around these values. These are in the form of distribution bars that show the 95% (upper) points and the 5% (lower) points from the characterization of the initial wafer lots of this new device type (see Figure 5). The distribution bars are shown at the points where data was actually collected. The 95% and 5% points are used instead of ±3 sigma since some of the distributions are not true Gaussian distributions.

The number of units tested and the number of different wafer lots used are on all of the graphs where distribution bars are shown. As noted in Figure 5, there were a total of 835 units from two wafer lots. In this case, there is a good estimate for the within-lot variability and a possibly poor estimate of the lot-to-lot variability. This is always the case on newly released products since there can only be data available from a few wafer lots.

The distribution bars are not intended to replace the minimum and maximum limits in the electrical tables. Each distribution bar represents 90% of the total units tested at a specific temperature. While 10% of the units tested fell outside any given distribution bar, this should not be interpreted to mean that the same individual devices fell outside every distribution bar.

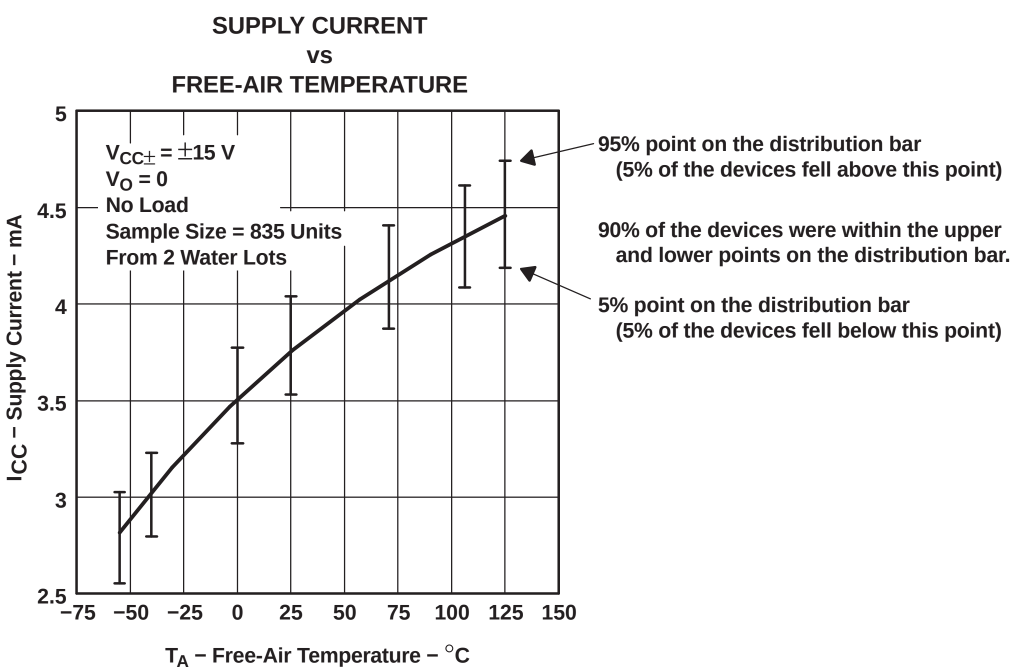


Figure 5. Sample Graph With Distribution Bars

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6,
ΔV_{IO}	Input offset voltage change	vs Time after power on	7, 8
I_{IO}	Input offset current	vs Free-air temperature	9
I_{IB}	Input bias current	vs Free-air temperature	10
		vs Common-mode input voltage	11
I_I	Input current	vs Differential input voltage	12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14
V_{OM}	Maximum (positive/negative) peak output voltage	vs Load resistance	15, 16
		vs Free-air temperature	17, 18
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	19
		vs Load resistance	20
		vs Frequency	21, 22
		vs Free-air temperature	23
z_o	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency	25
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	26
I_{OS}	Short-circuit output current	vs Supply voltage	27, 28
		vs Elapsed time	29, 30
		vs Free-air temperature	31, 32
I_{CC}	Supply current	vs Supply voltage	33
		vs Free-air temperature	34
	Voltage-follower pulse response	Small signal	35
		Large signal	36
V_n	Equivalent input noise voltage	vs Frequency	37
	Noise voltage (referred to input)	Over 10-s interval	38
B_1	Unity-gain bandwidth	vs Supply voltage	39
		vs Load capacitance	40
SR	Slew rate	vs Free-air temperature	41
φ_m	Phase margin	vs Supply voltage	42
		vs Loadcapacitance	43
		vs Free-air temperature	44

TYPICAL CHARACTERISTICS

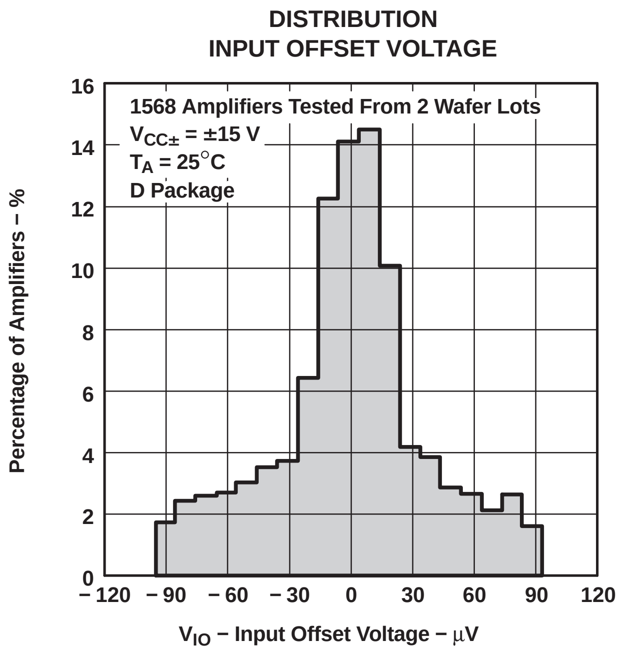


Figure 6.

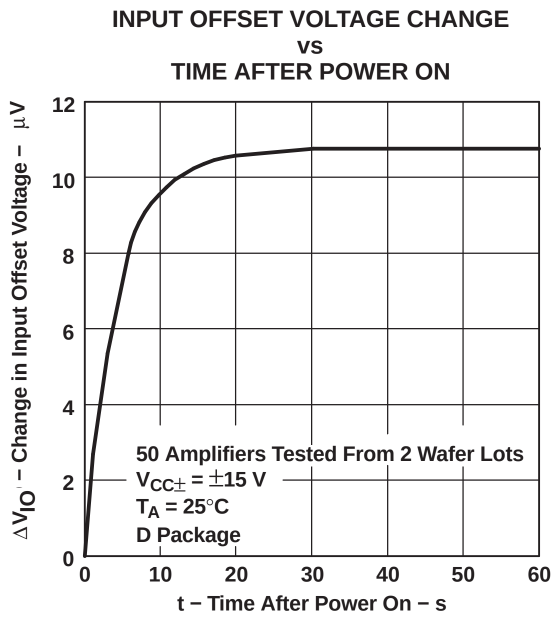


Figure 7.

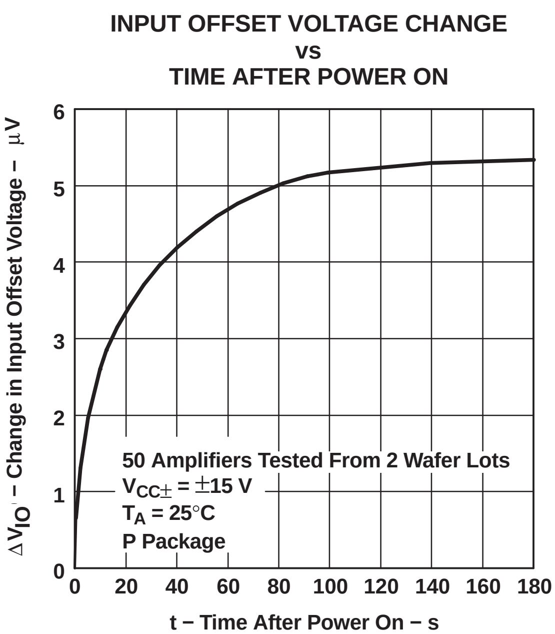
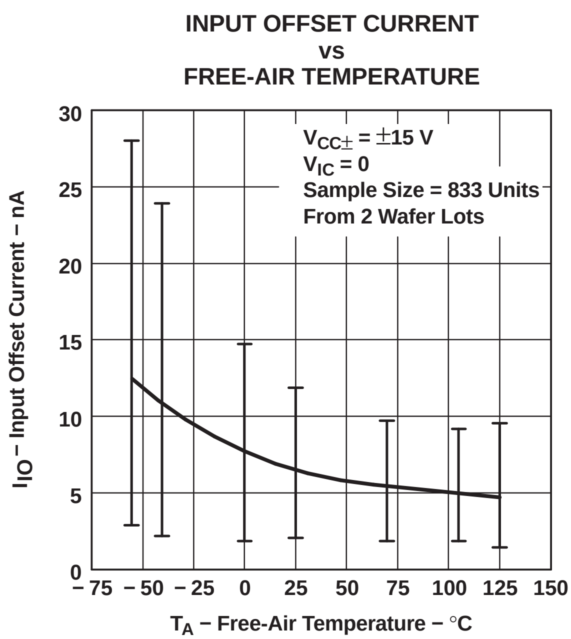


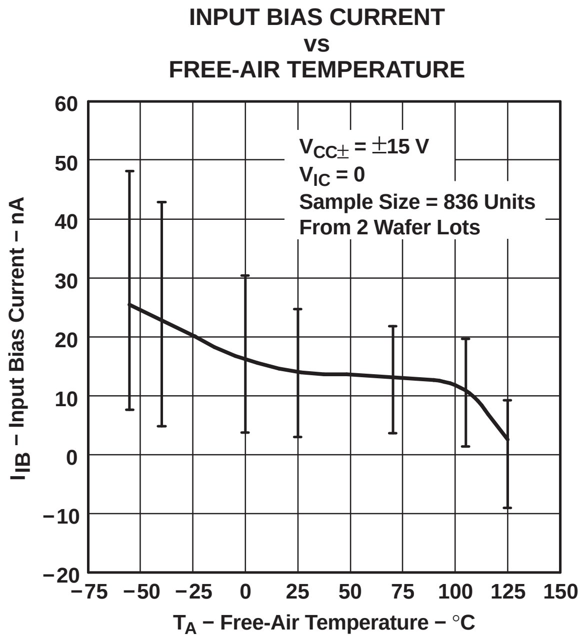
Figure 8.



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 9.

TYPICAL CHARACTERISTICS (continued)



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 10.

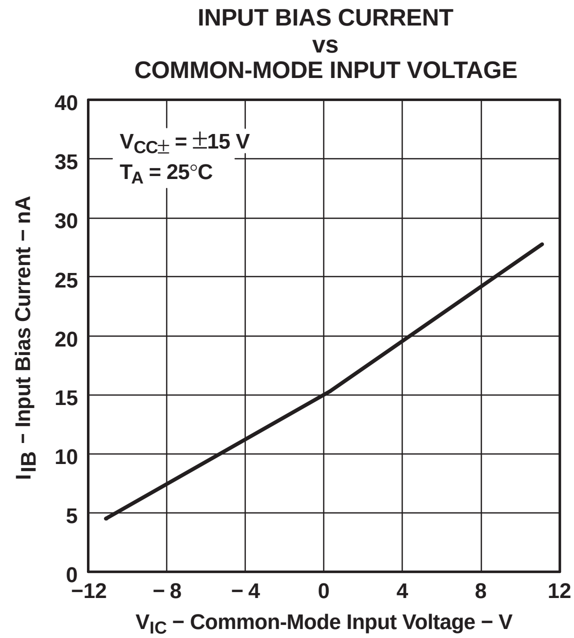


Figure 11.

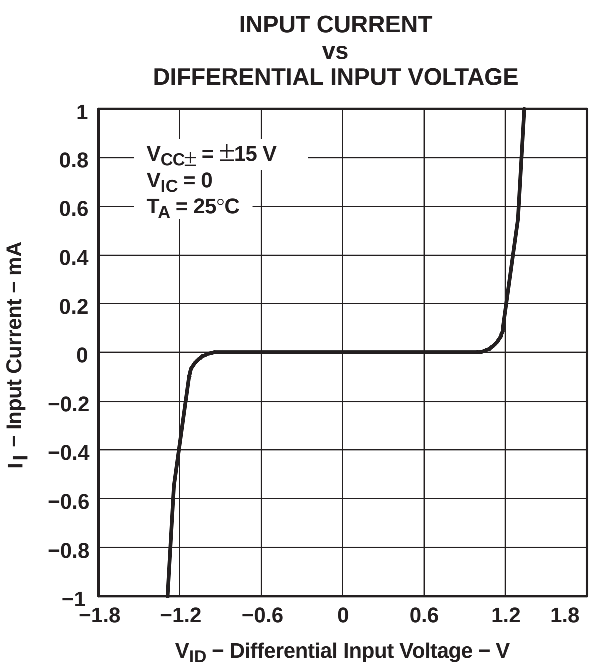
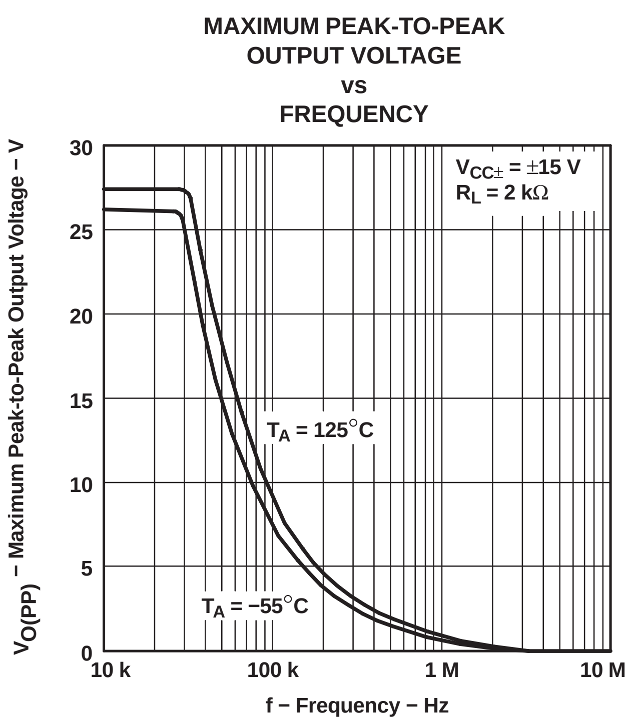


Figure 12.

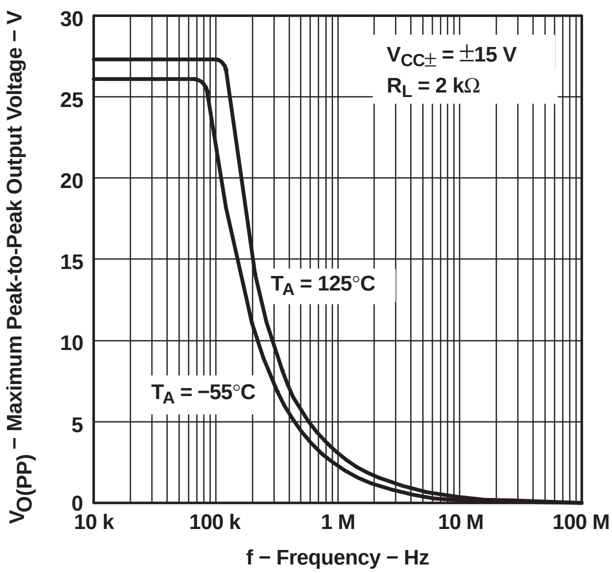


NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 13.

TYPICAL CHARACTERISTICS (continued)

TLE2037
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 14.

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

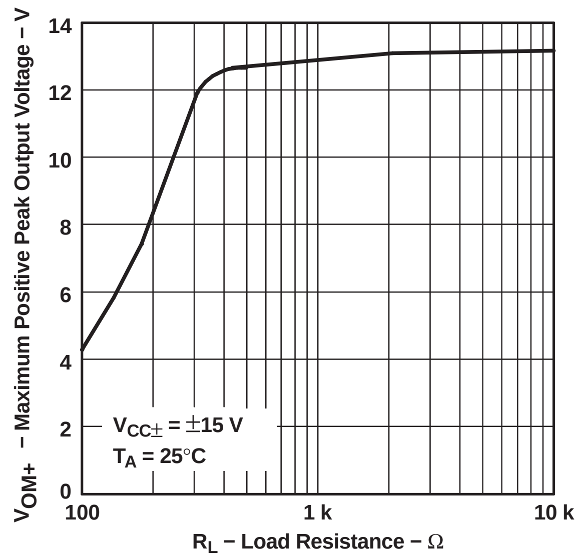


Figure 15.

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
LOAD RESISTANCE

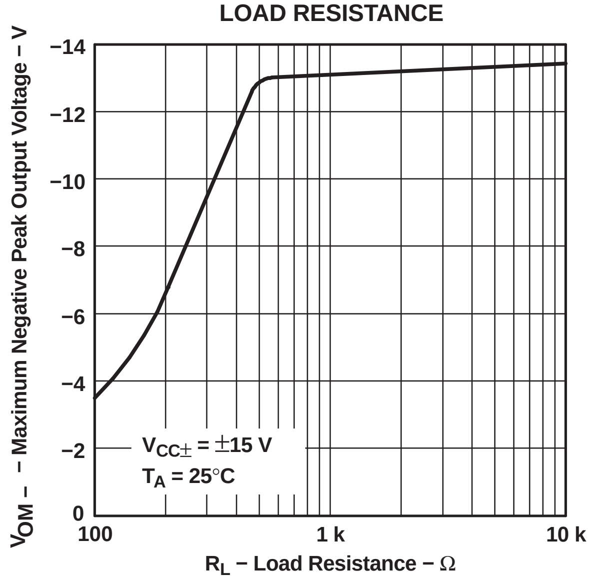
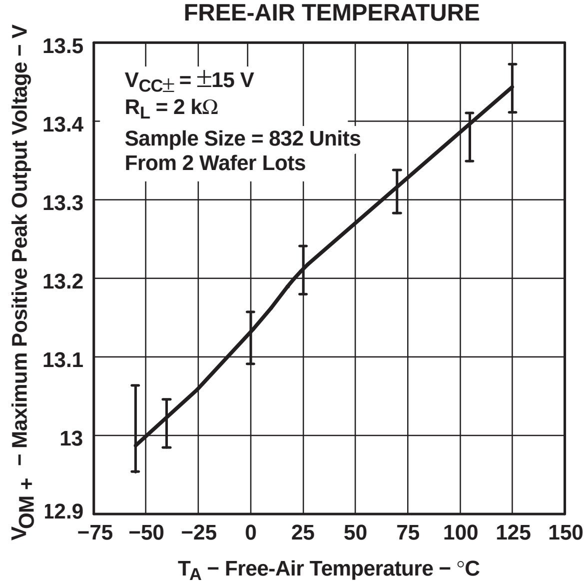


Figure 16.

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

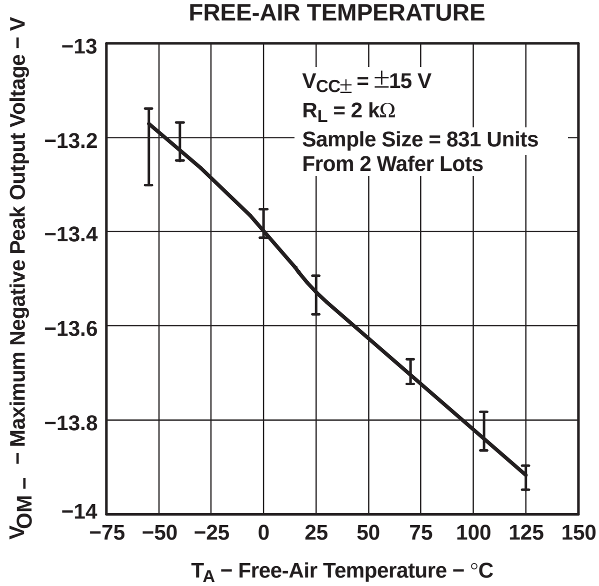


NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 17.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 18.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

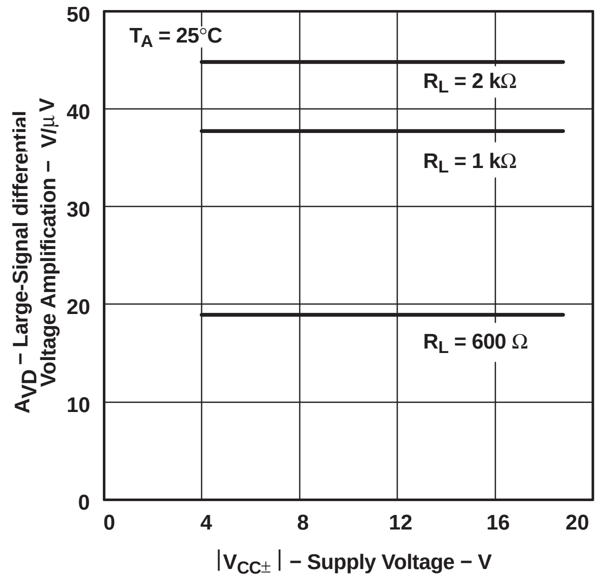


Figure 19.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

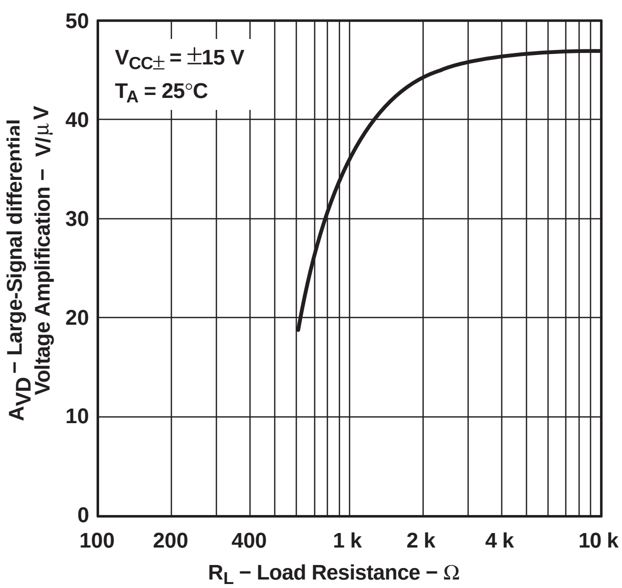


Figure 20.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

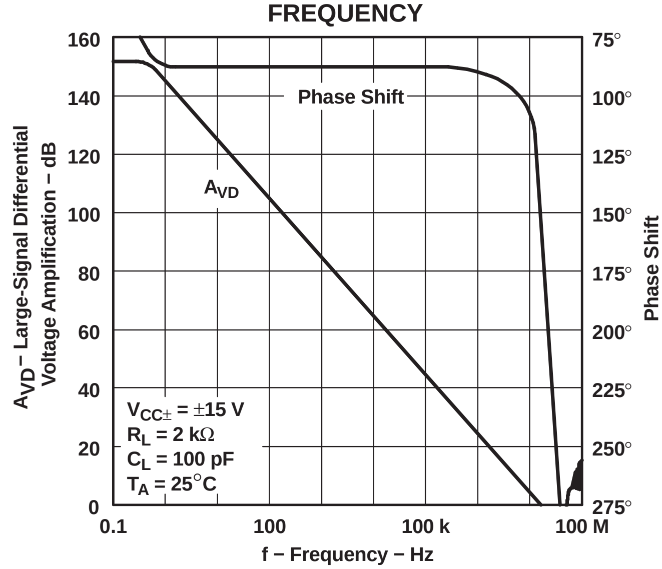


Figure 21.

TYPICAL CHARACTERISTICS (continued)

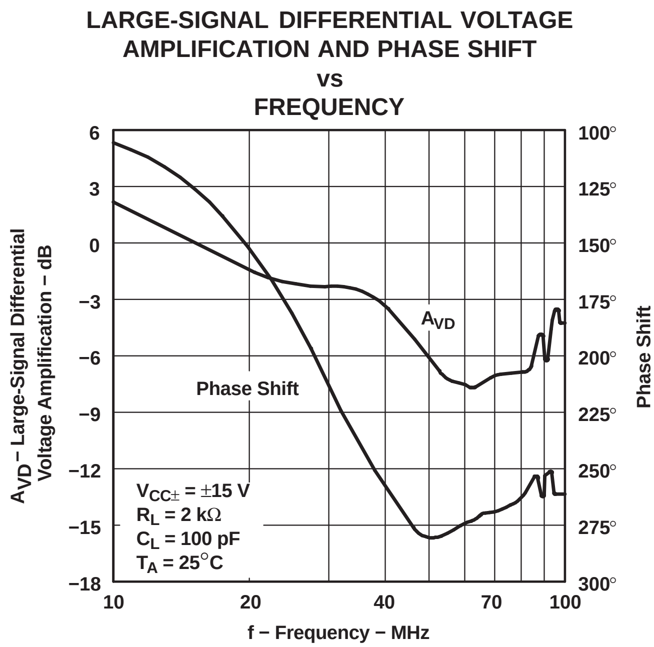
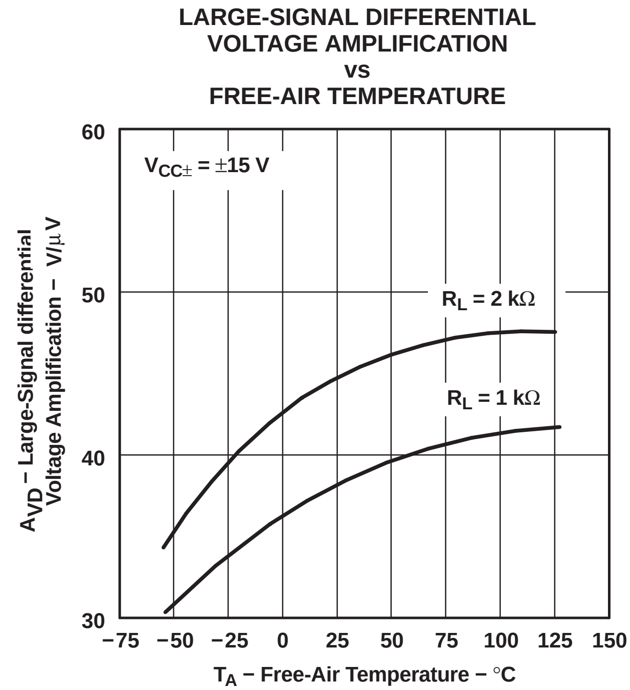
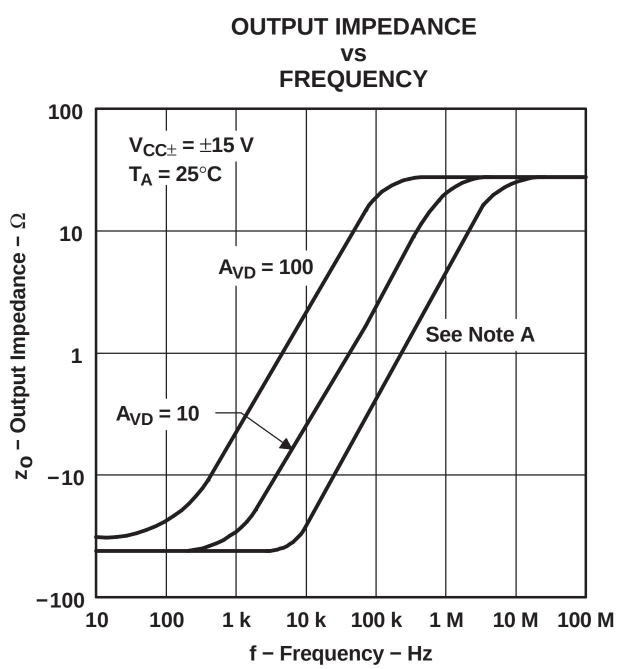


Figure 22.



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 23.



NOTE A: For this curve, A_{VD} = 1

Figure 24.

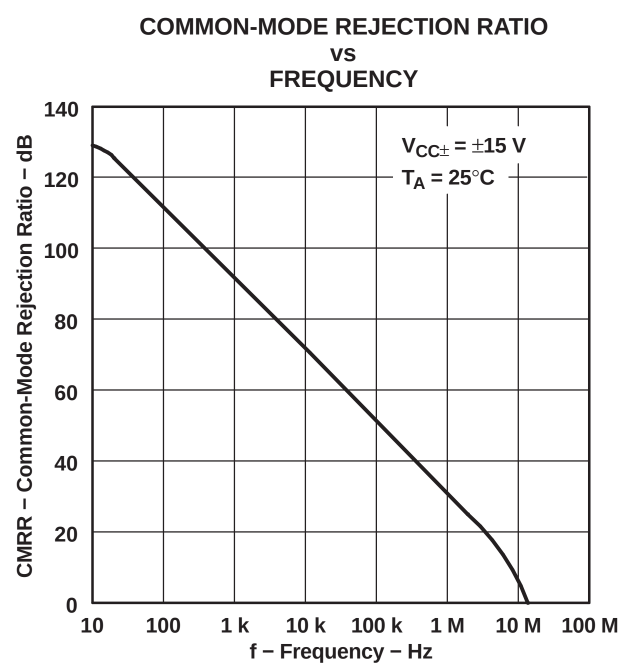


Figure 25.

TYPICAL CHARACTERISTICS (continued)

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

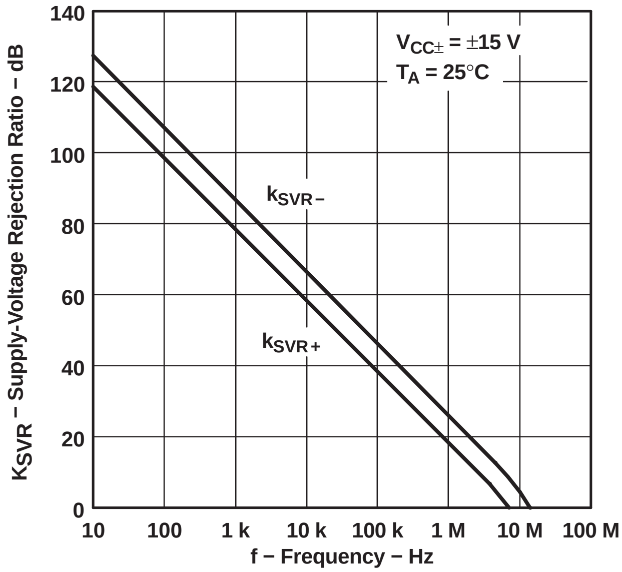


Figure 26.

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

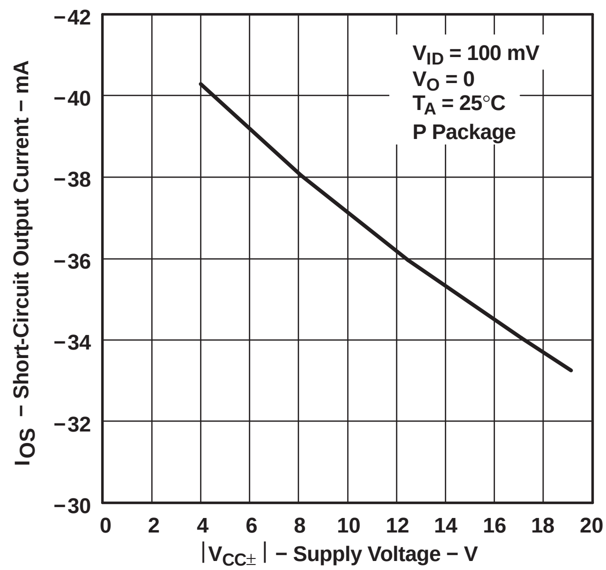


Figure 27.

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

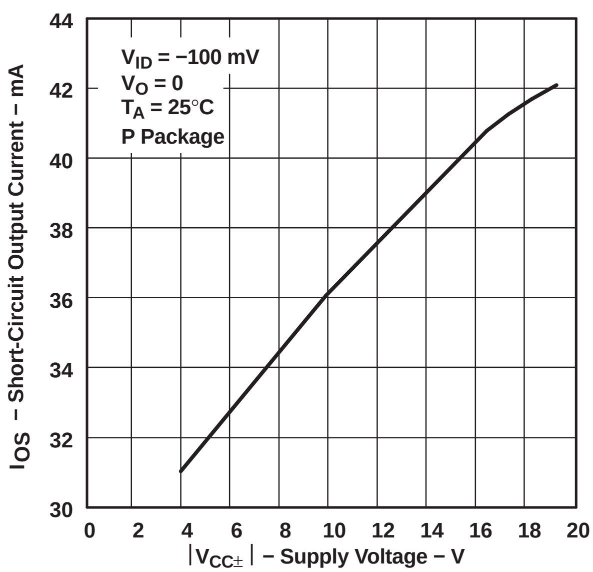


Figure 28.

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

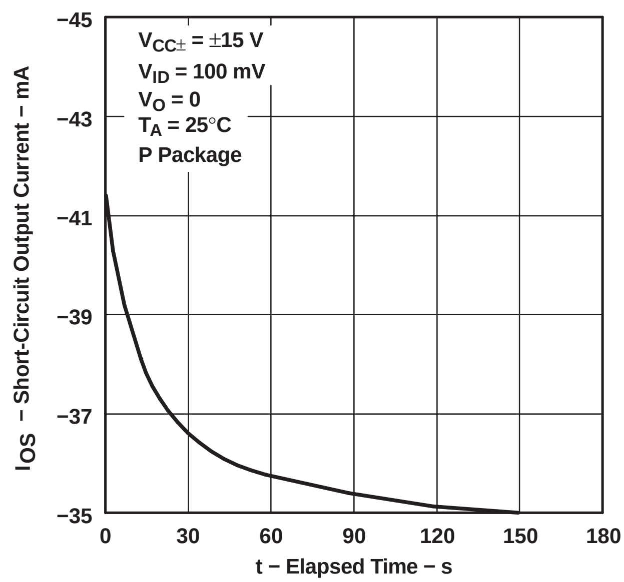


Figure 29.

TYPICAL CHARACTERISTICS (continued)

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

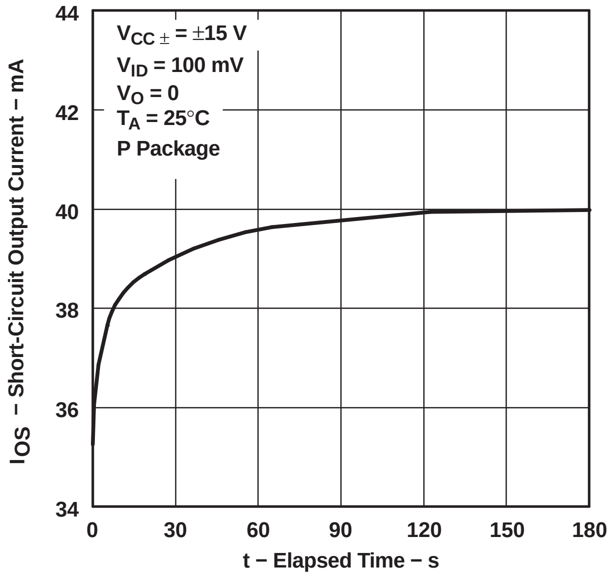
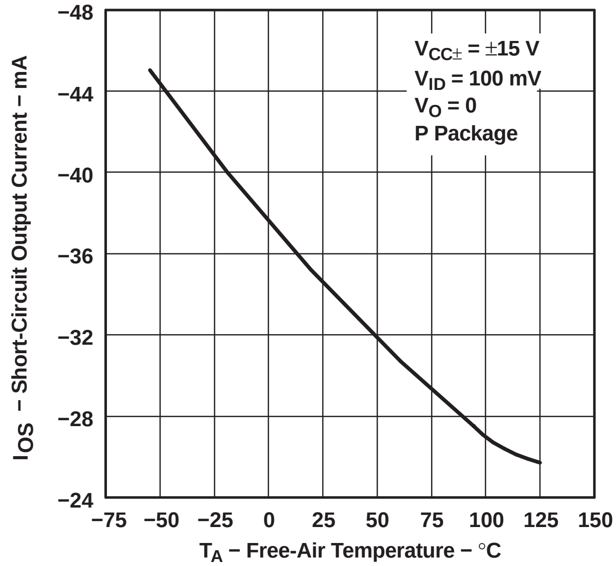


Figure 30.

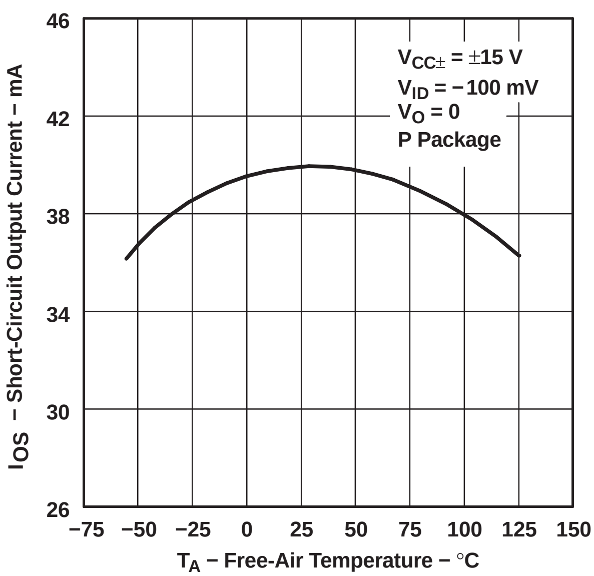
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 31.

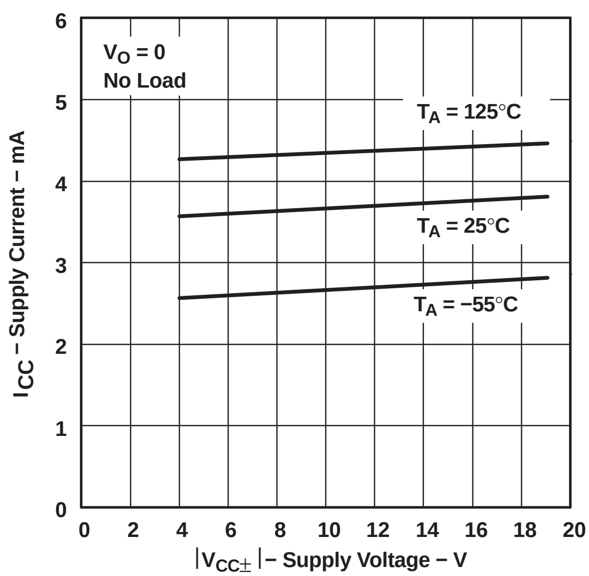
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 32.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

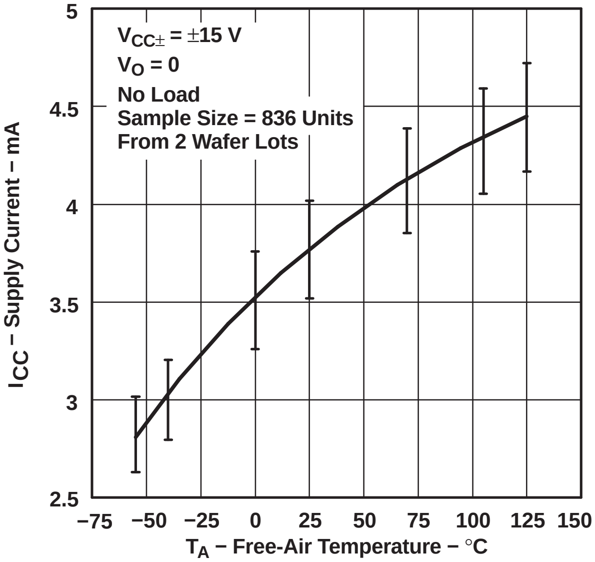


NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 33.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT vs FREE-AIR TEMPERATURE



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 34.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

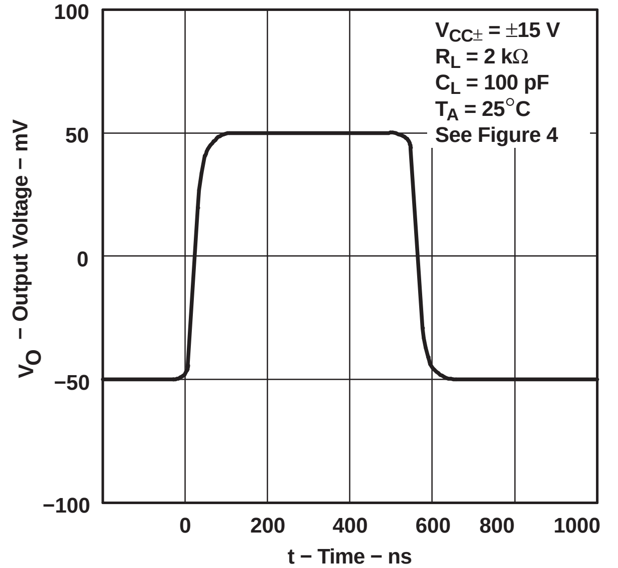


Figure 35.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

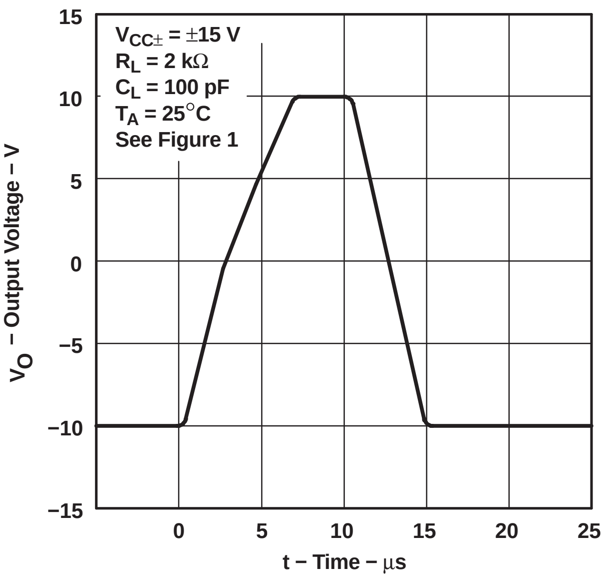


Figure 36.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

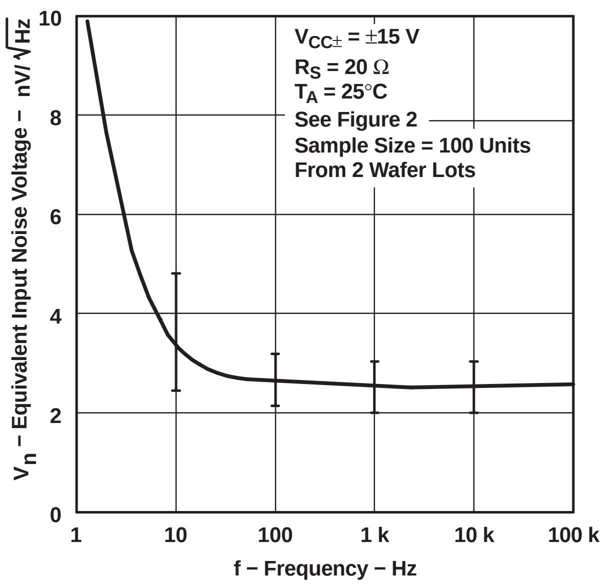


Figure 37.

TYPICAL CHARACTERISTICS (continued)

NOISE VOLTAGE
(REFERRED TO INPUT)
OVER A 10-S INTERVAL

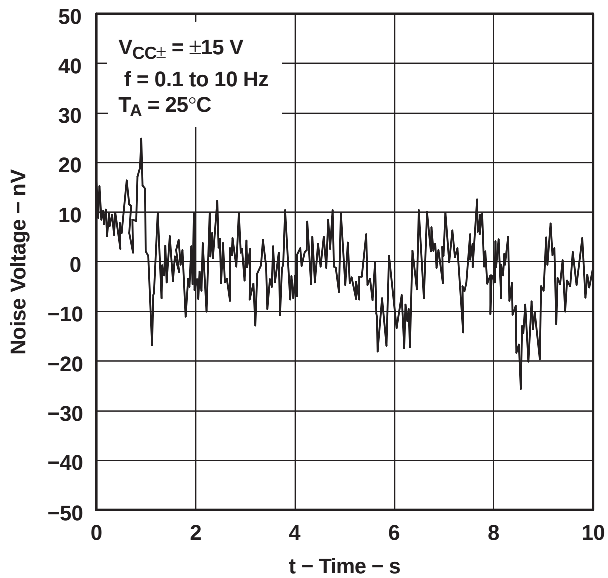


Figure 38.

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

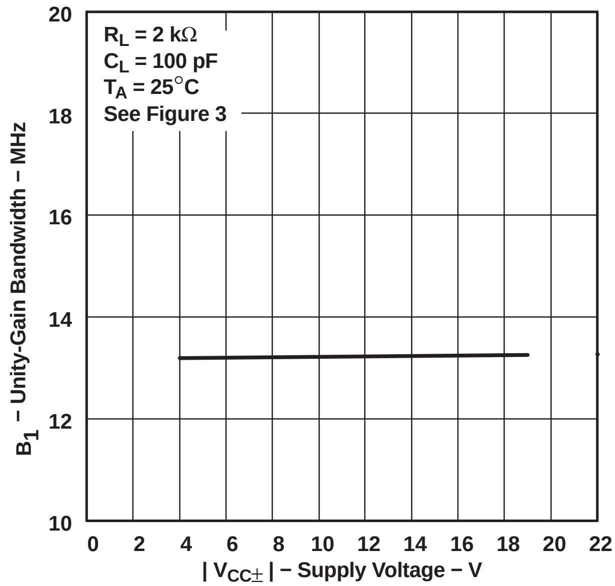


Figure 39.

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

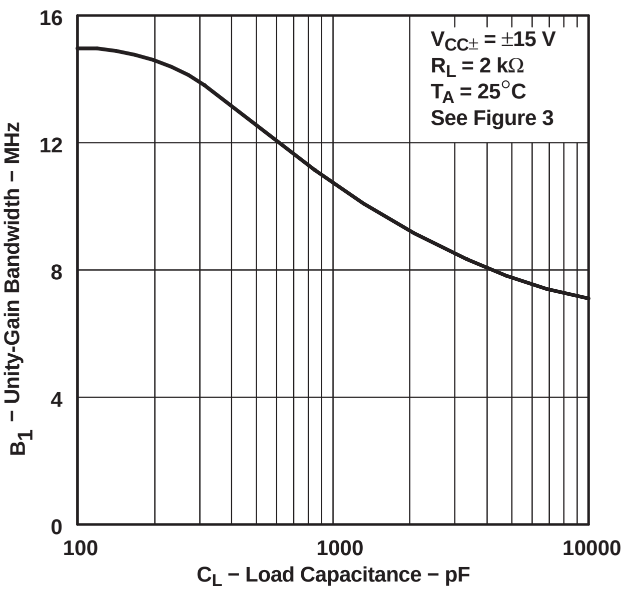
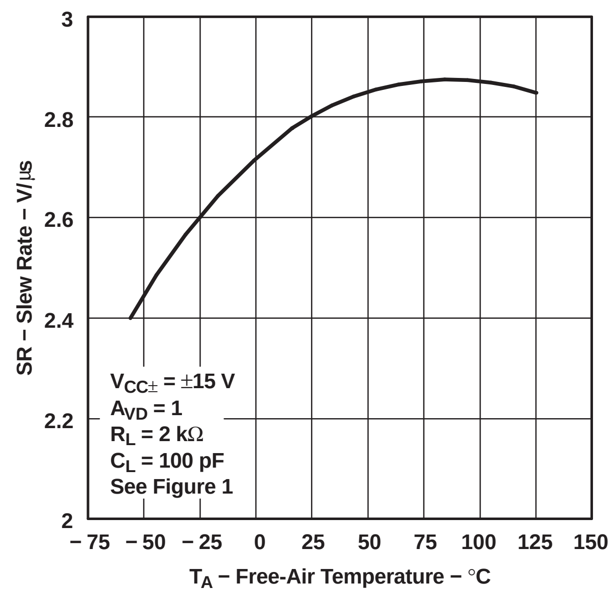


Figure 40.

SLEW RATE
vs
FREE-AIR TEMPERATURE



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 41.

TYPICAL CHARACTERISTICS (continued)

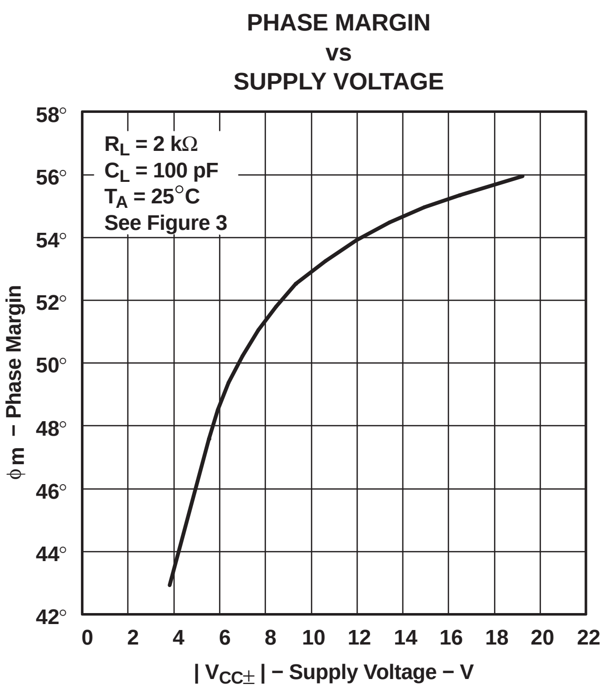


Figure 42.

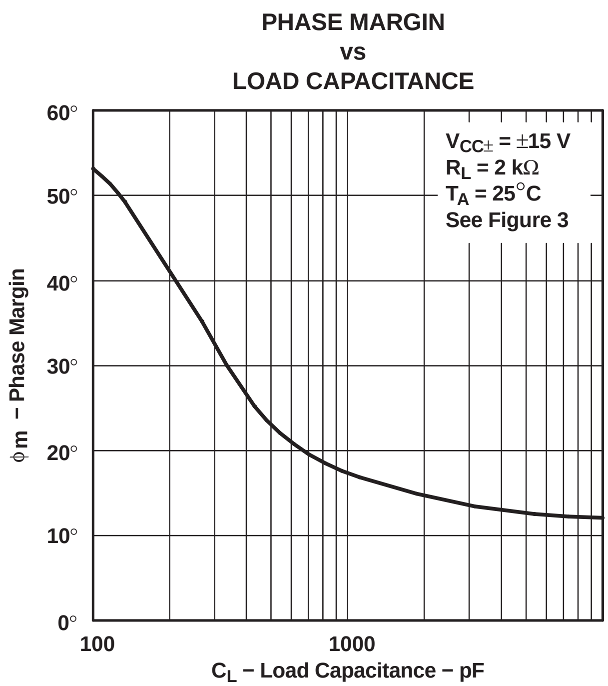
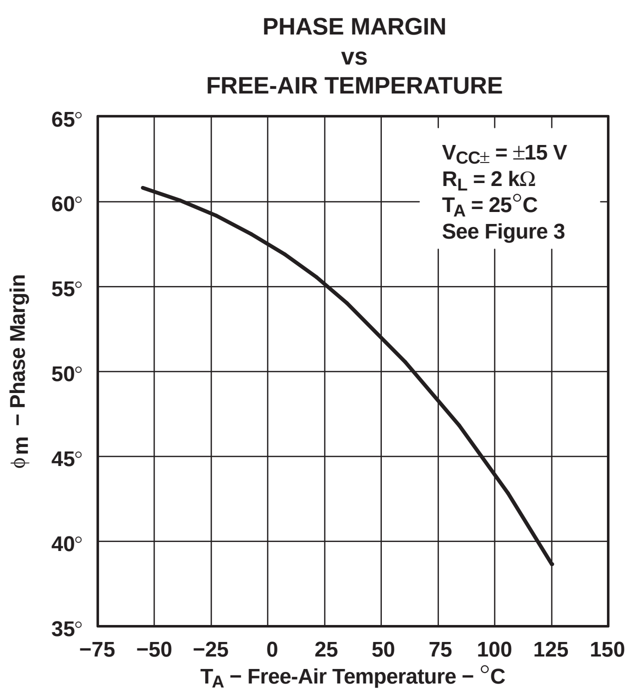


Figure 43.



NOTE A: Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Figure 44.

APPLICATION INFORMATION

Input Offset Voltage Nulling

The TLE2027 series offers external null pins that can be used to further reduce the input offset voltage. The circuits of Figure 45 can be connected as shown if the feature is desired. If external nulling is not needed, the null pins may be left disconnected.

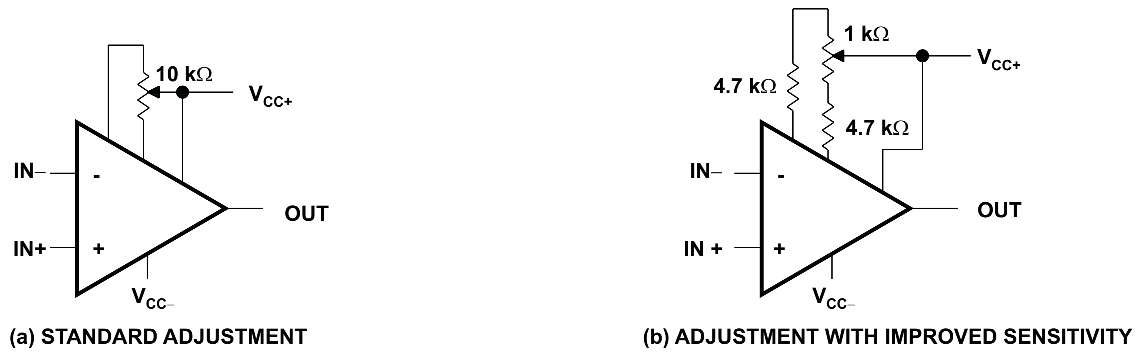


Figure 45. Input Offset Voltage Nulling Circuits

Voltage-Follower Applications

The TLE2027 circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. Also, this feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 kΩ, this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 46).

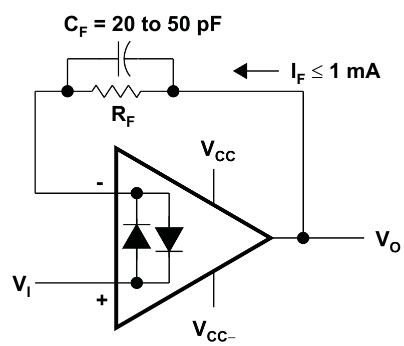


Figure 46. Voltage Follower

APPLICATION INFORMATION (continued)

Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel (see Note and Figure 47) and subcircuit (see Figure 48) were generated using the TLE202x7 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE:

G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

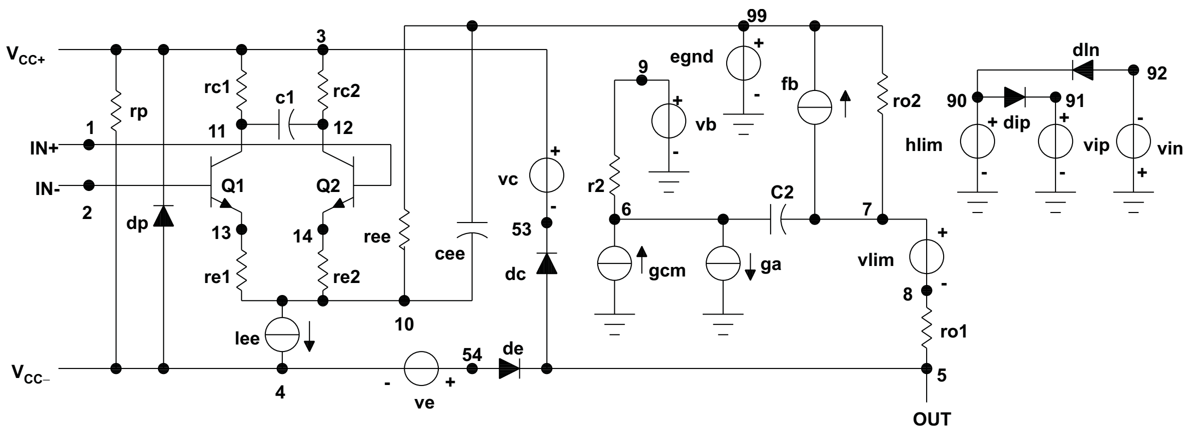


Figure 47. Boyle Macromodel

```
.subckt TLE2027 1 2 3 4 5
*
  c1      11   12   4.003E-12
  c2       6    7   20.00E-12
  dc       5   53   dz
  de      54    5   dz
  dlp     90   91   dz
  dln     92   90   dx
  dp       4    3   dz
  egnd    99    0   poly(2) (3,0)
(4,0) 0 5 .5
  fb       7   99   poly(5) vb vc ve
vlp vln 0 954.8E6 -1E9 1E9 1E9 -1E9
  ga       6    0   11  12
2.062E-3
  gcm      0    6   10  99
531.3E-12
  iee     10    4   dc  56.01E-6
  hlim    90    0   vlim 1K
  q1      11    2   13 qx
  q2      12    1   14 qx
  r2       6    9   100.0E3
  rc1      3   11   530.5
  rc2      3   12   530.5
  re1     13   10   -393.2
  re2     14   10   -393.2
  ree     10   99   3.571E6
  ro1      8    5   25
  ro2      7   99   25
  rp       3    4   8.013E3
  vb       9    0   dc  0
  vc       3   53   dc  2.400
  ve      54    4   dc  2.100
  vlim     7    8   dc  0
  vlp     91    0   dc  40
  vln      0   92   dc  40
.modeldx D(Is=800.0E-18)
.modelqx NPN(Is=800.0E-18
Bf=7.000E3)
.ends
```

Figure 48. TLE2027 Macromodel Subcircuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLE2027MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06674-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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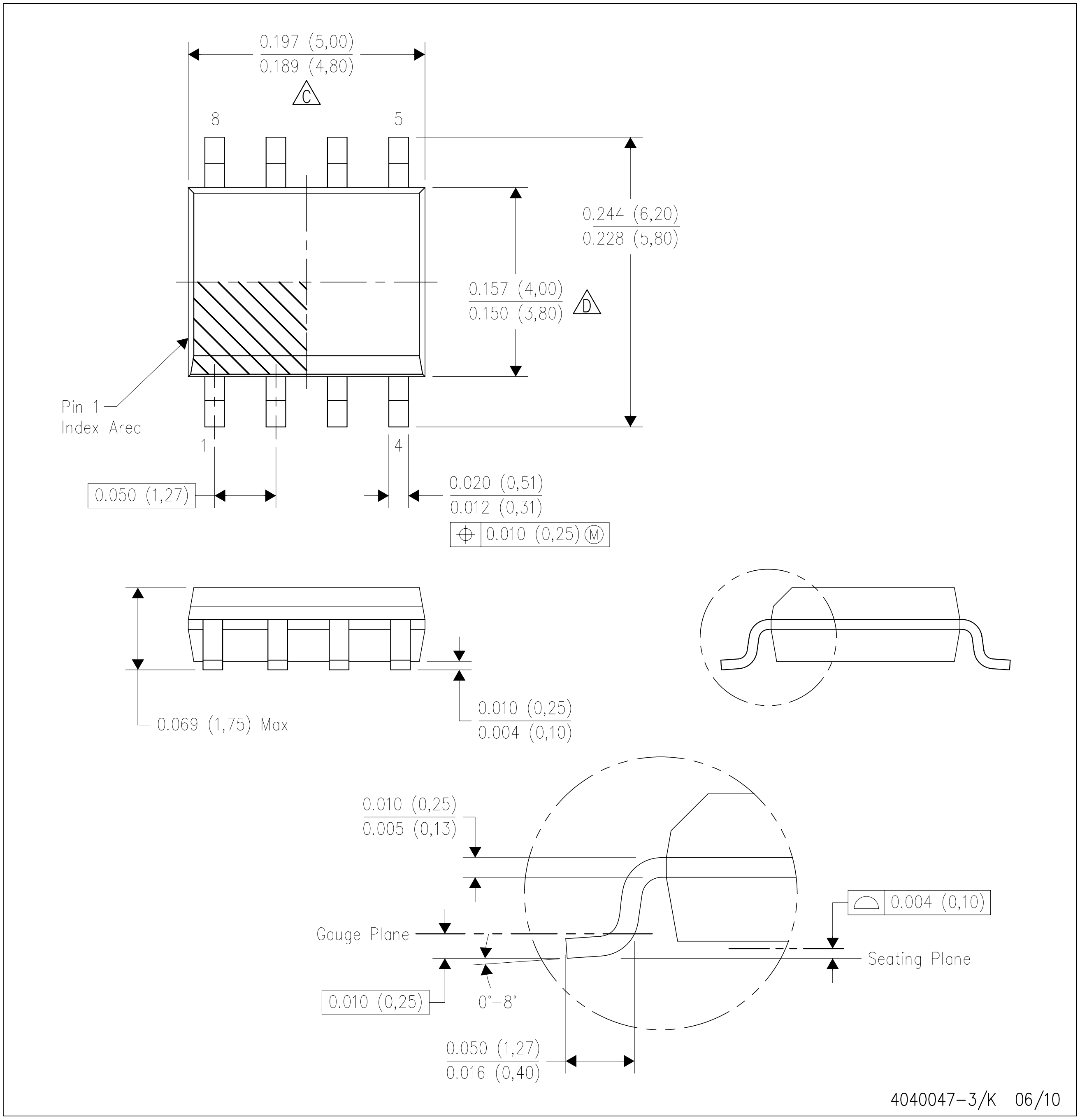
OTHER QUALIFIED VERSIONS OF TLE2027-EP :
- Catalog: TLE2027
- Military: TLE2027M

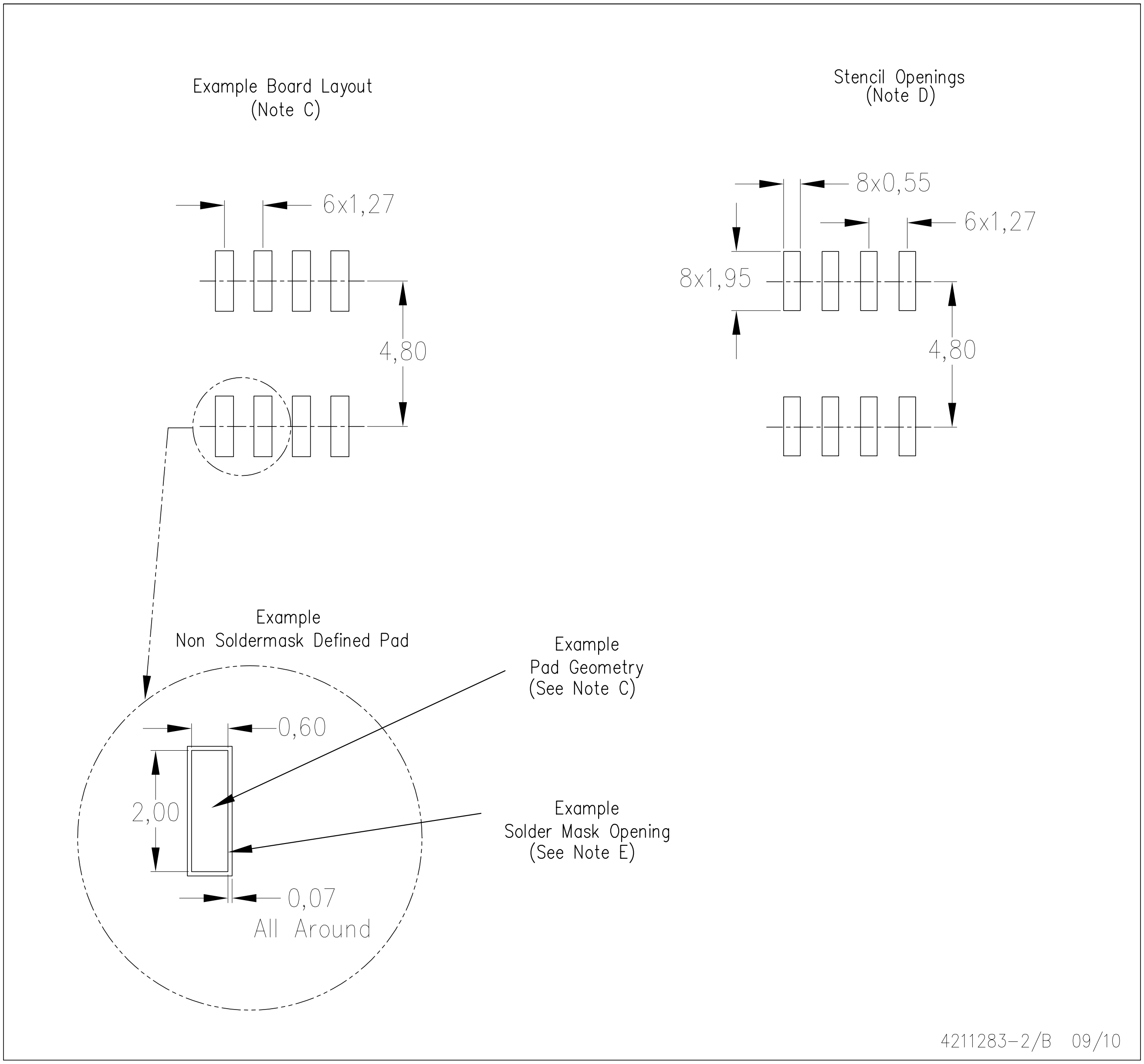
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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