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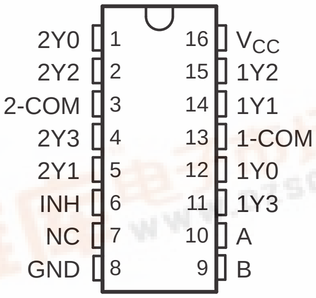
SN74HC4852-Q1
DUAL 4-TO-1 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

SCLS705A–DECEMBER 2006–REVISED FEBRUARY 2008

FEATURES

- **Qualified for Automotive Applications**
- **Injection-Current Cross Coupling <1 mV/mA (see Figure 1)**
- **Low Crosstalk Between Switches**
- **Pin Compatible With SN74HC4052, SN74LV4052A, and CD4052B**
- **2-V to 6-V V_{CC} Operation**

D OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

This dual 4-to-1 CMOS analog multiplexer/demultiplexer is pin compatible with the 4052 function and also features injection-current effect control. This feature has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

ORDERING INFORMATION(1)

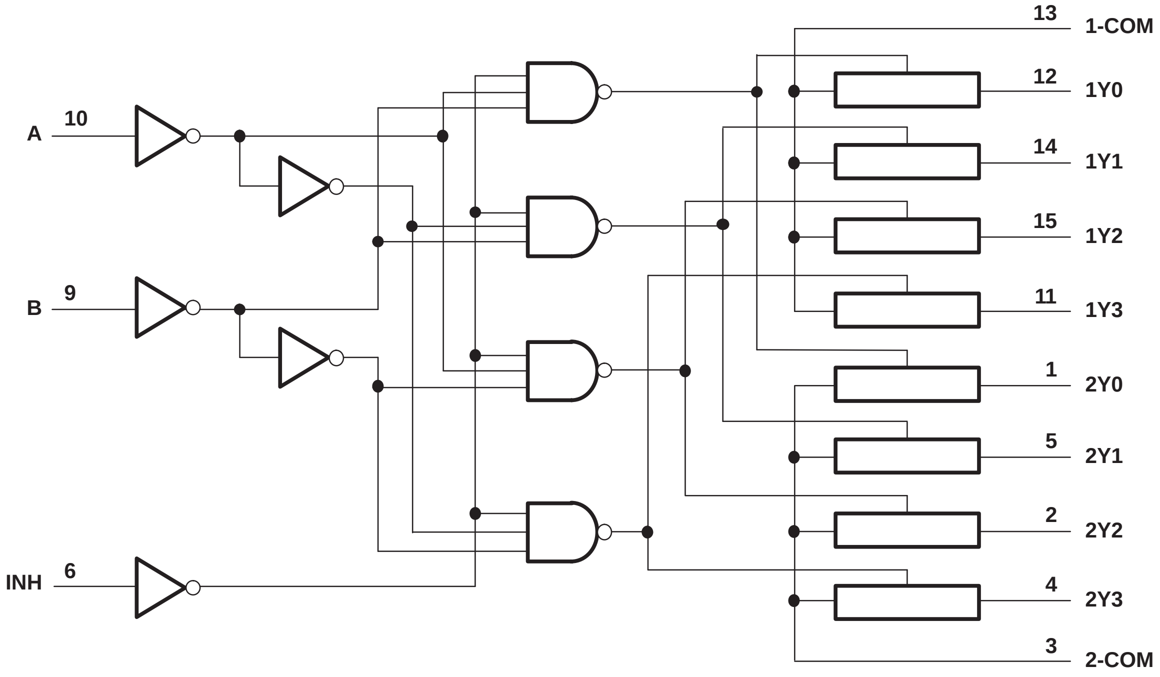
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN74HC4852QDRQ1	HC4852Q
	TSSOP – PW	Reel of 2000	SN74HC4852QPWRQ1	HC4852Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	V_{CC} + 0.5	V
V_{IO}	Switch I/O voltage range(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{IOK}	I/O diode current	$V_{IO} < 0$ or $V_{IO} > V_{CC}$		±20	mA
I_S	Switch through current	V_{IO} = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(4)	D package		73	°C/W
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)		2000	V
		Machine Model (MM)		200	
		Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.
(4) The package thermal impendance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 3.3 V	2.3		
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 3.3 V		1	
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Control input voltage		0	V_{CC}	V
V_{IO}	Input/output voltage		0	V_{CC}	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2 V		1000	ns
		V_{CC} = 3 V		800	
		V_{CC} = 3.3 V		700	
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	$I_S \le 2$ mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 5)	2 V		500	650		670		700	Ω
			3 V		215	280		320		360	
			3.3 V		210	270		305		345	
			4.5 V		160	210		240		270	
			6 V		150	195		220		250	
Δr_{on}	Difference in on-state resistance between switches	$I_S \le 2$ mA, $V_I = V_{CC}/2$, $V_{INH} = V_{IL}$	2 V		4	20		24		26	Ω
			3 V		2	14		16		18	
			3.3 V		2	14		16		18	
			4.5 V		2	10		14		18	
			6 V		3	11		15		20	
I_I	Control input current	$V_I = V_{CC}$ or GND	6 V			±0.1		±0.1		±1	µA
$I_{S(off)}$	Off-state switch leakage current (any one channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 6)	6 V			±0.1		±0.5		±1	µA
	Off-state switch leakage current (common channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 7)				±0.2		±2		±4	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 8)	6 V			±0.1		±0.5		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	6 V			2		5		10	µA
C_{IC}	Control input capacitance	A, B, INH			3.5	10		10		10	pF
C_{IS}	Common terminal capacitance	Switch off			22	40		40		40	pF
C_{OS}	Switch terminal capacitance	Switch off			6.7	15		15		15	pF

Injection-Current Coupling Specifications

T_A = –40°C to 125°C (see Figure 1)

PARAMETER		V_{CC}	TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
$V_{\Delta out}$	Maximum shift of output voltage of enabled analog channel	3.3 V	I_I[2] ≤ 1 mA	$R_S \le 3.9$ kΩ		0.05	1	mV
		5 V				0.1	1	
		3.3 V	I_I[2] ≤ 10 mA			0.345	5	
		5 V				0.067	5	
		3.3 V	I_I[2] ≤ 1 mA	$R_S \le 20$ kΩ		0.05	2	
		5 V				0.11	2	
		3.3 V	I_I[2] ≤ 10 mA			0.05	20	
		5 V				0.024	20	

(1) Typical values are measured at T_A = 25°C.
(2) I_I = total current injected into all disabled channels

Switching Characteristics

V_{CC} = 2 V, C_L = 50 pF, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 through Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	9.5	19.5	33	8	34	7	35	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn	14.6	24.5	38	14.4	40	12.8	42	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	15	23.6	47.5	13.8	52.5	12.5	57.5	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	34.5	48.4	100	34.3	105	34	115	ns

Switching Characteristics

V_{CC} = 3 V, C_L = 50 pF, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 through Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	3.6	12	17.5	4.5	19	3.2	20.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn	7.4	14.6	21	8.3	22.5	7.2	24	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	7.9	13.8	45	6.2	50	5.5	55	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	31.2	44.5	90	31.5	100	31	110	ns

Switching Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 through Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	3.9	11	15.5	4	17	3.2	18.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn	6.4	13.5	19	6.5	20.5	5.5	22.5	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	7	12.7	42.5	6.4	47.5	5.4	52.5	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	30	43.9	85	29.6	95	29.5	105	ns

Switching Characteristics

V_{CC} = 4.5 V, C_L = 50 pF, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 through Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	2.3	8.6	13	2.1	13.8	2	15.2	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn	5.3	11	16.6	5.5	18	4.6	19	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	4	9.9	40	4.3	45	3.4	50	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	24.5	41.4	80	24.2	90	24	100	ns

Switching Characteristics

V_{CC} = 6 V, C_L = 50 pF, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9 through Figure 14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	2	8	11.8	2.3	13	1.8	13.5	ns
t_{PLH} t_{PHL}	Propagation delay time	Channel Select	COM or Yn	3.4	9.5	14.6	3.7	16	2.8	17.5	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	2.8	8.4	39	3	40	2	40	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	12.4	38	78	11.5	80	11	80	ns

Operating Characteristics

T_A = 25°C (see Figure 15)

PARAMETER		V_{CC}	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	3.3 V	No load	48	pF
		5 V		60	

APPLICATION INFORMATION

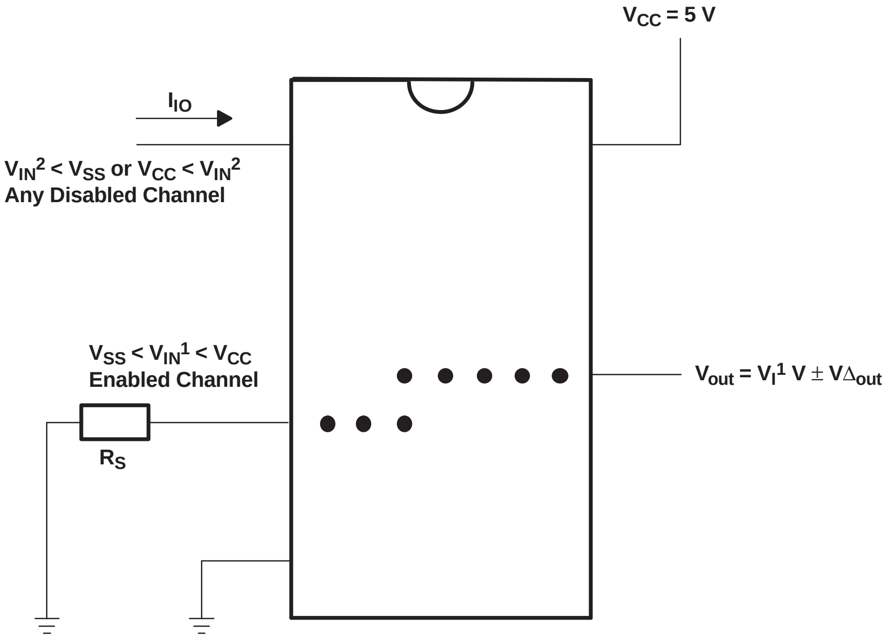


Figure 1. Injection-Current Coupling Specification

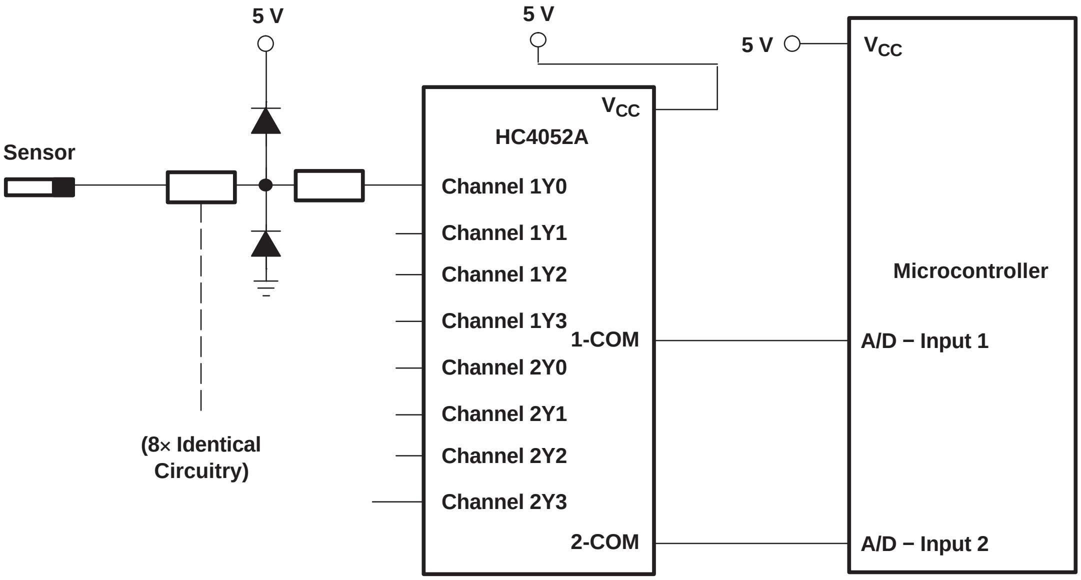


Figure 2. Actual Technology Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard HC4052 Multiplexer

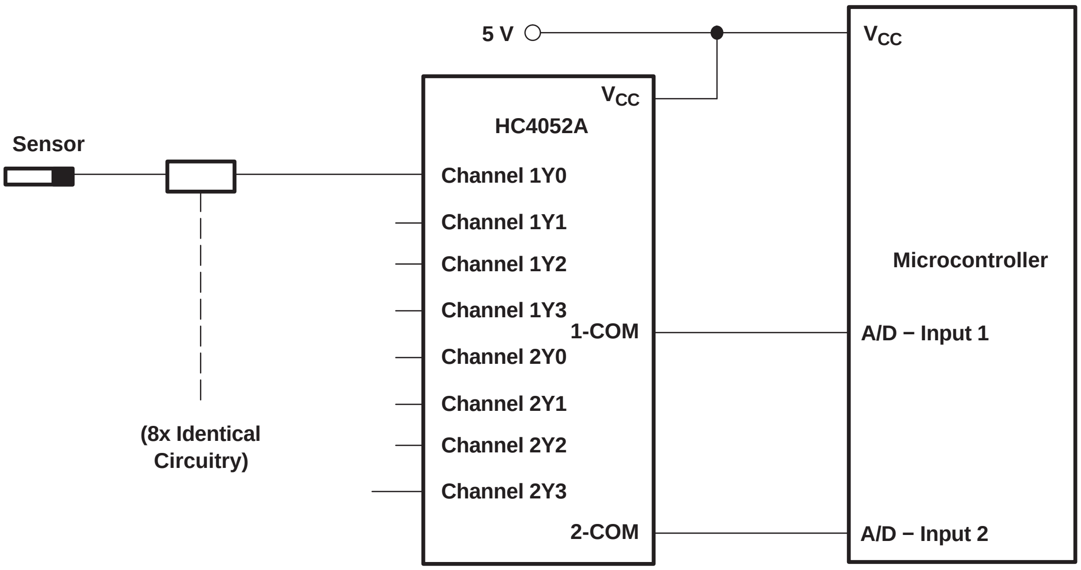


Figure 3. Solution by Applying the HC4852 Multiplexer

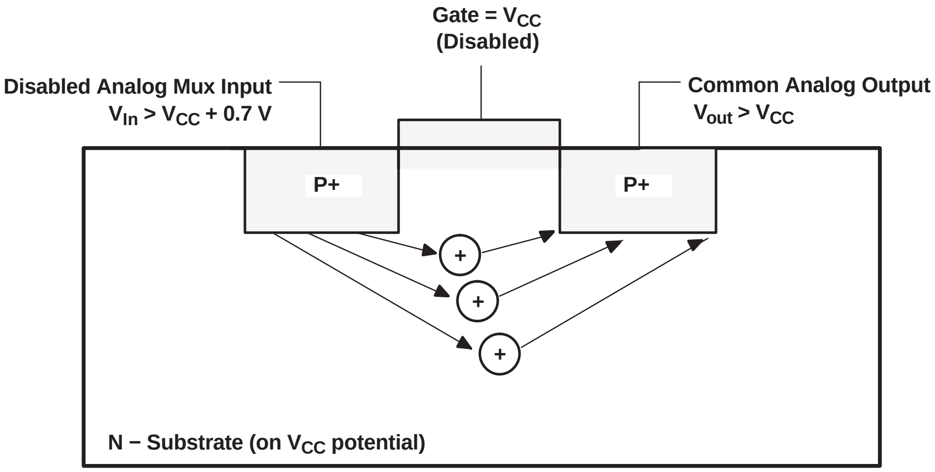


Figure 4. Diagram of Bipolar Coupling Mechanism
(Appears if V_{IN} Exceeds V_{CC}, Driving Injection Current Into the Substrate)

PARAMETER MEASUREMENT INFORMATION

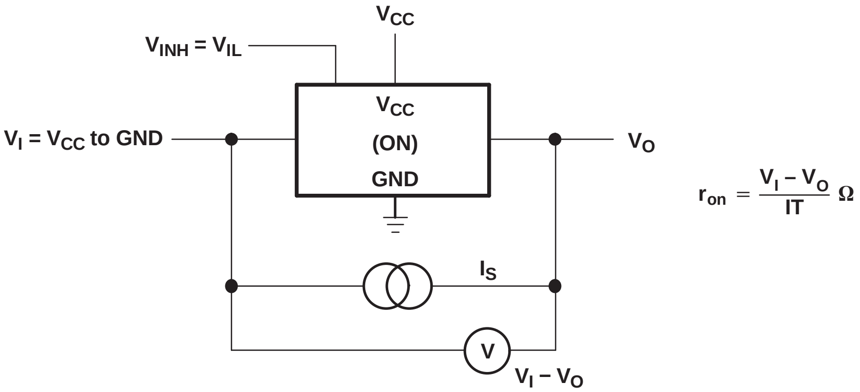


Figure 5. On-State Resistance Test Circuit

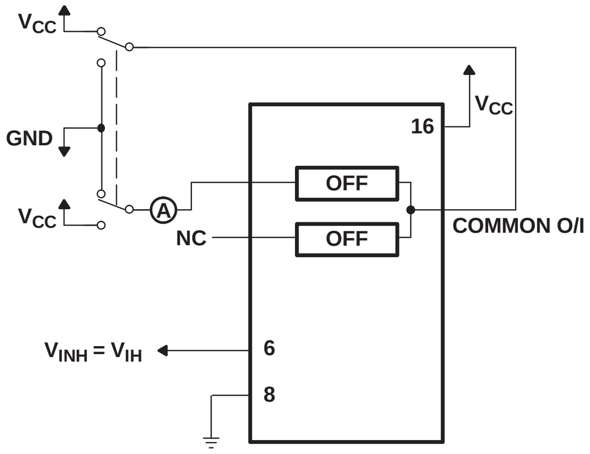


Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

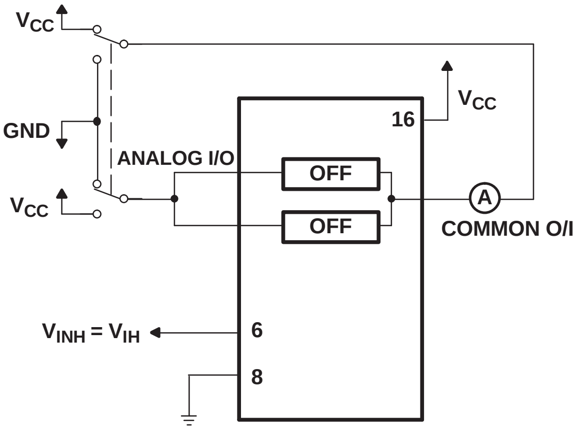


Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

PARAMETER MEASUREMENT INFORMATION (continued)

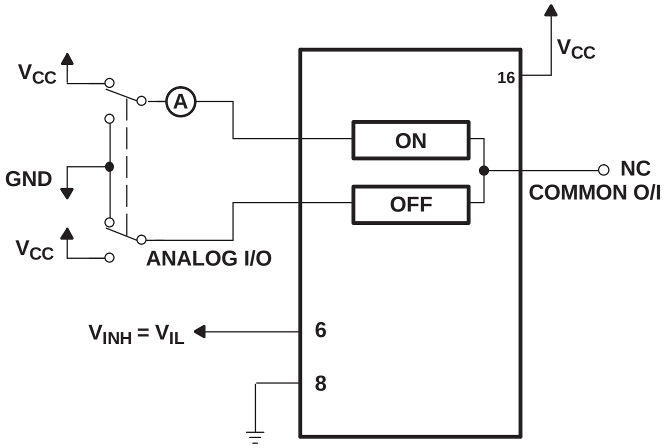


Figure 8. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup

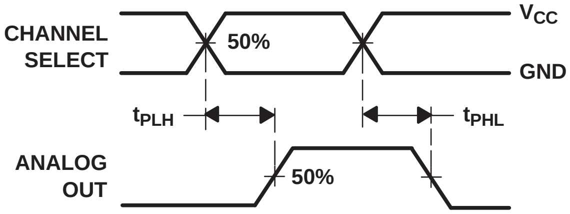
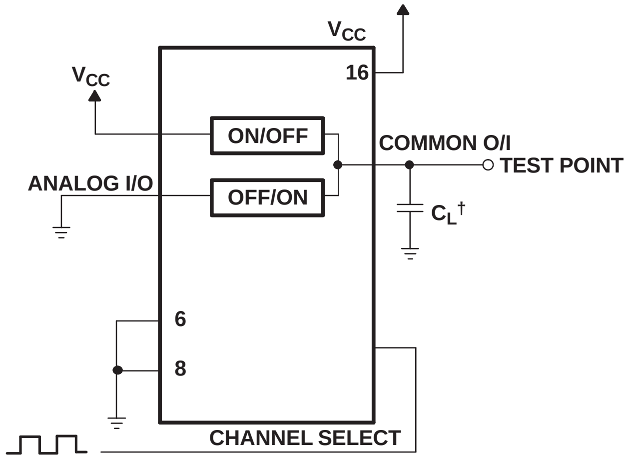


Figure 9. Propagation Delays, Channel Select to Analog Out



† Includes all probe and jig capacitance

Figure 10. Propagation Delay, Channel Select to Analog Out, Test Setup

PARAMETER MEASUREMENT INFORMATION (continued)

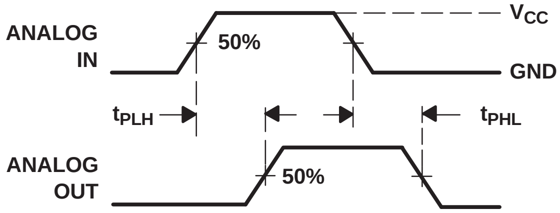
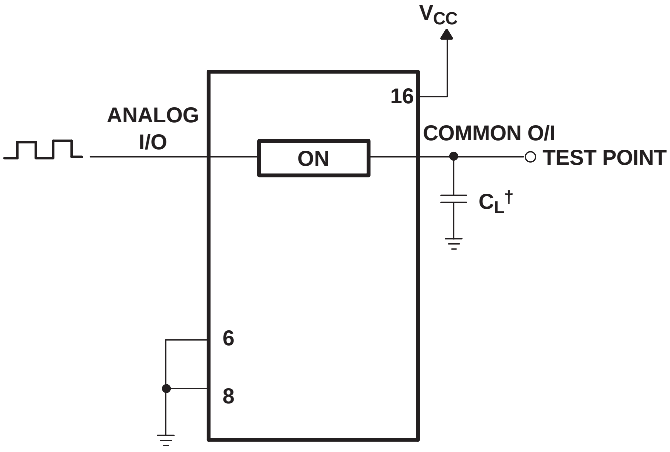


Figure 11. Propagation Delays, Analog In to Analog Out



† Includes all probe and jig capacitance

Figure 12. Propagation Delay, Analog In to Analog Out, Test Setup

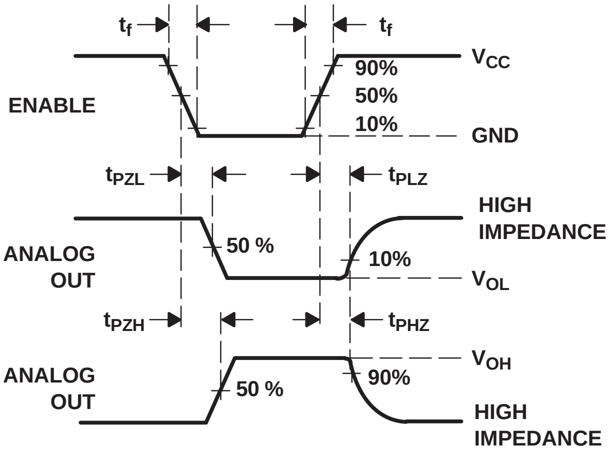


Figure 13. Propagation Delays, Enable to Analog Out

PARAMETER MEASUREMENT INFORMATION (continued)

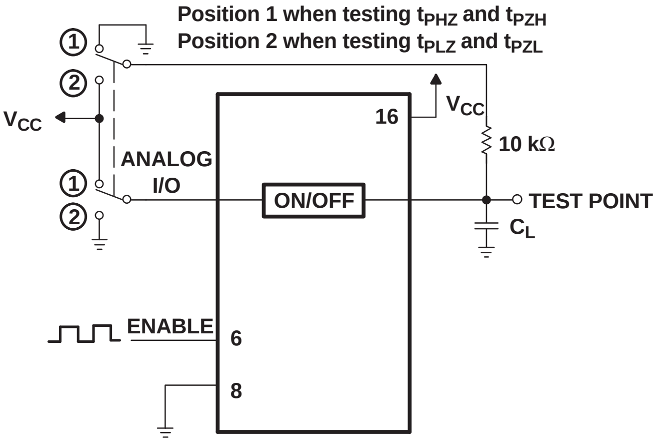


Figure 14. Propagation Delay, Enable to Analog Out, Test Setup

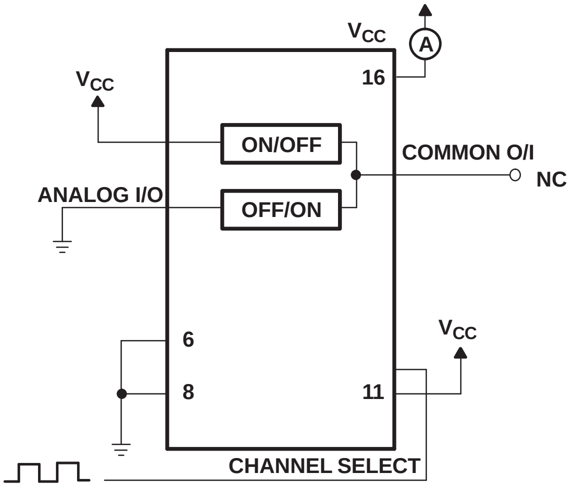


Figure 15. Power-Dissipation Capacitance, Test Setup

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74HC4852QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC4852QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

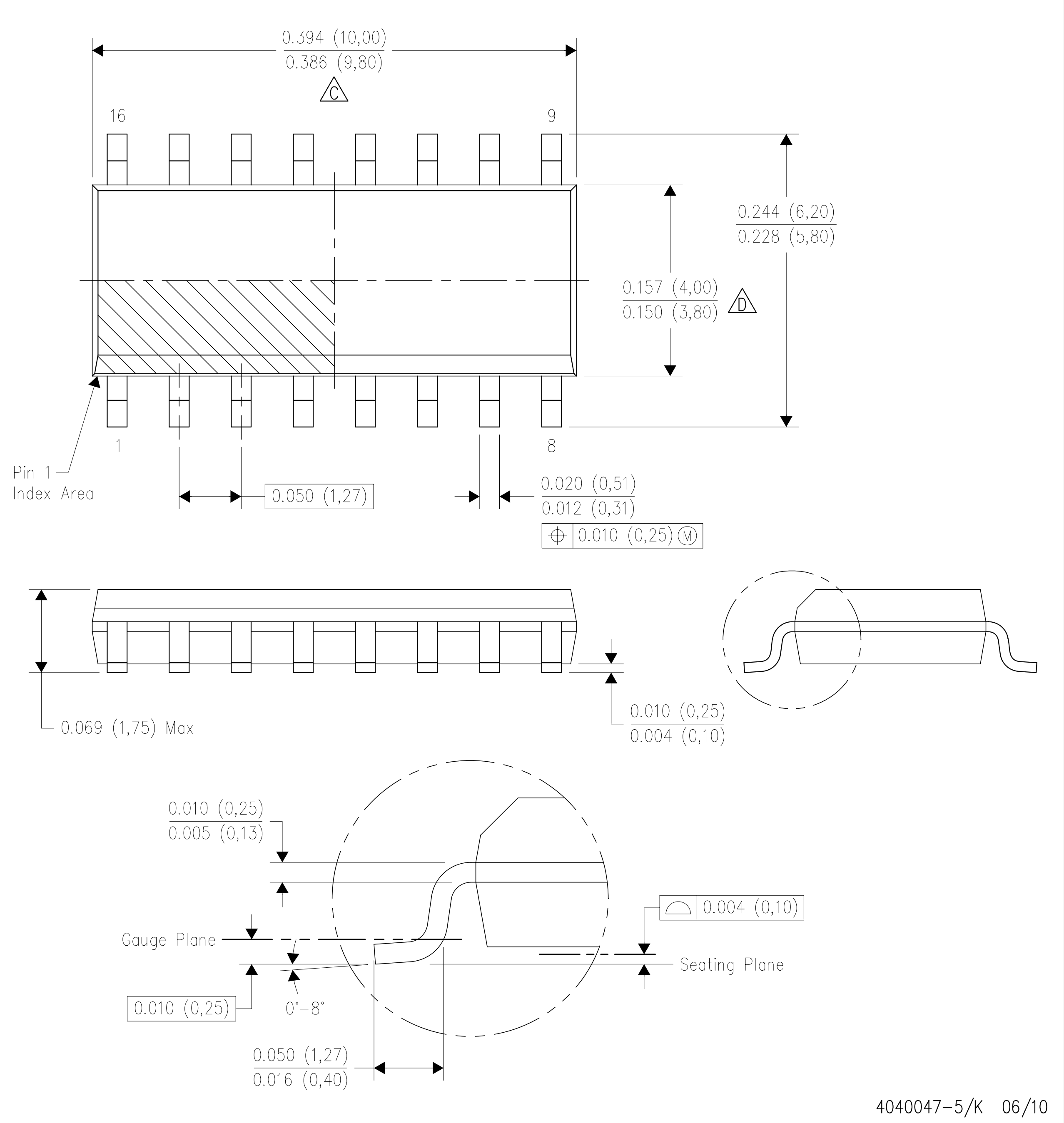
OTHER QUALIFIED VERSIONS OF SN74HC4852-Q1 :

- Catalog: SN74HC4852

NOTE: Qualified Version Definitions:

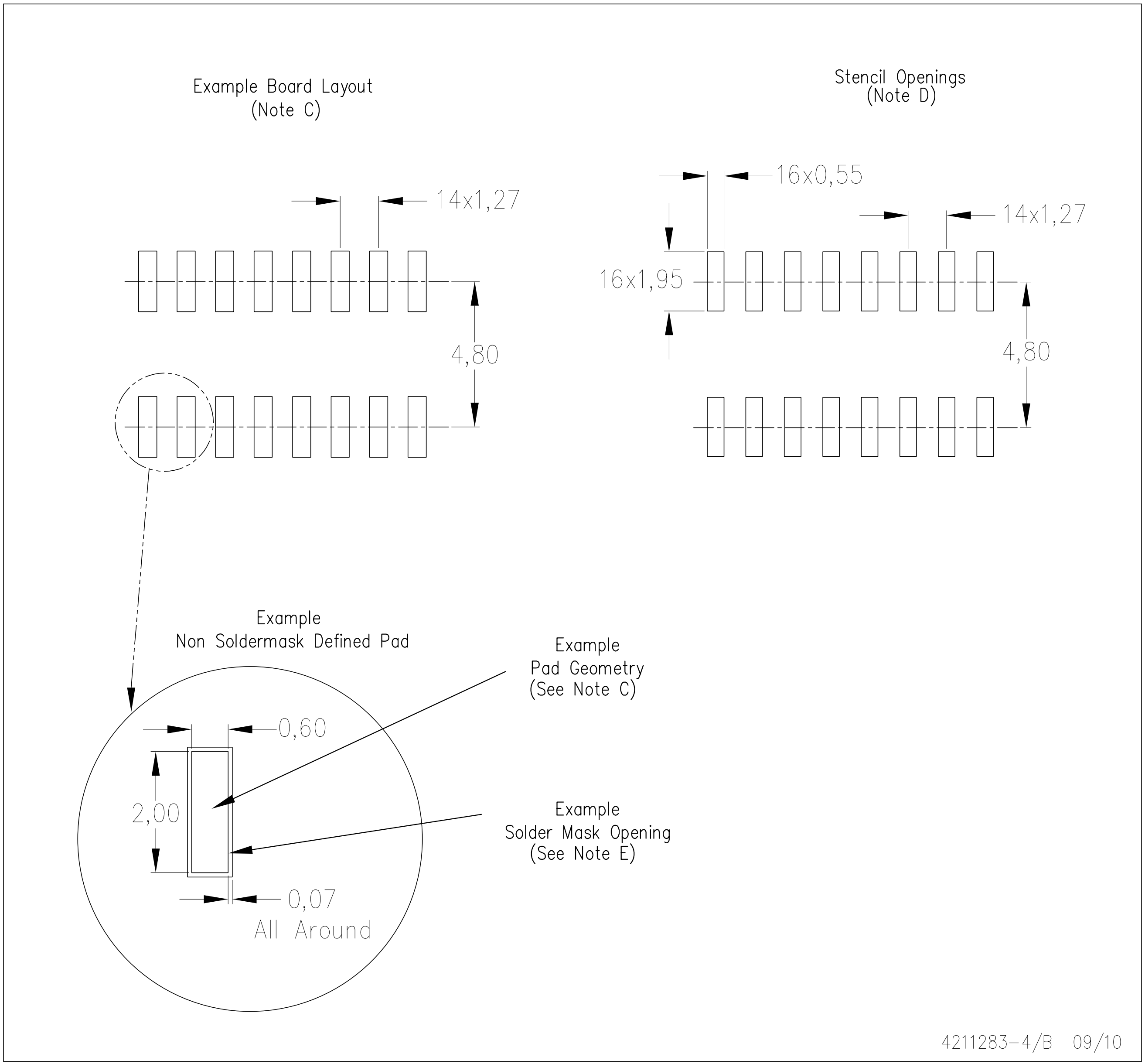
  - Catalog - TI's standard catalog product

D (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

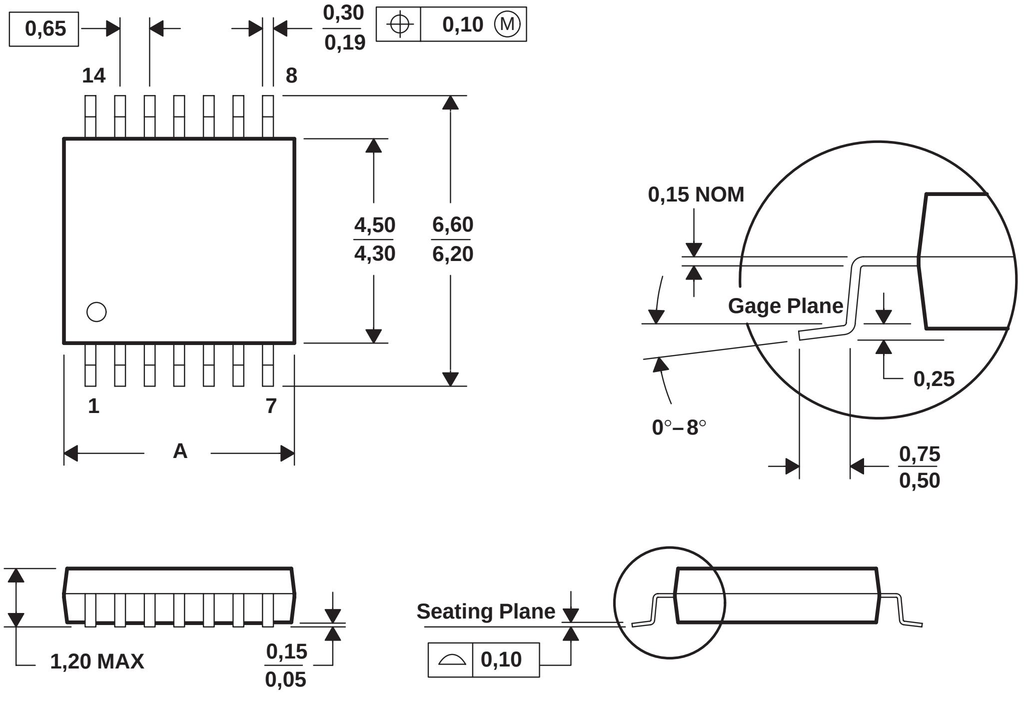
D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

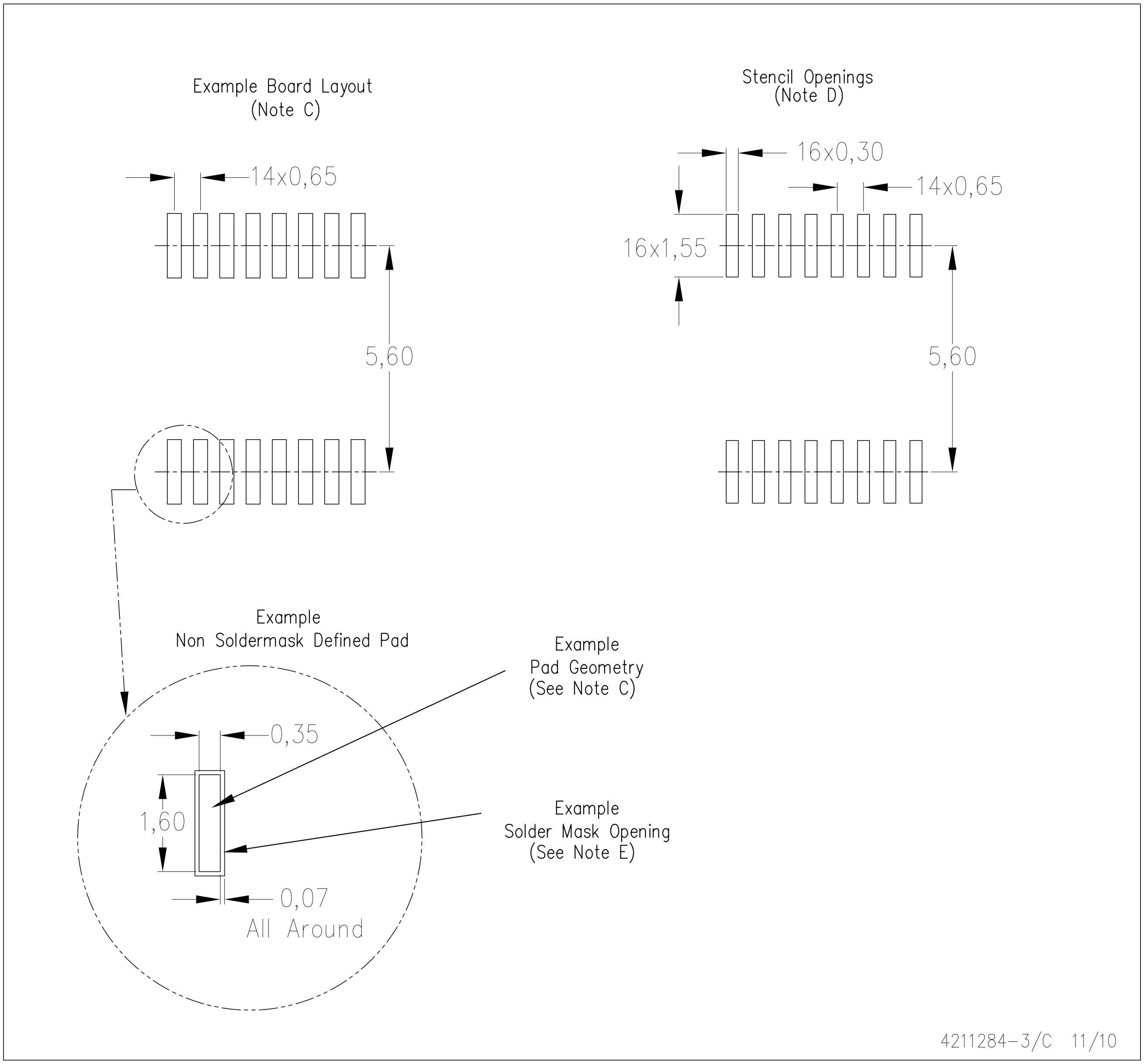


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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