REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48					
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thanh V. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thanh V. Nguyen APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 99-04-30 REVISION LEVEL	MICROCIRCUIT, DIGITAL, CMOS, DIGITAL SIGNAL PROCESSOR CONTROLLER, MONOLITHIC SILICON SIZE **A** / CAGE CODE **67268** / **5962-98612** SHEET 1 OF 48

DSCC FORM 2233
APR 97

5962-E268-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	98612	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320F240	Digital signal processor controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	132	Ceramic quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc 2/
Input voltage range (V_{IN})	-0.3 V dc to +7.0 V dc
Output voltage range (V_{OUT})	-0.3 V dc to +7.0 V dc
Storage temperature range (T_{STG})	-65 C to +150 C
Analog supply reference source (V_{REFHI}, V_{REFLO})	-0.3 V dc to +7.0 V dc
Analog input voltage range (V_{AI})	-0.3 V dc to +7.0 V dc
Resolution	10-bit (1024 values)
Monotonic	Assured
Output conversion mode	000h to 3FFh (000h for V_I V_{SSA}; 3FFh for V_I V_{CCA})
Thermal resistance, junction-to-ambient ($_{JA}$)	55.71 C/W
Thermal resistance, junction-to-case ($_{JC}$)	2.57 C/W

1.4 Recommended operating conditions.

Digital supply voltage range (DV_{DD})	+4.5 V to +5.5 V
Supply voltage return	0.0 V
High level input voltage range (V_{IH}):	
XTAL1/CLKIN	+3.0 V to V_{DD} + 0.3 V
$\overline{\text{PORESET}}$, NMI, $\overline{\text{RS}}$, and $\overline{\text{TRST}}$	+2.2 V to V_{DD} + 0.3 V
All other inputs	+2.0 V to V_{DD} + 0.3 V
Low level input voltage range (V_{IL}):	
XTAL1/CLKIN	-0.3 V to 0.7 V
All other inputs	-0.3 V to 0.8 V
High level output current (I_{OH}):	
$\overline{\text{RS}}$	-19 mA 3/
IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7, EMU0, EMU1/$\overline{\text{OFF}}$	-16 mA 3/
All other outputs	-23 mA 3/
Low level output current (I_{OL}):	
$\overline{\text{RS}}$	8 mA 3/
IOPA[0:3], SCIRXD/IO, SCITXD/IO, XINT2/IO, XINT3/IO, ADCSOC/IOPC0, TMRDIR/IOPB6, TMRCLK/IOPB7, EMU0, EMU1/$\overline{\text{OFF}}$	7.5 mA 3/
All other outputs	14.5 mA 3/
Case operating temperature range (T_C)	-55 C to +125 C
Flash programming operating temperature range (T_{FP})	-40 C to +85 C

Recommended operating conditions for 10-bit dual analog-to-digital converter (ADC):

Analog supply voltage range (V_{CCA})	4.5 V to +5.5 V
Analog ground (V_{SSA})	0 V
Analog supply reference source range (V_{REFHI})	V_{REFLO} to V_{CCA} 4/
Analog ground reference source range (V_{REFLO})	V_{SSA} to V_{REFHI} 4/
Analog input voltage range – ADCIN0-ADCIN15 (V_{AI})	V_{SSA} to V_{CCA}

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ V_{DD} refers to supply voltage types CV_{DD} (digital core supply voltage), DV_{DD} (digital I/O supply voltage), and V_{DDP} (programming voltage supply). All voltages are measured with respect to V_{SS}.
3/ Typical readings derived from Spice simulations. Not production tested.
4/ V_{REFHI} and V_{REFLO} must be stable, within 1/2 LSB of the required resolution, during the entire conversion time.

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 1/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Values will be added when they become available.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Test circuit and timing waveforms. The test circuit and timing waveforms are as specified on figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Theses devices shall be compliant to IEEE 1149.1.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
High-level output voltage	V_{OH}	I_{OH} = MAX		All	1, 2, 3	2.4		V
Low-level output voltage	V_{OL}	I_{OL} = MAX		All	1, 2, 3		0.6	V
Input current	I_I	$V_I = V_{SS}$ or V_{DD}	$\overline{TRST}$ with internal pulldown	All	1, 2, 3	-10	500	A
			EMU0, EMU1/$\overline{OFF}$, TMS, TCK, and TDI, with internal pullup			-500	10	
			All other input pins			-10	10	
Output current, high impedance state (off-state)	I_{OZ}	$V_O = V_{DD}$ or 0.0 V		All	1, 2, 3	-5	5	A
Supply current, operating mode	I_{DD1}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		100 1/	mA
Supply current, idle 1 low-power mode	I_{DD2}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		50 1/	mA
Supply current, idle 2 low-power mode	I_{DD3}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		7 1/	mA
Supply current, PLL power-down mode	I_{DD4}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		5 1/	mA
Supply current, OSC power-down mode	I_{DD5}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		400 1/	A
Flash programming supply current	I_{DDP}	$t_{c(CO)}$ = 50 ns		All	1, 2, 3		10 1/	mA
Input capacitance	C_I	See 4.4.1c		All	4		15	pF
Output capacitance	C_O	See 4.4.1c		All	4		15	pF
Functional testing		See 4.4.1b		All	7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Clock options – Input clock frequency with the PLL circuit disabled								
Input clock frequency, divide-by-2 mode	f_{x1}			All	9, 10, 11	0 2/	40	MHz
Input clock frequency, divide-by-1 mode	f_{x2}			All	9, 10, 11	0 2/	20	
Clock options – Switching characteristics, H = 0.5 $t_{c(CO)}$ 3/								
Cycle time, CPUCLK	$t_{c(CPU)}$	See figure 5	CLKIN divide by 2	All	9, 10, 11	$2t_{c(CI)}$ 1/	2/	ns
			CLKIN divide by 1			$t_{c(CI)}$ 1/		
Cycle time, SYSCLK	$t_{c(SYS)}$	See figure 5	CPUCLK divide by 2	All	9, 10, 11	$2t_{c(CPU)}$ 1/	2/	ns
			CPUCLK divide by 4 4/			$4t_{c(CPU)}$ 1/		
Cycle time, CLKOUT	$t_{c(CO)}$	See figure 5	CLKIN divide by 2	All	9, 10, 11	$2t_{c(CI)}$ 1/	2/	ns
			CLKIN divide by 1			$t_{c(CI)}$ 1/	2/	
Delay time, XTAL1/CLKIN high to CLKOUT high/low	$t_{d(CIH-CO)}$	See figure 5		All	9, 10, 11	3	22	ns
Fall time, CLKOUT	$t_{f(CO)}$			All	9, 10, 11		5 1/	ns
Rise time, CLKOUT	$t_{r(CO)}$			All	9, 10, 11		5 1/	ns
Pulse duration, CLKOUT low	$t_{w(COL)}$			All	9, 10, 11	H-10	H-1	ns
Pulse duration, CLKOUT high	$t_{w(COH)}$			All	9, 10, 11	H+0	H+8	ns
Clock options – Timing requirements								
Cycle time, XTAL1/CLKIN	$t_{c(CI)}$	See figure 5	Divide by 2	All	9, 10, 11	25	2/	ns
			Divide by 1			50	2/	
Fall time, XTAL1/CLKIN	$t_{f(CI)}$	See figure 5		All	9, 10, 11		5	ns
Rise time, XTAL1/CLKIN	$t_{r(CI)}$			All	9, 10, 11		5	ns
Pulse duration, XTAL1/CLKIN low as a percentage of $t_{c(CI)}$	$t_{w(CIL)}$			All	9, 10, 11	45	55	%
Pulse duration, XTAL1/CLKIN high as a percentage of $t_{c(CI)}$	$t_{w(CIH)}$			All	9, 10, 11	45	55	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Clock options – Input characteristics with the PLL circuit enabled								
Input clock frequency	f_x	External reference crystal = 4 MHz		All	9, 10, 11		4 1/	MHz
		External reference crystal = 6 MHz					6 1/	
		External reference crystal = 8 MHz					8 1/	
Load capacitance	C1, C2			All	4		10 1/	pF
Clock options – Switching characteristics, H = 0.5 $t_{c(CO)}$								
Cycle time, CPUCLK	$t_{c(CPU)}$	See figure 5	Before PLL lock, CLKIN divide by 2	All	9, 10, 11	$2t_{c(CI)}$ 1/	2/	ns
			Before PLL lock, CLKIN divide by 1			$t_{c(CI)}$ 1/		
			After PLL lock			50 1/		
Cycle time, SYSCLK	$t_{c(SYS)}$	See figure 5	CPUCLK divide by 2	All	9, 10, 11	$2t_{c(CPU)}$ 1/	2/	ns
			CPUCLK divide by 4 4/			$4t_{c(CPU)}$ 1/		
Cycle time, CLKOUT	$t_{c(CO)}$	See figure 5		All	9, 10, 11	50	2/	ns
Fall time, CLKOUT	$t_{f(CO)}$			All	9, 10, 11		5 1/	ns
Rise time, CLKOUT	$t_{r(CO)}$			All	9, 10, 11		5 1/	ns
Pulse duration, CLKOUT low	$t_{w(COL)}$			All	9, 10, 11	H-10	H-1	ns
Pulse duration, CLKOUT high	$t_{w(COH)}$			All	9, 10, 11	H+0	H+8	ns
Transition time, PLL synchronized after PLL enabled	t_p	See figure 5	Before PLL lock, CLKIN divide by 2	All	9, 10, 11		2000 $t_{c(CI)}$	ns
			Before PLL lock, CLKIN divide by 1				1000 $t_{c(CI)}$	
Clock options – Timing requirements 3/								
Cycle time, XTAL1/CLKIN	$t_{c(CI)}$	See figure 5	External reference crystal = 4 MHz	All	9, 10, 11	250	2/	ns
			External reference crystal = 6 MHz			167		
			External reference crystal = 8 MHz			125		
Fall time, XTAL1/CLKIN	$t_{f(CI)}$	See figure 5		All	9, 10, 11		5	ns
Rise time, XTAL1/CLKIN	$t_{r(CI)}$			All	9, 10, 11		5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Clock options – Timing requirements – Continued 3/								
Pulse duration, XTAL1/CLKIN low as a percentage of $t_{c(CI)}$	$t_{w(CIL)}$	See figure 5		All	9, 10, 11	40	60	%
Pulse duration, XTAL1/CLKIN high as a percentage of $t_{c(CI)}$	$t_{w(CIH)}$			All	9, 10, 11	40	60	%
Low-power mode timings – Switching characteristics, H = 0.5 $t_{c(CO)}$								
Delay time, CLKOUT switching to program execution resume 3/	$t_{d(WAKE-A)}$	See figure 5	Idle 1 and idle 2	All	9, 10, 11		$15xt_{c(CO)}$ 1/	ns
			PLL or OSC power down				$15xt_{c(CI)}$ 1/	
Delay time, idle instruction executed to CLKOUT high 3/	$t_{d(IDLE-COH)}$	See figure 5	Idle 2, PLL power down, OSC power down	All	9, 10, 11		500 1/	ns
Delay time, CLKOUT switching to PLL synchronized 3/	$t_{d(WAKE-LOCK)}$	See figure 5	PLL or OSC power down	All	9, 10, 11		100 1/	s
Delay time, wakeup interrupt asserted to oscillator running	$t_{d(WAKE-OSC)}$	See figure 5	OSC power down	All	9, 10, 11		10 1/	ms
Delay time, idle instruction executed to oscillator power off	$t_{d(IDLE-OSC)}$	See figure 5	OSC power down	All	9, 10, 11		60 1/	s
Memory and parallel I/O interface read timings – Switching characteristics for a memory read, H = 0.5 $t_{c(CO)}$ 5/								
Delay time, CLKOUT/IOPC1 low to address valid	$t_{d(CO-A)RD}$	See figure 5		All	9, 10, 11		17	ns
Delay time, CLKOUT/IOPC1 low to $\overline{STRB}$ low	$t_{d(CO-SL)RD}$			All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 low to $\overline{STRB}$ high	$t_{d(CO-SH)RD}$			All	9, 10, 11		6	ns
Delay time, CLKOUT/IOPC1 low to $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, and $\overline{BR}$ low	$t_{d(CO-ACTL)RD}$			All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 low to $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, and $\overline{BR}$ high	$t_{d(CO-ACTH)RD}$			All	9, 10, 11		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Memory and parallel I/O interface read timings – Timing requirements for a memory read, H = 0.5 $t_{c(CO)}$ 5/								
Access time, from address valid to read data	$t_{a(A)}$	See figure 5	0 wait state	All	9, 10, 11		2H-32	ns
			1 wait state				4H-32	
Setup time, data read before CLKOUT/IOPC1 low	$t_{su(D-COL)RD}$	See figure 5		All	9, 10, 11	13		ns
Hold time, data read after CLKOUT/IOPC1 low	$t_{h(COL-D)RD}$			All	9, 10, 11	2		ns
Memory and parallel I/O interface write timings – Switching characteristic for a memory write, H = 0.5 $t_{c(CO)}$ 5/								
Delay time, CLKOUT/IOPC1 high to address valid	$t_{d(CO-A)W}$	See figure 5		All	9, 10, 11		17	ns
Delay time, CLKOUT/IOPC1 low to data bus driven	$t_{d(CO-D)}$			All	9, 10, 11		15	ns
Delay time, address valid after $\overline{WE}$ high	$t_{d(D-WH)}$			All	9, 10, 11	H-8		ns
Pulse duration, $\overline{WE}$ high	$t_{w(WH)}$			All	9, 10, 11	2H-11		ns
Pulse duration, $\overline{WE}$ low	$t_{w(WL)}$			All	9, 10, 11	2H-11		ns
Delay time, CLKOUT/IOPC1 low to $\overline{WE}$ low	$t_{d(CO-WL)}$			All	9, 10, 11		9	ns
Delay time, CLKOUT/IOPC1 low to $\overline{WE}$ high	$t_{d(CO-WH)}$			All	9, 10, 11		9	ns
Delay time, write data valid before $\overline{WE}$ high	$t_{d(WH-D)}$			All	9, 10, 11	2H-8		ns
Delay time, $\overline{WE}$ high to data bus high-Z	$t_{d(D-WHZ)}$			All	9, 10, 11	0	5	ns
Delay time, CLKOUT/IOPC1 low to $\overline{STRB}$ low	$t_{d(CO-SL)W}$			All	9, 10, 11		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Memory and parallel I/O interface write timings – Switching characteristic for a memory write, H = 0.5 $t_{c(CO)}$ – Continued 5/							
Delay time, CLKOUT/IOPC1 low to $\overline{STRB}$ high	$t_{d(CO-SH)W}$	See figure 5	All	9, 10, 11		6	ns
Delay time, CLKOUT/IOPC1 high to $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, and $\overline{BR}$ low	$t_{d(CO-ACTL)W}$		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, and $\overline{BR}$ high	$t_{d(CO-ACTH)W}$		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to R/$\overline{W}$ low	$t_{d(CO-RWL)}$		All	9, 10, 11		10	ns
Delay time, CLKOUT/IOPC1 high to R/$\overline{W}$ high	$t_{d(CO-RWH)}$		All	9, 10, 11		10	ns
READY timings – Timing requirements 6/							
Setup time, READY low before CLKOUT/IOPC1 high	$t_{su(R-CO)}$	See figure 5	All	9, 10, 11	14		ns
Hold time, READY low after CLKOUT/IOPC1 high	$t_{h(CO-R)}$		All	9, 10, 11	0		ns
Valid time, READY after address valid on read	$t_{v(R)ARD}$		All	9, 10, 11		3H-31	ns
Valid time, READY after address valid on write	$t_{v(R)AW}$		All	9, 10, 11		4H-31	ns
$\overline{RS}$ and $\overline{PORESET}$ timings – Switching characteristics for a reset, H = 0.5 $t_{c(CO)}$							
Pulse duration, $\overline{RS}$ low 7/	$t_{w(RSL1)}$	See figure 5	All	9, 10, 11	8$t_{c(SYS)}$		ns
Delay time, $\overline{RS}$ low to program address at reset vector	$t_{d(RS)}$		All	9, 10, 11	4H		ns
Delay time, $\overline{RS}$ high to reset vector executed	$t_{d(EX)}$		All	9, 10, 11	32H		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{RS}$ and $\overline{PORESET}$ timings – Timing requirements for a reset, H = 0.5 $t_{c(CO)}$							
Pulse duration, $\overline{RS}$ or $\overline{PORESET}$ low 8/	$t_{w(RSL)}$	See figure 5	All	9, 10, 11	5		ns
XF, $\overline{BIO}$, and MP/$\overline{MC}$ timings – Switching characteristic, H = 0.5 $t_{c(CO)}$							
Delay time, CLKOUT high to XF high/low	$t_{d(XF)}$	See figure 5	All	9, 10, 11		11	ns
XF, $\overline{BIO}$, and MP/$\overline{MC}$ timings – Timing requirements, H = 0.5 $t_{c(CO)}$							
Pulse duration, $\overline{BIO}$ low	$t_{w(BIOL)}$	See figure 5	All	9, 10, 11	2H+16		ns
Pulse duration, MP/$\overline{MC}$ valid 9/	$t_{w(MPMCV)}$		All	9, 10, 11	2H+24		ns
PWM/CMP timings – Switching characteristic for PWM timing, H = 0.5 $t_{c(CO)}$							
Delay time, CLKOUT high to PWM output switching	$t_{d(PWM)CO}$	See figure 5	All	9, 10, 11		12	ns
PWM/CMP timings – Timing requirements							
Pulse duration, TMRDIR low/high	$t_{w(TMRDIR)}$	See figure 5	All	9, 10, 11	4H+12		ns
Pulse duration, TMRCLK low as a percentage of TMRCLK cycle time	$t_{w(TMRCLKL)}$		All	9, 10, 11	40	60	%
Pulse duration, TMRCLK high as a percentage of TMRCLK cycle time	$t_{w(TMRCLKH)}$		All	9, 10, 11	40	60	%
Cycle time, TMRCLK	$t_{c(TMRCLK)}$		All	9, 10, 11	$4xt_{c(CPU)}$		ns
Capture and QEP timings – Timing requirements							
Pulse duration, CAP input low/high	$t_{w(CAP)}$	See figure 5	All	9, 10, 11	4H+12		ns
Interrupt timings – Switching characteristics for interrupt, H = 0.5 $t_{c(CO)}$							
Delay time, $\overline{PDPINT}$ low to PWM to high-impedance state	$t_{d(PWM)PDP}$	See figure 5	All	9, 10, 11	0	15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Interrupt timings – Timing requirements								
Pulse duration, INT input low/high	$t_{w(INT)}$	See figure 5		All	9, 10, 11	$t_{c(SYS)}$+12		ns
Pulse duration, $\overline{PDPINT}$ input low	$t_{w(PDP)}$			All	9, 10, 11	2H+18		ns
Delay time, INT low/high to interrupt-vector fetch	$t_{d(INT)}$			All	9, 10, 11	$2t_{c(SYS)}$+ $4t_{c(CPU)}$		ns
General-purpose input/output timings – Switching characteristics for a GPI/O, H = 0.5 $t_{c(CO)}$								
Delay time, CLKOUT low to GPO low/high	$t_{d(GPO)CO}$	See figure 5	XINT2/IO, XINT3/IO, IOPB6, IOPB7, and IOPC0	All	9, 10, 11		33	ns
			All other GPOs				25	
General-purpose input/output timings - Timing requirements								
Pulse duration, GPI high/low	$t_{w(GPI)}$	See figure 5		All	9, 10, 11	$t_{c(SYS)}$+12		ns
Serial communications interface (SCI) I/O timings – Timing characteristics for SCI 10/								
Cycle time, SCICLK	$t_{c(SCC)}$	See figure 5	(BRR+1) is even and BRR = 0	All	9, 10, 11	$16t_c$	$65536t_c$	ns
			(BRR+1) is odd and BRR 0			$24t_c$	$65535t_c$	
Valid time, SCITXD data	$t_{v(TXD)}$	See figure 5	(BRR+1) is even and BRR = 0	All	9, 10, 11	$t_{c(SCC)}$–70	$t_{c(SCC)}$+70	ns
			(BRR+1) is odd and BRR 0			$t_{c(SCC)}$–70	$t_{c(SCC)}$+70	
Valid time, SCIRXD data	$t_{v(RXD)}$	See figure 5	(BRR+1) is even and BRR = 0	All	9, 10, 11	$16t_c$		ns
			(BRR+1) is odd and BRR 0			$24t_c$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
SPI master mode external timing parameters (clock phase = 0) 11/								
Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$4t_c$ 10/	$128t_c$ 10/	ns
			(SPIBRR+1) is odd or SPIBRR 3			$5t_c$ 10/	$127t_c$ 10/	
Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70	$0.5t_{c(SPC)M}$ $-0.5t_c$	
Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70	$0.5t_{c(SPC)M}$ $-0.5t_c$	
Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $+0.5t_c$-70	$0.5t_{c(SPC)M}$ $+0.5t_c$	
Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $+0.5t_c$-70	$0.5t_{c(SPC)M}$ $+0.5t_c$	
Delay time, SPICLK high (clock polarity = 0) to SPISIMO valid	$t_{d(SPCH-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	-10	10	ns
			(SPIBRR+1) is odd or SPIBRR 3			-10	10	
Delay time, SPICLK low (clock polarity = 1) to SPISIMO valid	$t_{d(SPCL-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	-10	10	ns
			(SPIBRR+1) is odd or SPIBRR 3			-10	10	
Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $+0.5t_c$-70		
Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $+0.5t_c$-70		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
SPI master mode external timing parameters (clock phase = 0) – Continued 11/								
Setup time, SPISOMI before SPICLK low (clock polarity = 0)	$t_{su(SOMI-SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR 3			0		
Setup time, SPISOMI before SPICLK high (clock polarity = 1)	$t_{su(SOMI-SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR 3			0		
Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{h(SPCL-SOMI)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.25t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70		
Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{h(SPCH-SOMI)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.25t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70		
SPI master mode external timing parameters (clock phase = 1) 13/								
Cycle time, SPICLK	$t_{c(SPC)M}$	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$4t_c$ 10/	$128t_c$ 10/	ns
			(SPIBRR+1) is odd or SPIBRR 3			$5t_c$ 10/	$127t_c$ 10/	
Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70	$0.5t_{c(SPC)M}$ $-0.5t_c$	
Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $-0.5t_c$-70	$0.5t_{c(SPC)M}$ $-0.5t_c$	
Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ $+0.5t_c$-70	$0.5t_{c(SPC)M}$ $+0.5t_c$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
SPI master mode external timing parameters (clock phase = 1) – Continued 13/								
Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70	$0.5t_{c(SPC)M}$	ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ +0.5t_c-70	$0.5t_{c(SPC)M}$ +0.5t_c	
Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		
Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		
Hold time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{h(SPCH-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		
Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_{h(SPCL-SIMO)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.5t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		
Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR 3			0		
Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	0		ns
			(SPIBRR+1) is odd or SPIBRR 3			0		
Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{h(SPCH-SOMI)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.25t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		
Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{h(SPCL-SOMI)M}$ 12/	See figure 5	(SPIBRR+1) is even or SPIBRR = 0 or 2	All	9, 10, 11	$0.25t_{c(SPC)M}$ -70		ns
			(SPIBRR+1) is odd or SPIBRR 3			$0.5t_{c(SPC)M}$ -70		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
SPI slave mode external timing requirements (clock phase = 0) 14/							
Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 5	All	9, 10, 11	$8t_c$ 10/		ns
Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Delay time, SPICLK high (clock polarity = 0) to SPISOMI valid	$t_{d(SPCH-SOMI)S}$ 12/		All	9, 10, 11	$0.375t_{c(SPC)S}$ -70		ns
Delay time, SPICLK low (clock polarity = 1) to SPISOMI valid	$t_{d(SPCL-SOMI)S}$ 12/		All	9, 10, 11	$0.375t_{c(SPC)S}$ -70		ns
Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SOMI)S}$ 12/		All	9, 10, 11	$0.75t_{c(SPC)S}$		ns
Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SOMI)S}$ 12/		All	9, 10, 11	$0.75t_{c(SPC)S}$		ns
Setup time, SPISIMO before SPICLK low (clock polarity = 0)	$t_{su(SIMO-SPCL)S}$ 12/		All	9, 10, 11	0		ns
Setup time, SPISIMO before SPICLK high (clock polarity = 1)	$t_{su(SIMO-SPCH)S}$ 12/		All	9, 10, 11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
SPI slave mode external timing requirements (clock phase = 0) – Continued 14/							
Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$t_{v(SPCL-SIMO)S}$ 12/	See figure 5	All	9, 10, 11	$0.5t_{c(SPC)S}$		ns
Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$t_{v(SPCH-SIMO)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$		ns
SPI slave mode external timing requirements (clock phase = 1) 15/							
Cycle time, SPICLK	$t_{c(SPC)S}$	See figure 5	All	9, 10, 11	$8t_c$ 10/		ns
Pulse duration, SPICLK high (clock polarity = 0)	$t_{w(SPCH)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK low (clock polarity = 1)	$t_{w(SPCL)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK low (clock polarity = 0)	$t_{w(SPCL)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Pulse duration, SPICLK high (clock polarity = 1)	$t_{w(SPCH)S}$ 12/		All	9, 10, 11	$0.5t_{c(SPC)S}$ -70	$0.5t_{c(SPC)S}$	ns
Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$t_{su(SOMI-SPCH)S}$ 12/		All	9, 10, 11	$0.125t_{c(SPC)S}$		ns
Setup time, SPISOMI before SPICLK low (clock polarity = 1)	$t_{su(SOMI-SPCL)S}$ 12/		All	9, 10, 11	$0.125t_{c(SPC)S}$		ns
Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SOMI)S}$ 12/		All	9, 10, 11	$0.75t_{c(SPC)S}$		ns
Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SOMI)S}$ 12/		All	9, 10, 11	$0.75t_{c(SPC)S}$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
SPI slave mode external timing requirements (clock phase = 1) – Continued 15/								
Setup time, SPISIMO before SPICLK high (clock polarity = 0)	$t_{su(SIMO-SPCH)S}$ 12/	See figure 5		All	9, 10, 11	0		ns
Setup time, SPISIMO before SPICLK low (clock polarity = 1)	$t_{su(SIMO-SPCL)S}$ 12/			All	9, 10, 11	0		ns
Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$t_{v(SPCH-SIMO)S}$ 12/			All	9, 10, 11	$0.5t_{c(SPC)S}$		ns
Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$t_{v(SPCL-SIMO)S}$ 12/			All	9, 10, 11	$0.5t_{c(SPC)S}$		ns
10-bit dual analog-to-digital converter (ADC) – Electrical characteristics 16/								
Analog supply current	I_{CCA}	V_{CCA} = 5.5 V	Converting	All	1, 2, 3		5	mA
			Non-converting				2	
		$V_{CCA} = V_{REFHI}$ = 5.5 V	PLL or OSC power down				1	
Input charge current, V_{REFHI} or V_{REFLO}	I_{ref}	$V_{CCA} = V_{CCD} = V_{REFHI}$ = 5.5 V V_{REFLO} = 0 V		All	1, 2, 3		5	mA
Analog input capacitance	C_{ai}	Typical capacitive load on analog input pin	Non-sampling	All	4		6	pF
			Sampling				8	
Analog input source impedance	Z_{AI}	Analog input source impedance for conversions to remain within specifications		All	1, 2, 3		9	k
Differential non-linearity error	E_{DNL}	Difference between the actual step width and the ideal value		All	1, 2, 3	-1	1.5	LSB
Integral non-linearity error	E_{INL}	Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error		All	1, 2, 3		1.5	LSB
Delay time, power-up to ADC valid	$t_{d(PU)}$	Time to stabilize analog stage after power-up		All	9, 10, 11		10	s

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
10-bit dual analog-to-digital converter (ADC) – Timing requirements							
Cycle time, ADC prescaled clock	$t_{c(AD)}$	See figure 5	All	9, 10, 11	1		s
Pulse duration, total sample/hold and conversion time 17/	$t_{w(SHC)}$		All	9, 10, 11	6.1		s
Pulse duration, sample/hold time	$t_{w(SH)}$		All	9, 10, 11	$t_{c(AD)}$		s
Setup time, analog input stable before sample/hold start	$t_{su(SH)}$		All	9, 10, 11	0		ns
Hold time, analog input stable after sample/hold complete	$t_{h(SH)}$		All	9, 10, 11	0		ns
Pulse duration, total conversion time	$t_{w(C)}$		All	9, 10, 11	$4.5t_{c(AD)}$		s
Delay time, start of conversion to begin of sample and hold 18/	$t_{d(SOC-SH)}$		All	9, 10, 11	$3t_{c(SYS)}$		ns
Delay time, end of conversion to data loaded into result FIFO	$t_{d(EOC-FIFO)}$		All	9, 10, 11	$3t_{c(SYS)}$		ns
Flash EEPROM – Switching characteristics							
Program-erase endurance			All	9, 10, 11	10K		Cycles
Program pulse per word 19/			All	9, 10, 11	1	150	Pulses
Erase pulses per array 19/			All	9, 10, 11	1	1000	Pulses
Flash-write pulses per array 19/			All	9, 10, 11	1	6000	Pulses

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions -55 C T_C +125 C +4.5 V V_{DD} +5.5 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Flash EEPROM – Timing requirements							
Delay time, after mode deselect to stabilization 19/	$t_{d(BUSY)}$		All	9, 10, 11	10		s
Delay time, verify read mode select to stabilization 19/	$t_{d(RD-VERIFY)}$		All	9, 10, 11	10		s
Flash EEPROM – Programming operation (maximum programming temperature 85 C for flash memory)							
Pulse duration, programming algorithm 19/	$t_{w(PGM)}$		All	9, 10, 11	95	105	s
Delay time, program mode select to stabilization 19/	$t_{d(PGM-MODE)}$		All	9, 10, 11	10		s
Flash EEPROM – Erase operation							
Pulse duration, erase algorithm 19/	$t_{w(ERASE)}$		All	9, 10, 11	6.65	7.35	ms
Delay time, erase mode select to stabilization 19/	$t_{d(ERASE-MODE)}$		All	9, 10, 11	10		s
Flash EEPROM – Flash-write operation							
Pulse duration, flash-write algorithm 19/ 20/	$t_{w(FLW)}$		All	9, 10, 11	13.3	14.7	ms
Delay time, flash-write mode select to stabilization 19/ 20/	$t_{d(FLW-MODE)}$		All	9, 10, 11	10		s
JTAG timings							
TMS/TDI setup to TCK high	t_{su}	See figure 5	All	9, 10, 11	20		ns
TMS/TDI hold from TCK high	t_h		All	9, 10, 11	15		ns
TCK low to TDO valid	t_d		All	9, 10, 11		30	ns

1/ Not production tested.

2/ This device utilizes a fuly static design and, therefore, can operate with input clock cycle time [$t_{c(CI)}$] approaching infinity. The device is characterized at frequencies approaching 0 Hz.

3/ Timing assume CLKOUT is set to output CPUCLK. CLKOUT is initialized to CPUCLK by power-on reset.

TABLE I. Electrical performance characteristics - Continued.

4/ SYSCLK is initialized to divide-by-4 mode by any device reset.

5/ All timings with respect to CLKOUT/IOPC1 assume CLKSRC[1:0] bits are set to select CPUCLK for output.

6/ The READY timings are based on one software wait state. At full speed operation, the device does not allow for single READY-based wait states.

7/ The parameter $t_{w(RSL1)}$ refers to the time $\overline{RS}$ is an output.

8/ The parameter $t_{w(RSL)}$ refers to the time $\overline{RS}$ is an input.

9/ This is the minimum time the MP/$\overline{MC}$ pin needs to be stable in order to be recognized by internal logic; however, for proper operation, the user must maintain a valid level for the duration of the entire memory access (or accesses) on- or off-chip.

10/ t_c = system clock cycle time = 1/SYSCLK = $t_{c(SYS)}$.

11/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.

12/ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

13/ The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.

14/ The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.

15/ The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is set.

16/ Absolute resolution = 4.89 mV. At V_{REFHI} = 5 V and V_{REFLO} = 0 V, this is one LSB. As V_{REFHI} decreases, V_{REFLO} increases, ot both, the LSB sizes decrease. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

17/ The total sample/hold and conversion time is determined by the summation of $t_{d(SOC-SH)}$, $t_{w(SH)}$, $t_{w(C)}$, and $t_{d(EOC-FIFO)}$.

18/ Start of conversion is signaled by the ADCIMSTART bit or the ADCSOC bit set in software, the external start signal active (ADCSOC), or internal EVSOC signal active.

19/ These parameters are used in the flash programming algorithms.

20/ Refer to the recommended operating conditions section for the flash programming operating temperature range when programming flash.

Case outline X

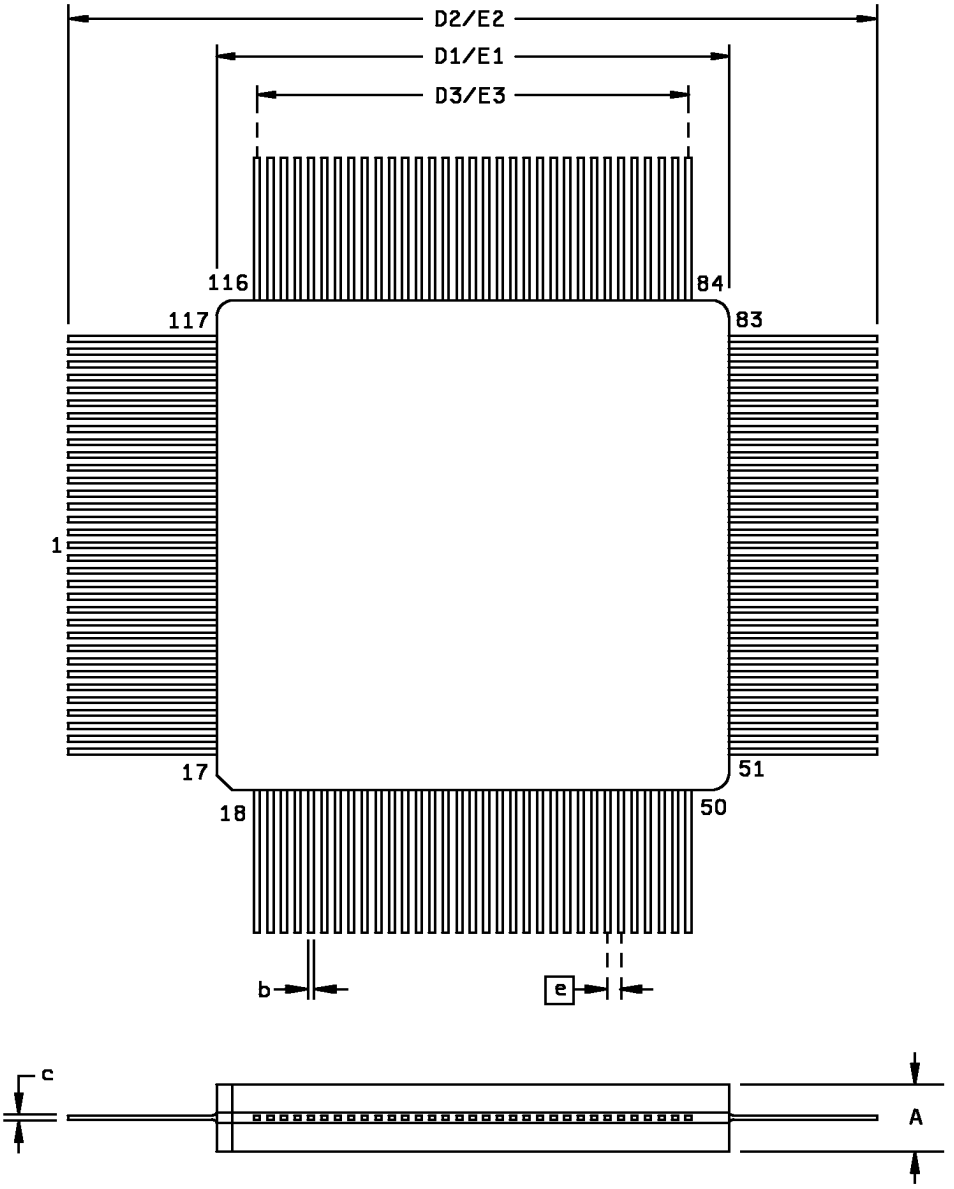


FIGURE 1. Case outline.

Case outline X - Continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.79	3.81	.110	.150
b	0.20	0.36	.008	.014
c	0.10	0.20	.004	.008
D1/E1	23.75	24.51	.935	.965
D2/E2	37.08	39.12	1.460	1.540
D3/E3	20.32 TYP		.800 TYP	
e	0.635 BSC		.025 BSC	

FIGURE 1. Case outline – Continued.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{WE}$	23	D10	45	SPISIMO/IO
2	DV_{DD}	24	D11	46	V_{SS}
3	V_{SS}	25	D12	47	DV_{DD}
4	R/$\overline{W}$	26	D13	48	SPISOMI/IO
5	$\overline{BR}$	27	D14	49	SPICLK/IO
6	$\overline{STRB}$	28	D15	50	V_{CCP}/WDDIS
7	CV_{DD}	29	V_{SS}	51	SPISTE/IO
8	CV_{SS}	30	TCK	52	$\overline{PDPINT}$
9	D0	31	TDI	53	XINT1
10	D1	32	$\overline{TRST}$	54	XINT2/IO
11	D2	33	TMS	55	XINT3/IO
12	D3	34	TDO	56	$\overline{OSCBYP}$
13	DV_{DD}	35	$\overline{RS}$	57	XTAL2
14	V_{SS}	36	READY	58	XTAL1/CLKIN
15	D4	37	MP/$\overline{MC}$	59	V_{SS}
16	D5	38	EMU0	60	CV_{DD}
17	D6	39	EMU1/$\overline{OFF}$	61	V_{SS}
18	D7	40	NMI	62	DV_{DD}
19	D8	41	$\overline{PORESET}$	63	ADCSOC/IOPC0
20	V_{SS}	42	RESERVED	64	CLKOUT/IOPC1
21	DV_{DD}	43	SCIRXD/IO	65	XF/IOPC2
22	D9	44	SCITXD/IO	66	$\overline{BIO}$ /IOPC3

FIGURE 2. Terminal connections.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
67	CAP1/QEP1/IOPC4	89	ADCIN10	111	A1
68	CAP2/QEP2/IOPC5	90	ADCIN9/IOPA2	112	A2
69	CAP3/IOPC6	91	ADCIN8/IOPA3	113	V_{SS}
70	CAP4/IOPC7	92	V_{SS}	114	A3
71	V_{SS}	93	DV_{DD}	115	A4
72	ADCIN0/IOPA0	94	PWM1/CMP1	116	A5
73	ADCIN1/IOPA1	95	PWM2/CMP2	117	A6
74	ADCIN2	96	PWM3/CMP3	118	A7
75	ADCIN3	97	PWM4/CMP4	119	A8
76	ADCIN4	98	PWM5/CMP5	120	V_{SS}
77	ADCIN5	99	PWM6/CMP6	121	DV_{DD}
78	ADCIN6	100	PWM7/CMP7/IOPB0	122	A9
79	ADCIN7	101	PWM8/CMP8/IOPB1	123	A10
80	ADCIN15	102	PWM9/CMP9/IOPB2	124	A11
81	ADCIN14	103	DV_{DD}	125	A12
82	ADCIN13	104	V_{SS}	126	A13
83	ADCIN12	105	T1PWM/T1CMP/IOPB3	127	A14
84	V_{CCA}	106	T2PWM/T2CMP/IOPB4	128	A15
85	V_{REFHI}	107	T3PWM/T3CMP/IOPB5	129	$\overline{DS}$
86	V_{REFLO}	108	TMRDIR/IOPB6	130	$\overline{IS}$
87	V_{SSA}	109	TMRCLK/IOPB7	131	$\overline{PS}$
88	ADCIN11	110	A0	132	W/$\overline{R}$

FIGURE 2. Terminal connections - Continued.

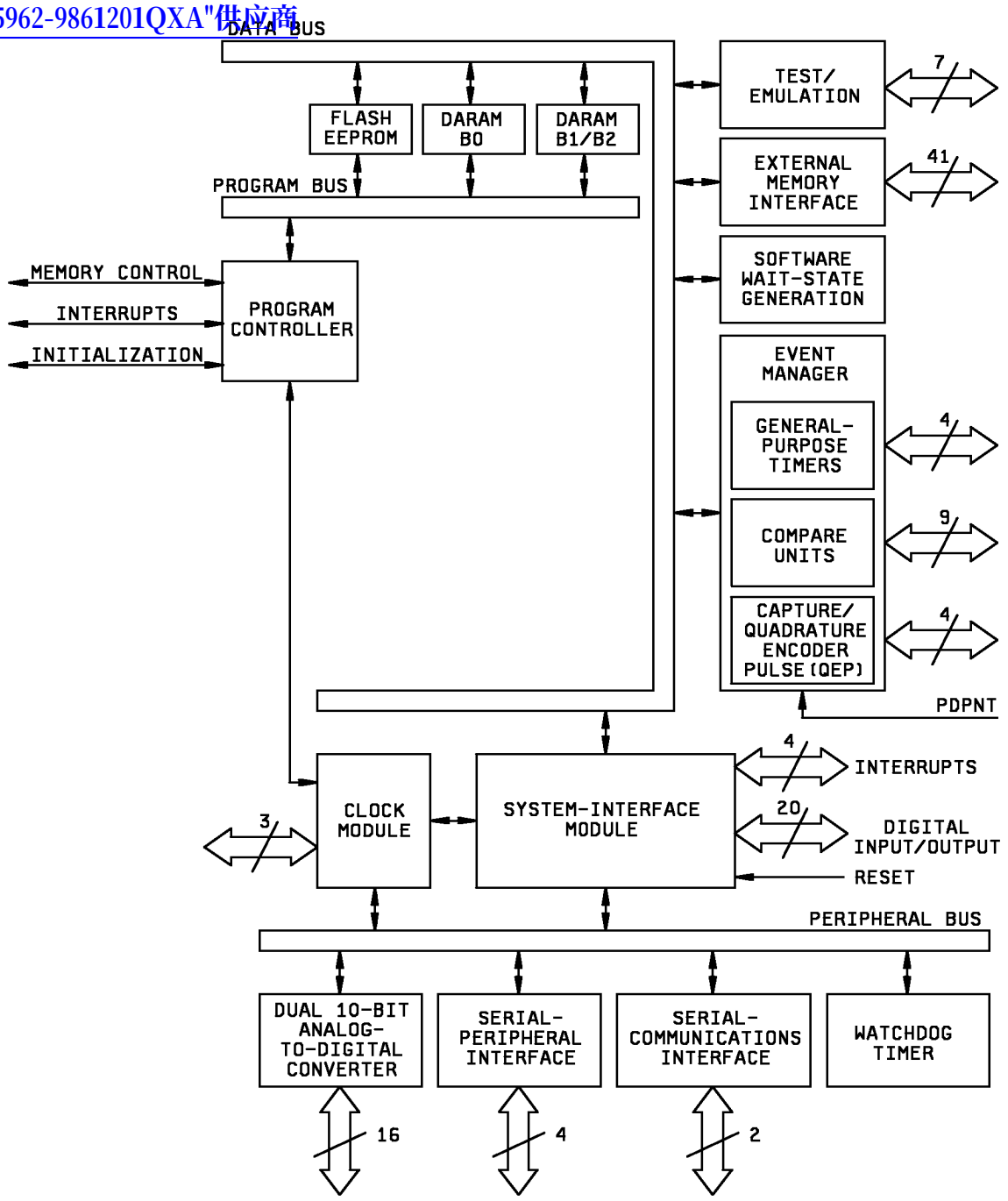
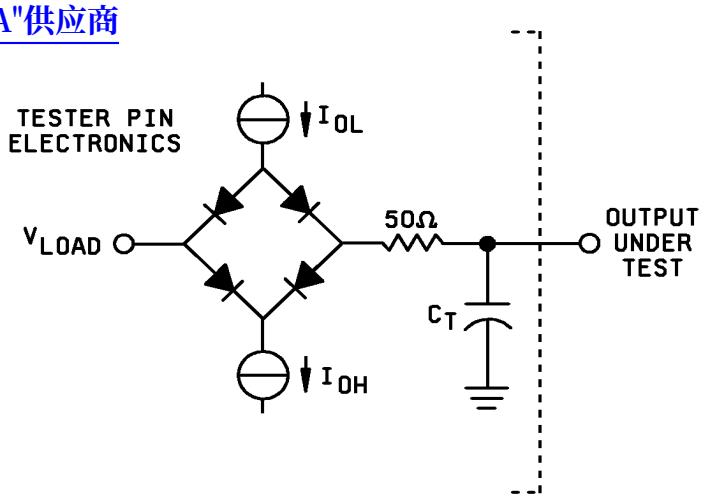


FIGURE 3. Block diagram.

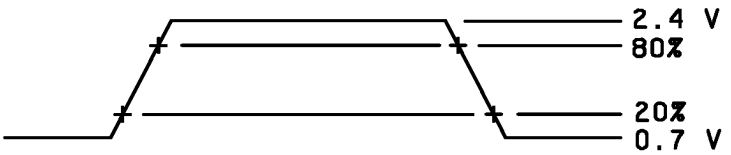
Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	TRIBYP
00000011	INTEST

FIGURE 4. Boundary scan instruction codes.

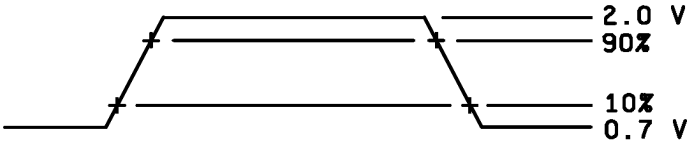


NOTES: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 A (all outputs)
V_{LOAD} = 1.5 V
C_T = 110-pF typical load-circuit capacitance

TEST LOAD CIRCUIT

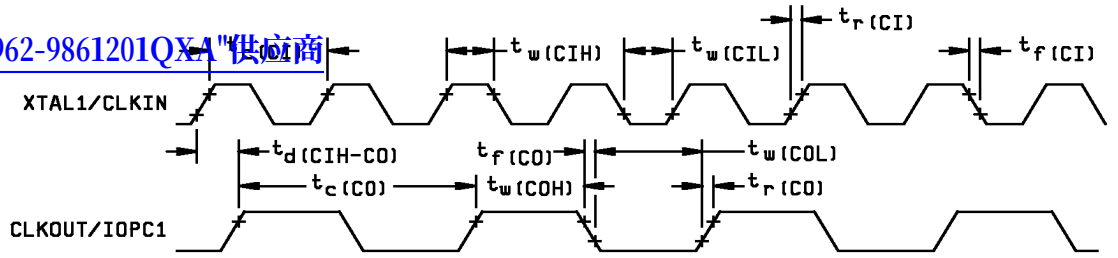


TTL-LEVEL OUTPUTS

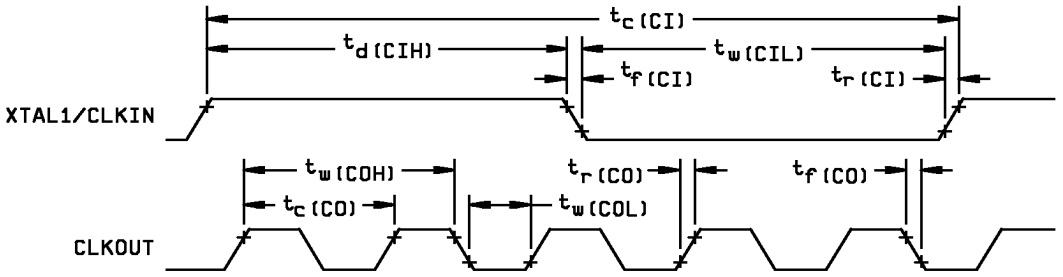


TTL-LEVEL INPUTS

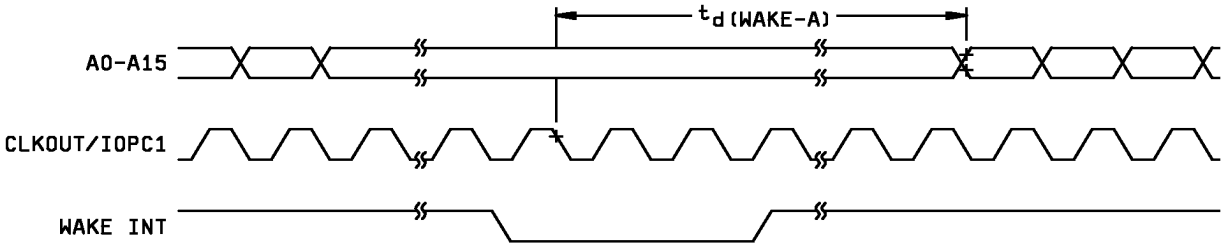
FIGURE 5. Test circuit and timing waveforms.



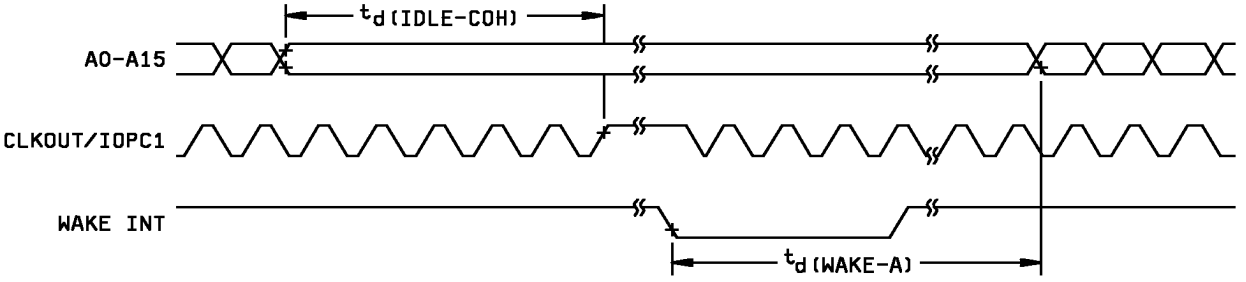
EXTERNAL DIVIDE-BY-TWO CLOCK TIMINGS



CLKIN-TO-CLKOUT TIMINGS FOR PLL OSCILLATOR MODE,
MULTIPLY-BY-5 OPTION WITH 4-MHz CRYSTAL

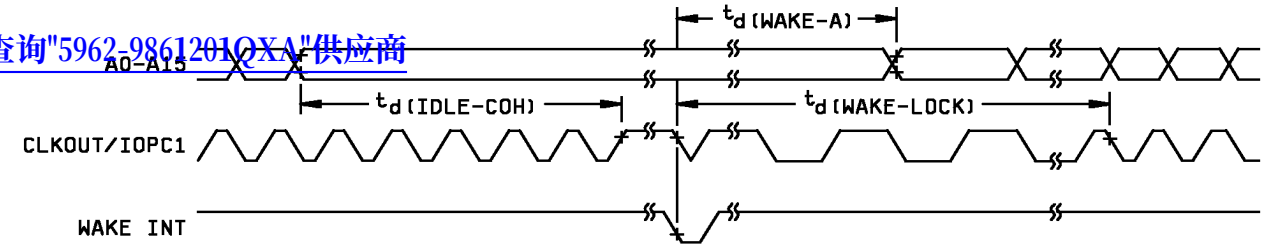


IDLE1 ENTRY AND EXIT TIMINGS

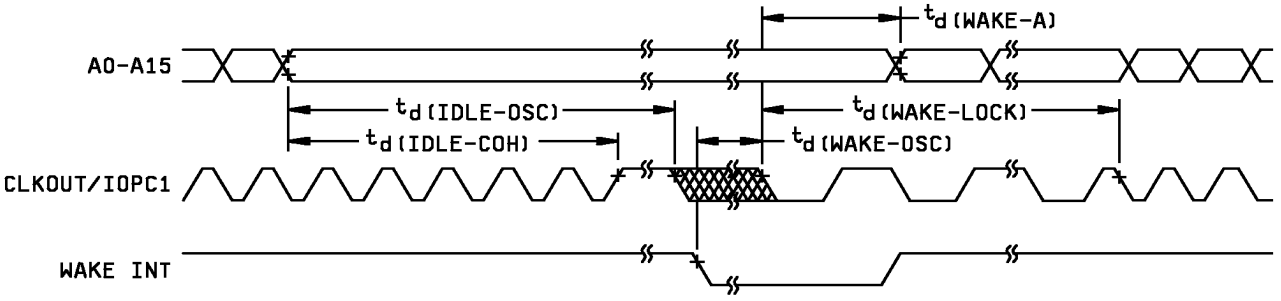


IDLE2 ENTRY AND EXIT TIMINGS

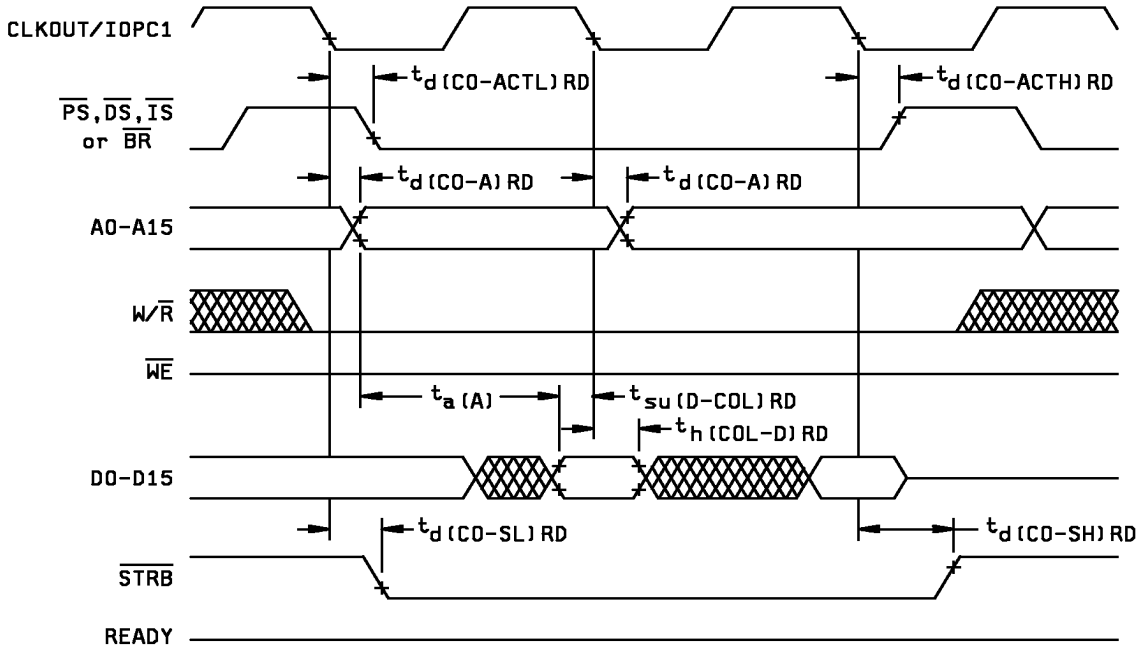
FIGURE 5. Test circuit and timing waveforms - Continued.



PLL POWER-DOWN ENTRY AND EXIT TIMINGS

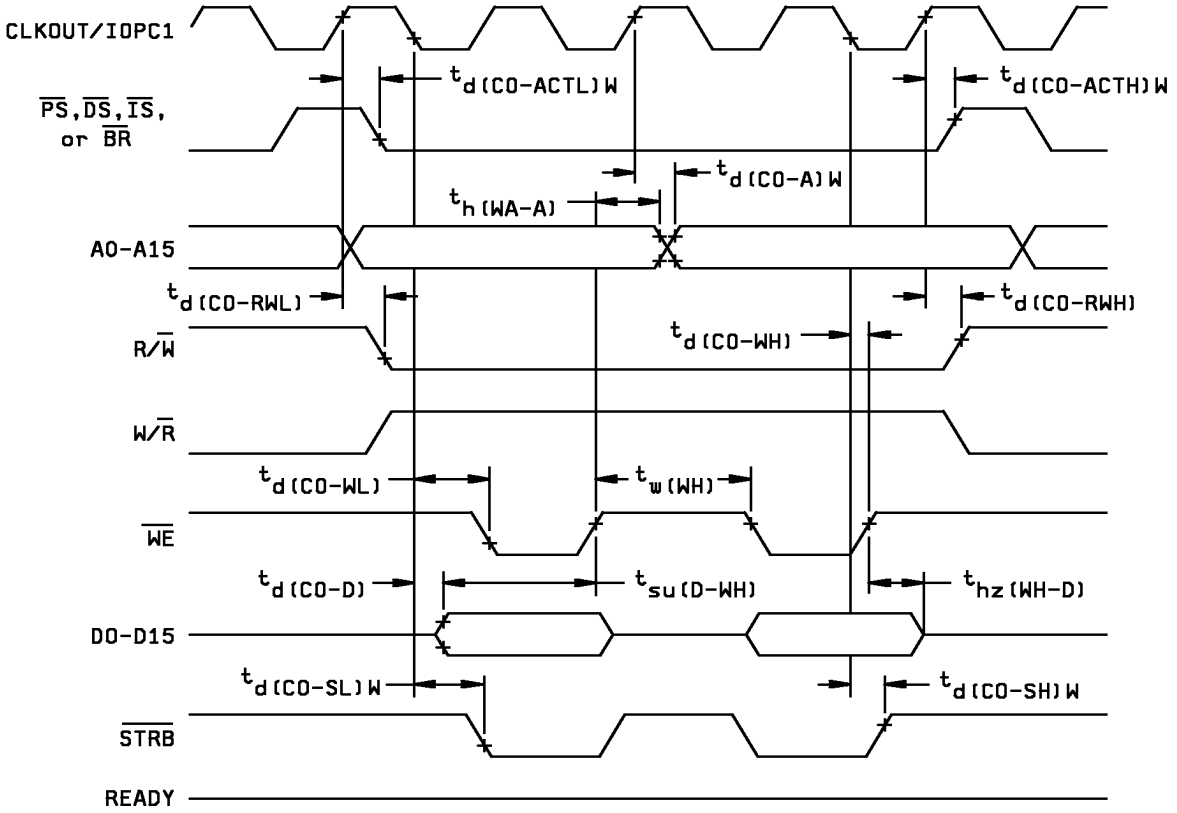


OSC POWER-DOWN ENTRY AND EXIT TIMINGS



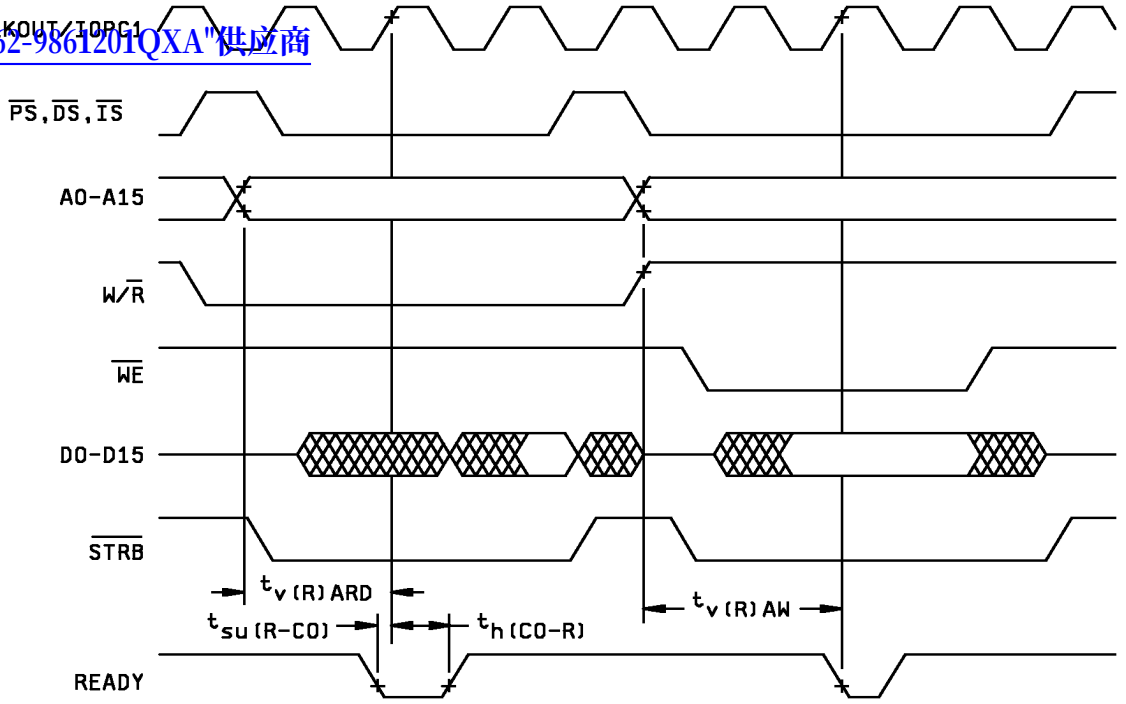
MEMORY INTERFACE READ TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.

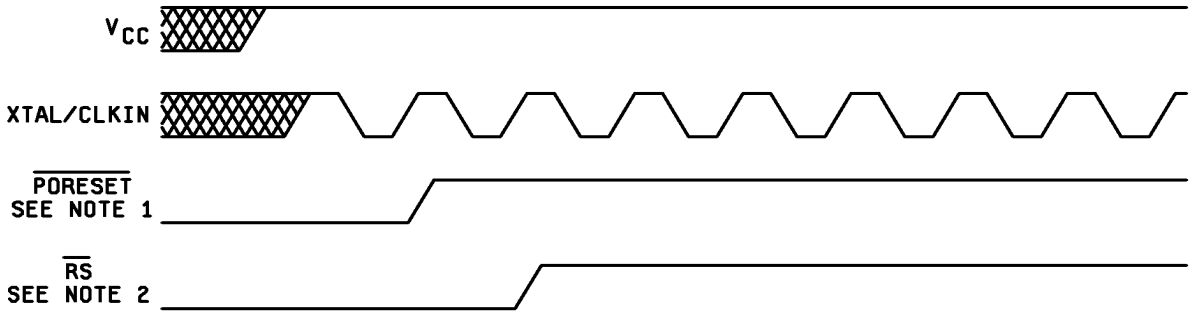


MEMORY INTERFACE WRITE TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.



READY TIMINGS

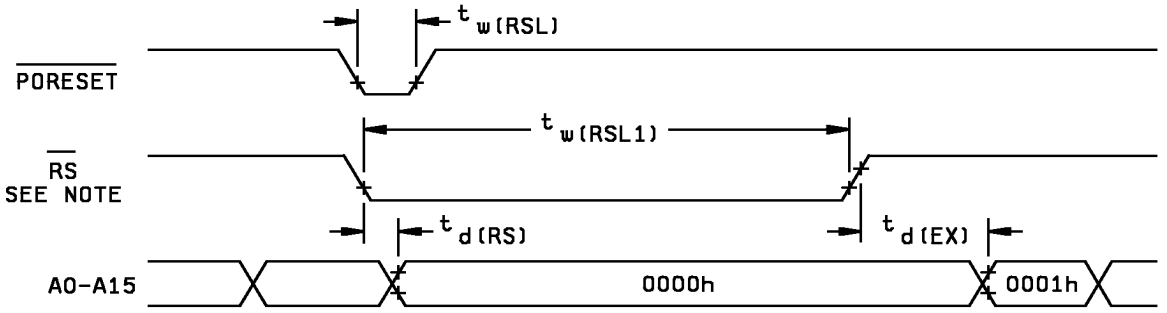


RESET TIMINGS

NOTES:

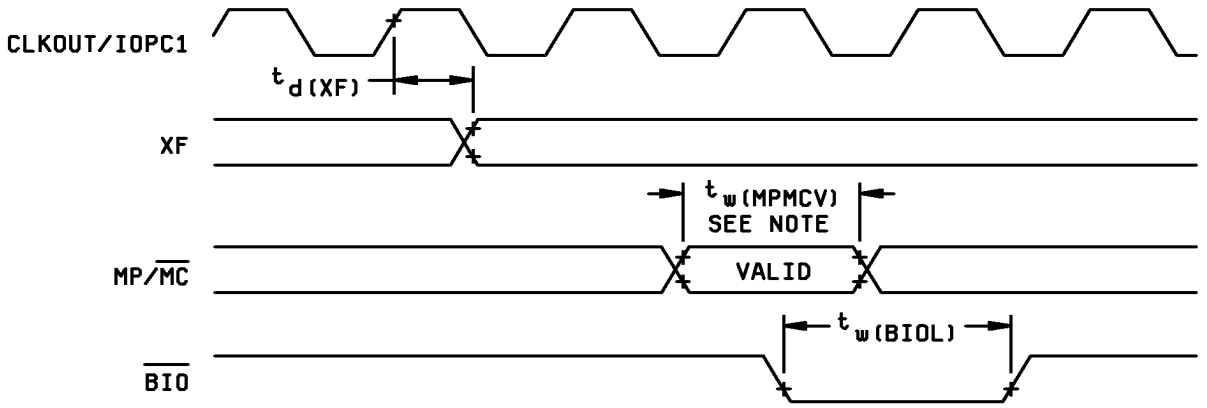
1. $\overline{\text{PORESET}}$ is required to be driven low during power up to ensure all clock/PLL registers are reset to a known state.
2. $\overline{\text{RS}}$ is a bidirectional (open-drain output) pin and can be optionally pulled low through an open-drain or open-collector drive circuit, or through a 2.7-k resistor in series with a totem pole drive circuit. If $\overline{\text{RS}}$ is left undriven, then a 20-k pullup resistor should be used.

FIGURE 5. Test circuit and timing waveforms - Continued.



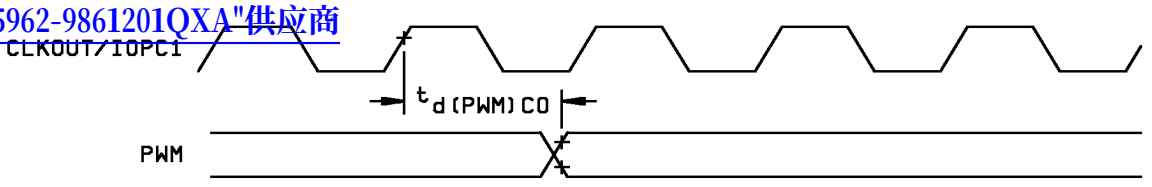
POWER-ON RESET TIMINGS

NOTE: $\overline{RS}$ is driven low by any device reset, which includes asserting $\overline{PORESET}$, $\overline{RS}$, access to an illegal address, execution of a software reset, or a watchdog timer reset.

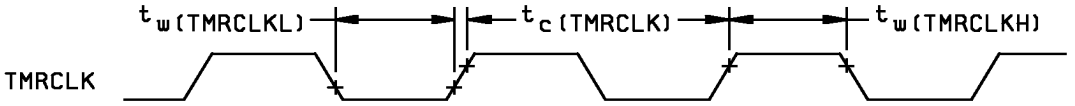


XF, $\overline{BIO}$, AND MP/$\overline{MC}$ TIMINGS

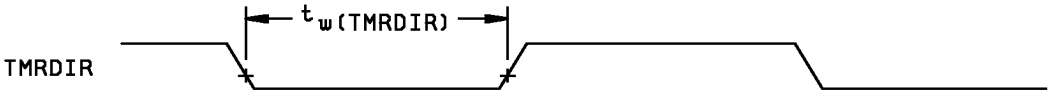
FIGURE 5. Test circuit and timing waveforms - Continued.



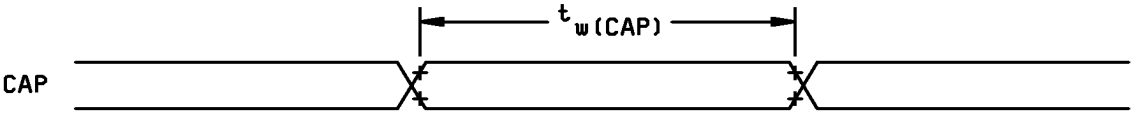
PWM AND COMPARE OUTPUT TIMINGS



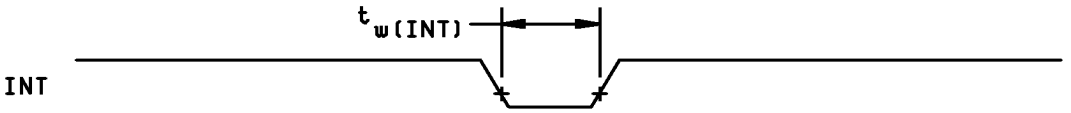
EXTERNAL TIMER CLOCK INPUT TIMINGS



EXTERNAL TIMER DIRECTION INPUT TIMINGS

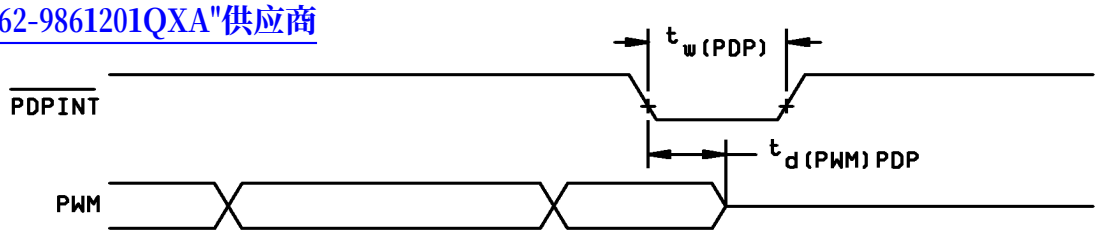


CAPTURE AND QEP INPUT TIMINGS

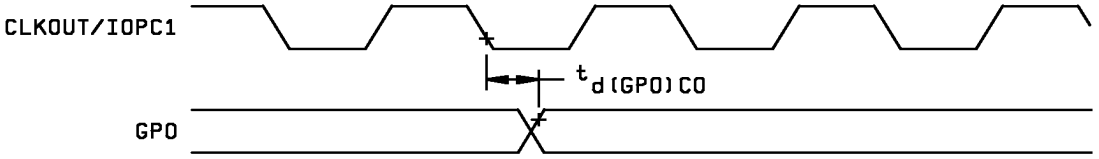


EXTERNAL INTERRUPT TIMINGS

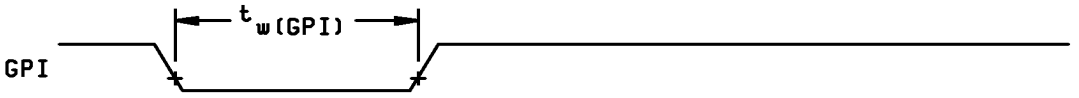
FIGURE 5. Test circuit and timing waveforms - Continued.



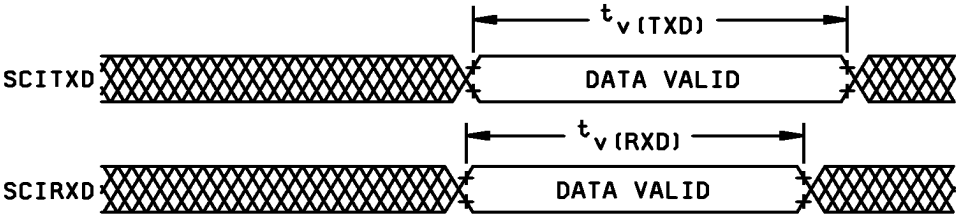
POWER-DRIVE PROTECTION INTERRUPT TIMINGS



GENERAL-PURPOSE OUTPUT TIMINGS

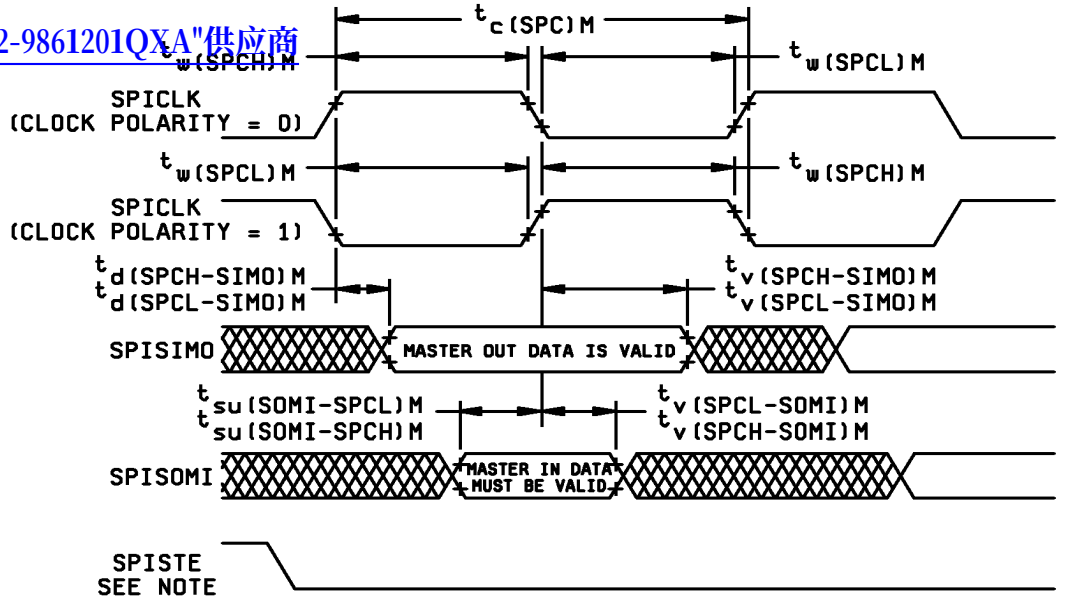


GENERAL-PURPOSE INPUT TIMINGS

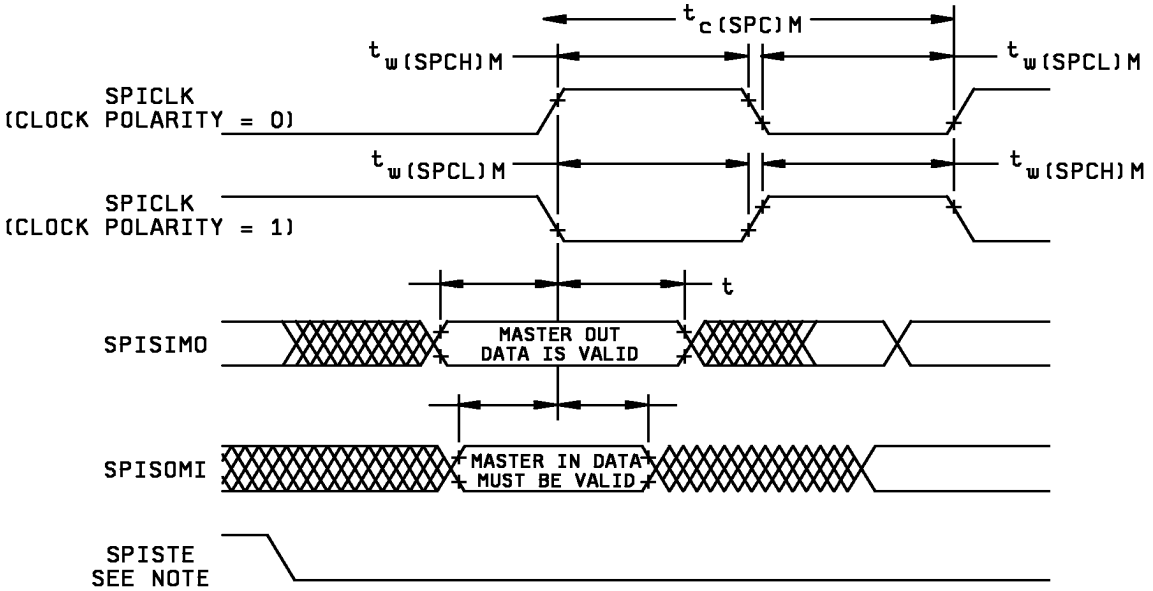


SCI TIMINGS

FIGURE 5. Test circuit and timing waveforms - Continued.



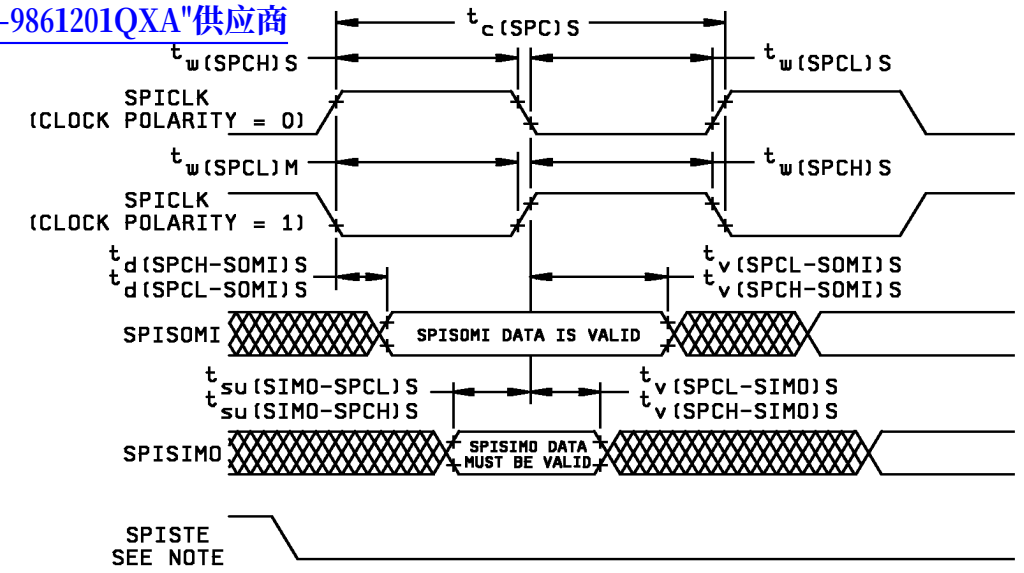
SPI MASTER MODE EXTERNAL TIMINGS (CLOCK PHASE = 0)



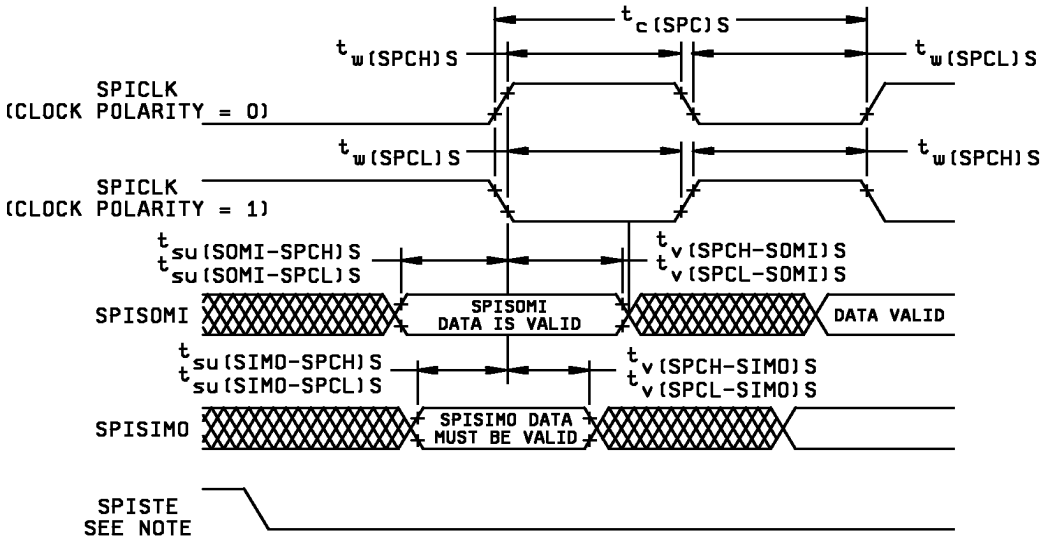
SPI MASTER MODE EXTERNAL TIMINGS (CLOCK PHASE = 1)

NOTE: The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

FIGURE 5. Test circuit and timing waveforms - Continued.



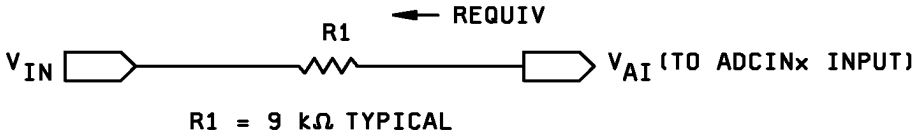
SPI SLAVE MODE EXTERNAL TIMING (CLOCK PHASE = 0)



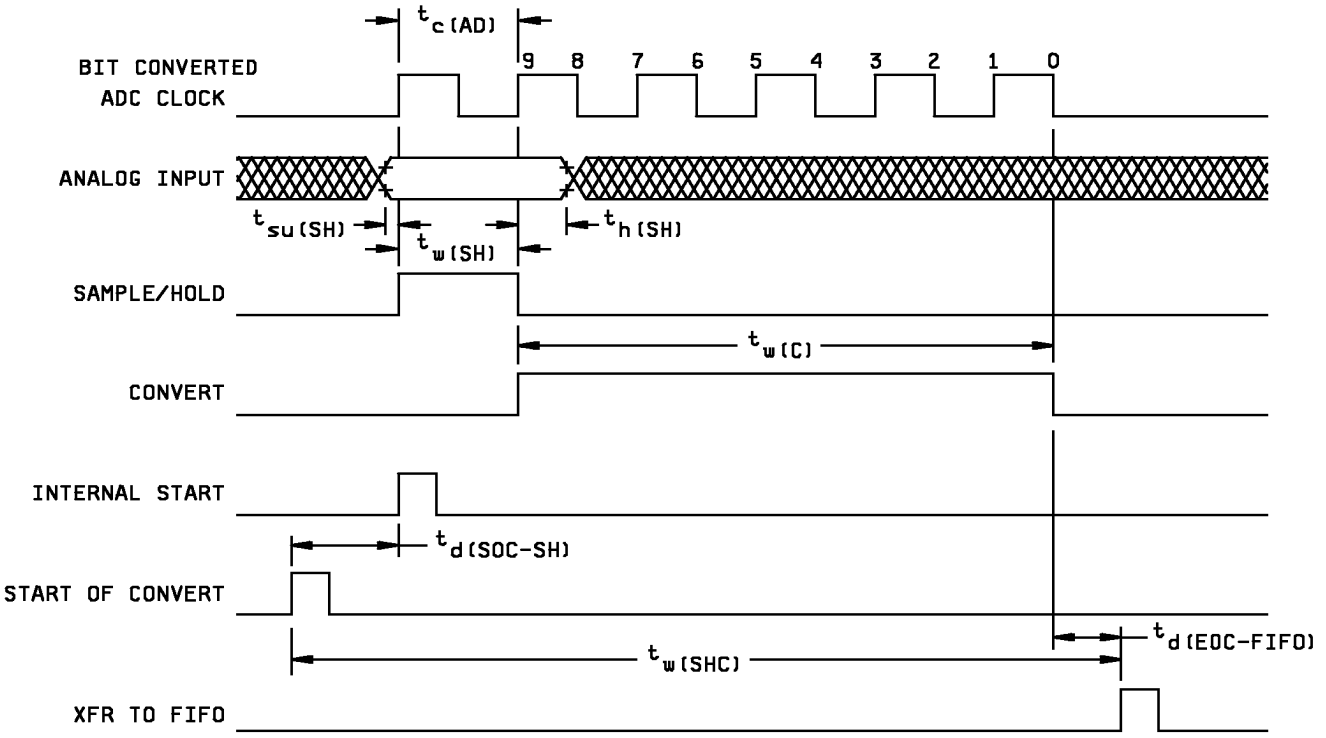
SPI SLAVE MODE EXTERNAL TIMING (CLOCK PHASE = 1)

NOTE: The SPISTE signal must be active before the SPI communication stream starts; the SPISTE signal must remain active until the SPI communication stream is complete.

FIGURE 5. Test circuit and timing waveforms - Continued.

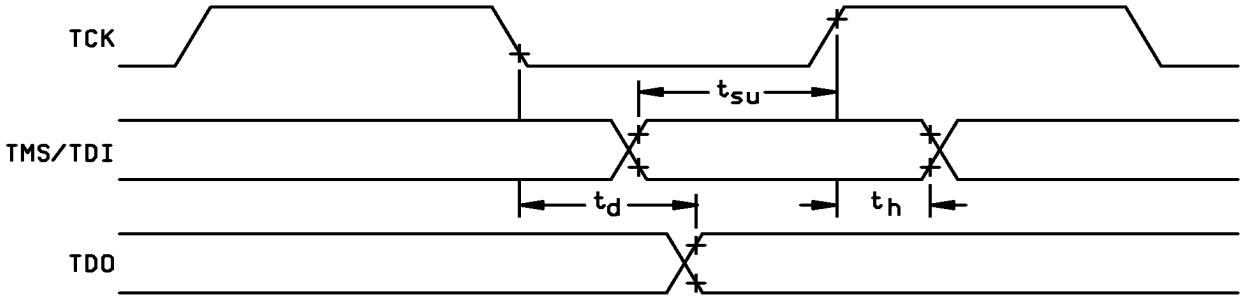


TYPICAL ADC INPUT PIN CIRCUIT



ANALOG-TO-DIGITAL TIMING

FIGURE 5. Test circuit and timing waveforms - Continued.



JTAG TIMING

FIGURE 5. Test circuit and timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125 C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A. 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125 C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25 C 5 C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Terminal descriptions.

Terminal name	Type 1/	Description
EXTERNAL INTERFACE DATA/ADDRESS SIGNALS		
A0 through A15	O/Z	Parallel address bus A0 [least significant bit (LSB)] through A15 [most significant bit (MSB)]. A15-A0 are multiplexed to address external data/program memory or I/O. A15-A0 are placed in the high-impedance state when EMU1/$\overline{\text{OFF}}$ is active low and hold their previous states in power-down modes.
D0 through D15	I/O/Z	Parallel data bus D0 (LSB) through D15 (MSB). D15-D0 are multiplexed to transfer data between the device and external data/program memory and I/O space (devices). D15-D0 are placed in the high-impedance state when not outputting, when in power-down mode, when reset ($\overline{\text{RS}}$) is asserted, or when EMU1/$\overline{\text{OFF}}$ is active low.
EXTERNAL INTERFACE CONTROL SIGNALS		
$\overline{\text{DS}}$, $\overline{\text{PS}}$, $\overline{\text{IS}}$	O/Z	Data, program, and I/O space select signals. $\overline{\text{DS}}$, $\overline{\text{PS}}$, and $\overline{\text{IS}}$ are always high unless low-level asserted for communication to a particular external space. They are placed in the high-impedance state during reset, power down, and when EMU1/$\overline{\text{OFF}}$ is active low.
READY	I	Data ready. READY indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again.
R/$\overline{\text{W}}$	O/Z	Read/write signal. R/$\overline{\text{W}}$ indicates transfer direction during communication to an external device. It is normally in read mode (high), unless low level is asserted for performing a write operation. It is placed in the high-impedance state during reset, power down, and when EMU1/$\overline{\text{OFF}}$ is active low.
$\overline{\text{STRB}}$	O/Z	Strobe. $\overline{\text{STRB}}$ is always high unless asserted low to indicate an external bus cycle. It is placed in the high-impedance state during reset, power down, and when EMU1/$\overline{\text{OFF}}$ is active low.
$\overline{\text{WE}}$	O/Z	Write enable. The falling edge of $\overline{\text{WE}}$ indicates that the device is driving the external data bus (D15-D0). Data can be latched by an external device on the rising edge of $\overline{\text{WE}}$. $\overline{\text{WE}}$ is active on all external program, data, and I/O writes. $\overline{\text{WE}}$ goes in the high-impedance state following reset and when EMU1/$\overline{\text{OFF}}$ is active low.
W/$\overline{\text{R}}$	O/Z	Write/read. W/$\overline{\text{R}}$ is an inverted form of R/$\overline{\text{W}}$ and can connect directly to the output enable of external devices. W/$\overline{\text{R}}$ is placed in the high-impedance state following reset and when EMU1/$\overline{\text{OFF}}$ is active low.
$\overline{\text{BR}}$	O/Z	Bus request. $\overline{\text{BR}}$ is asserted during access of external global data memory space. $\overline{\text{BR}}$ can be used to extend the data memory address space by up to 32K words. $\overline{\text{BR}}$ goes in the high-impedance state during reset, power down, and when EMU1/$\overline{\text{OFF}}$ is active low.
V_{CCP}/WDDIS	I	Flash-programming voltage supplyl lf. V_{CCP} = 5 V, then WRITE/ERASE can be made to the ENTIRE on-chip flash memory block - that is, for programming the flash. If V_{CCP} = 0 V, then WRITE/ERASE of the flash memory is not allowed, thereby protecting the entire memory block from being overwritten. WDDIS also functions as a hardware watchdog disable. The watchdog timer is disabled when V_{CCP}/WDDIS = 5 V and bit 6 in WDCR is set to 1.

See foonotes at end of table.

TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
ADC INPUTS (UNSHARED)		
ADCIN2 through ADCIN7	I	Analog inputs to the first ADC.
ADCIN10 through ADCIN15	I	Analog inputs to the second ADC
BIT I/O AND SHARED FUNCTIONS PINS		
ADCIN0/IOPA0	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN0/IOPA0 is configured as a digital input by all device resets.
ADCIN1/IOPA1	I/O	Bidirectional digital I/O. Analog input to the first ADC. ADCIN1/IOPA1 is configured as a digital input by all device resets.
ADCIN9/IOPA2	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN9/IOPA2 is configured as a digital input by all device resets.
ADCIN8/IOPA3	I/O	Bidirectional digital I/O. Analog input to the second ADC. ADCIN8/IOPA3 is configured as a digital input by all device resets.
PWM7/CMP7/ IOPB0	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 1 output. The state of PWM7/CMP7/IOPB0 is determined by the simple compare/PWM and the simple action control register (SACTR). It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM7/CMP7/IOPB0 is configured as a digital input by all device resets.
PWM8/CMP8/ IOPB1	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 2 output. The state of PWM8/CMP8/IOPB1 is determined by the simple compare/PWM and the SACTR. It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM8/CMP8/IOPB1 is configured as a digital input by all device resets.
PWM9/CMP9/ IOPB2	I/O/Z	Bidirectional digital I/O. Simple compare/PWM 3 output. The state of PWM9/CMP9/IOPB2 is determined by the simple compare/PWM and the SACTR. It goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. PWM9/CMP9/IOPB2 is configured as a digital input by all device resets.
T1PWM/T1CMP/ IOPB3	I/O/Z	Bidirectional digital I/O. Timer 1 compare output. T1PWM/T1CMP/IOPB3 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T2PWM/T2CMP/ IOPB4	I/O/Z	Bidirectional digital I/O. Timer 2 compare output. T2PWM/T2CMP/IOPB4 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
T3PWM/T3CMP/ IOPB5	I/O/Z	Bidirectional digital I/O. Timer 3 compare output. T3PWM/T3CMP/IOPB5 goes to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low. This pin is configured as a digital input by all device resets.
TMRDIR/IOPB6	I/O	Bidirectional digital I/O. Direction signal for the timers. Up-counting direction if TMRDIR/IOPB6 is low, down-counting direction if this pin is high. This pin is configured as a digital input by all device resets.
TMRCLK/IOPB7	I/O	Bidirectional digital I/O. External clock input for general-purpose timers. This pin is configured as a digital input by all device resets.

See footnotes at end of table.

TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
BIT I/O AND SHARED FUNCTIONS PINS – CONTINUED		
ADCSOC/IOPC0	I/O	Bidirectional digital I/O. External start of conversion input for ADC. This pin is configured as a digital input by all device resets.
CAP1/QEP1/ IOPC4	I/O	Bidirectional digital I/O. Capture 1 or QEP 1 input. This pin is configured as a digital input by all device resets.
CAP2/QEP2/ IOPC5	I/O	Bidirectional digital I/O. Capture 2 or QEP 2 input. This pin is configured as a digital input by all device resets.
CAP3/IOPC6	I/O	Bidirectional digital I/O. Capture 3 input. This pin is configured as a digital input by all device resets.
CAP4/IOPC7	I/O	Bidirectional digital I/O. Capture 4 input. This pin is configured as a digital input by all device resets.
XF/IOPC2	I/O	Bidirectional digital I/O. External flag output (latched software-programmable signal). XF is used for signaling other processors in multiprocessing configurations or as a general-purpose output pin. This pin is configured as an external flag output by all device resets.
$\overline{\text{BIO}}$ /IOPC3	I/O	Bidirectional digital I/O. Branch control input. $\overline{\text{BIO}}$ is polled by the BIOZ instruction. If $\overline{\text{BIO}}$ is low, the CPU executes a branch. If $\overline{\text{BIO}}$ is not used, it should be pulled high. This pin is configured as a branch-control input by all device resets.
CLKOUT/IOPC1	I/O	Bidirectional digital I/O. Clock output. Clock output is selected by the CLKSRC bits in the SYSCR register. This pin is configured as a DSP clock output by a power-on reset.
SERIAL COMMUNICATIONS INTERFACE (SCI) AND BIT I/O PINS		
SCITXD/IO	I/O	SCI asynchronous serial port transmit data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SCIRXD/IO	I/O	SCI asynchronous serial port receive data, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SERIAL PERIPHERAL INTERFACE (SPI) AND BIT I/O PINS		
SPISIMO/IO	I/O	SPI slave in, master out, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISOMI/IO	I/O	SPI slave out, master in, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPICLK/IO	I/O	SPI clock, or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
SPISTE/IO	I/O	SPI slave transmit enable (optional), or general-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
COMPARE SIGNALS		
PWM1/CMP1 through PWM6/CMP6	O/Z	Compare units compare or PWM outputs. The state of these pins is determined by the compare/PWM and the full action control register (ACTR). CMP1-CMP6 go to the high-impedance state when unmasked $\overline{\text{PDPINT}}$ goes active low, and when reset ($\overline{\text{RS}}$) is asserted.

See footnotes at end of table.

TABLE III. Terminal descriptions – Continued.

Terminal name	Type 1/	Description
INTERRUPT AND MISCELLANEOUS SIGNALS		
$\overline{RS}$	I/O	Reset input. $\overline{RS}$ causes the device to terminate execution and sets PC = 0. When $\overline{RS}$ is brought to a high level, execution begins at location zero of program memory. $\overline{RS}$ affects (or sets to zero) various registers and status bits. $\overline{RS}$ is a bidirectional (open-drain output) pin.
MP/$\overline{MC}$	I	MP/ $\overline{MC}$ (microprocessor/microcomputer) select. If MP/$\overline{MC}$ is low, internal program memory is selected. If it is high, external program memory is selected.
NMI	I	Nonmaskable interrupt. When NMI is activated, the device is interrupted regardless of the state of the INTM bit of the status register. NMI has programmable polarity.
$\overline{PORESET}$	I	Power-on reset. $\overline{PORESET}$ causes the device to terminate execution and sets PC = 0. When $\overline{PORESET}$ is brought to a high level, execution begins at location zero of program memory. $\overline{PORESET}$ affects (or sets to zero) the same registers and status bits as $\overline{RS}$. In addition, $\overline{PORESET}$ initializes the PLL control registers.
XINT1	I	External user interrupt no. 1.
XINT2/IO	I/O	External user interrupt no. 2. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
XINT3/IO	I/O	External user interrupt no. 3. General-purpose bidirectional I/O. This pin is configured as a digital input by all device resets.
$\overline{PDPINT}$	I	Maskable power-drive protection interrupt. If $\overline{PDPINT}$ is unmasked and it goes active low, the timer compare outputs immediately go to the high-impedance state.
CLOCK SIGNALS		
XTAL2	O	PLL oscillator output. XTAL2 is tied to one side of a reference crystal when the device is in PLL mode (CLKMD[1:0] = 1x, CKCR0.7-6). This pin can be left unconnected in oscillator bypass mode ($\overline{OSCBYP}$ V_{IL}). This pin goes in the high-impedance state when EMU1/$\overline{OFF}$ is active low.
XTAL1/CLKIN	I/Z	PLL oscillator input. XTAL1/CLKIN is tied to one side of a reference crystal in PLL mode (CLKMD[1:0] = 1x, CKCR0.7-6), or is connected to an external clock source in oscillator bypass mode ($\overline{OSCBYP}$ V_{IL}).
$\overline{OSCBYP}$	I	Bypass oscillator if low.
SUPPLY SIGNALS		
CV_{ss}	I	Digital core logic ground reference.
V_{SS}	I	Digital logic ground reference.
V_{SSA}	I	Analog ground reference.
DV_{DD} 2/	I	Digital I/O logic supply voltage.
CV_{DD} 2/	I	Digital core logic supply voltage.

See footnotes at end of table.

TABLE III. Terminal descriptions – Continued.

Terminal name	TYPE 1/	Description
SUPPLY SIGNALS – CONTINUED		
V_{CCA}	I	Analog supply voltage.
V_{REFHI}	I	ADC analog voltage reference high.
V_{REFLO}	I	ADC analog voltage reference low.
TEST SIGNALS		
TCK	I	IEEE standard test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on test-access port (TAP) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register of the device core on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard test data input (TDI). TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state when $\overline{OFF}$ is active low.
TMS	I	IEEE standard test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{TRST}$	I	IEEE standard test reset. $\overline{TRST}$, when active low, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored.
EMU0	I/O/Z	Emulator pin 0. When $\overline{TRST}$ is driven low, EMU0 must be high for activation of the $\overline{OFF}$ condition. When $\overline{TRST}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output through the scan.
EMU1/$\overline{OFF}$	I/O/Z	Emulator pin 1/disable all outputs. When $\overline{TRST}$ is driven high, EMU1/$\overline{OFF}$ is used as an interrupt to or from the emulator system and is defined as input/output through JTAG scan. When $\overline{TRST}$ is driven low, this pin is configured as $\overline{OFF}$. When EMU1/$\overline{OFF}$ is active low, it puts all output drivers in the high-impedance state. $\overline{OFF}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications); therefore, for $\overline{OFF}$ condition, the following conditions apply: $\overline{TRST}$ = low, EMU0 = high, EMU1/$\overline{OFF}$ = low.
RESERVED	I	Reserved for test. This pin has an internal pulldown and must be left unconnected for the device.

1/ I = Input; O = Ouput; Z = High impedance.

2/ V_{DD} refers to supply voltage types CV_{DD} (digital core supply voltage), DV_{DD} (digital I/O supply voltage), and V_{DDP} (programming voltage supply). All voltage are measured with respect to V_{SS}.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-04-30

Approved sources of supply for SMD 5962-98612 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9861201QXA	01295	SMJ320F240MHFPM40

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: 6412 U.S Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-0084

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