

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio and WLL applications.

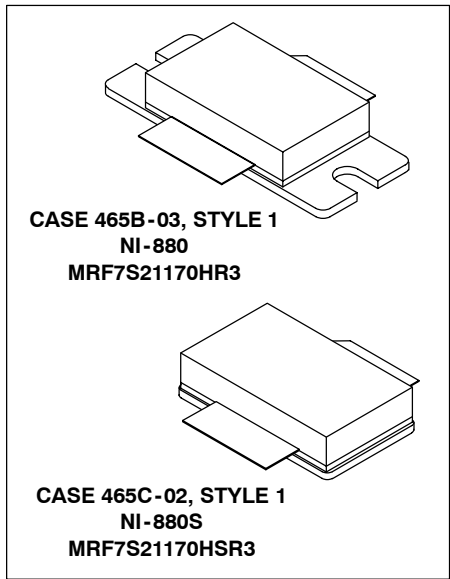
- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1400$  mA,  $P_{out} = 50$  Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.  
 Power Gain — 16 dB  
 Drain Efficiency — 31%  
 Device Output Signal PAR — 6.1 dB @ 0.01% Probability on CCDF  
 ACPR @ 5 MHz Offset — -37 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2140 MHz, 170 Watts CW Output Power
- $P_{out}$  @ 1 dB Compression Point  $\geq 170$  Watts CW

### Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF7S21170HR3**  
**MRF7S21170HSR3**

**2110-2170 MHz, 50 W AVG., 28 V**  
**SINGLE W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 170 W CW Case Temperature 73°C, 25 W CW	$R_{\theta JC}$	0.31 0.36	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	500	nAdc
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 372\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1400\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage <sup>(1)</sup> ( $V_{DD} = 28\text{ Vdc}$ , $I_D = 1400\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.5	5.4	6.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.72\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
<b>Dynamic Characteristics <sup>(2)</sup></b>					
Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.9	—	pF
Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	703	—	pF

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1400\text{ mA}$ ,  $P_{out} = 50\text{ W Avg.}$ ,  $f = 2112.5\text{ MHz}$  and  $f = 2167.5\text{ MHz}$ , Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

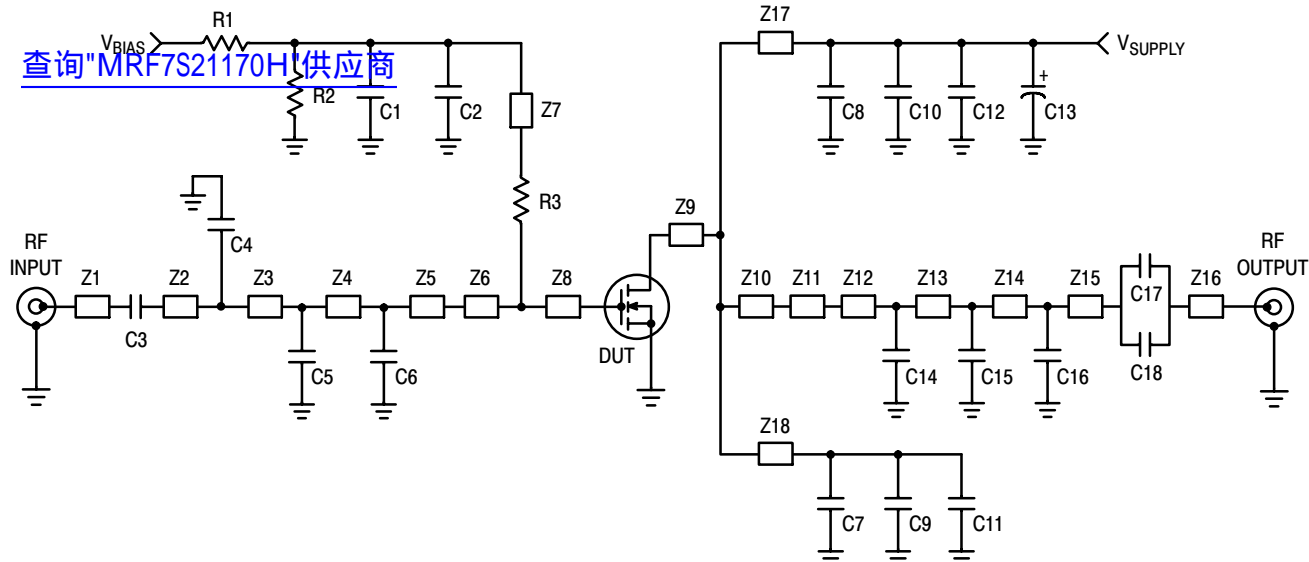
Power Gain	$G_{ps}$	15	16	18	dB
Drain Efficiency	$\eta_D$	29	31	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37	-35	dBc
Input Return Loss	IRL	—	-15	-9	dB

- $V_{GG} = 2 \times V_{GS(Q)}$ . Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part internally matched both on input and output.

(continued)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performances</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28 \text{ Vdc}$ , $I_{DQ} = 1400 \text{ mA}$ , 2110-2170 MHz Bandwidth					
Video Bandwidth @ 170 W PEP $P_{out}$ where $IM3 = -30 \text{ dBc}$ (Tone Spacing from 100 kHz to VBW) $\Delta IMD3 = IMD3 @ \text{VBW frequency} - IMD3 @ 100 \text{ kHz} < 1 \text{ dBc}$ (both sidebands)	VBW	—	25	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 50 \text{ W Avg.}$	$G_F$	—	0.4	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{out} = 170 \text{ W CW}$	$\Phi$	—	1.95	—	°
Average Group Delay @ $P_{out} = 170 \text{ W CW}$ , $f = 2140 \text{ MHz}$	Delay	—	1.7	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 170 \text{ W CW}$ $f = 2140 \text{ MHz}$ , Six Sigma Window	$\Delta\Phi$	—	18	—	°
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.015	—	dB/°C
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta P_{1dB}$	—	0.01	—	dBm/°C



Z1	0.250" x 0.083" Microstrip	Z11	0.060" x 0.760" Microstrip
Z2*	0.090" x 0.083" Microstrip	Z12*	0.129" x 0.083" Microstrip
Z3*	0.842" x 0.083" Microstrip	Z13*	0.436" x 0.083" Microstrip
Z4*	0.379" x 0.083" Microstrip	Z14*	0.490" x 0.083" Microstrip
Z5*	0.307" x 0.083" Microstrip	Z15*	0.275" x 0.083" Microstrip
Z6	0.156" x 0.787" Microstrip	Z16	0.230" x 0.083" Microstrip
Z7	1.160" x 0.080" Microstrip	Z17, Z18	0.900" x 0.080" Microstrip
Z8	0.119" x 0.787" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$
Z9	0.077" x 0.880" Microstrip		
Z10	0.459" x 1.000" Microstrip		

\* Variable for tuning

Figure 1. MRF7S21170HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S21170HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	100 pF Chip Capacitor	ATC100B101JT500XT	ATC
C2, C3, C7, C8, C17, C18	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C4, C15	0.3 pF Chip Capacitors	ATC100B0R3BT500XT	ATC
C5	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C6	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C9, C10, C11, C12	10 $\mu$ F Chip Capacitors	C5750X5R1H106MT	TDK
C13	470 $\mu$ F, 63 V Electrolytic Capacitor, Radial	477KXM063M	Illinois Capacitor
C14	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
C16	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay
R3	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

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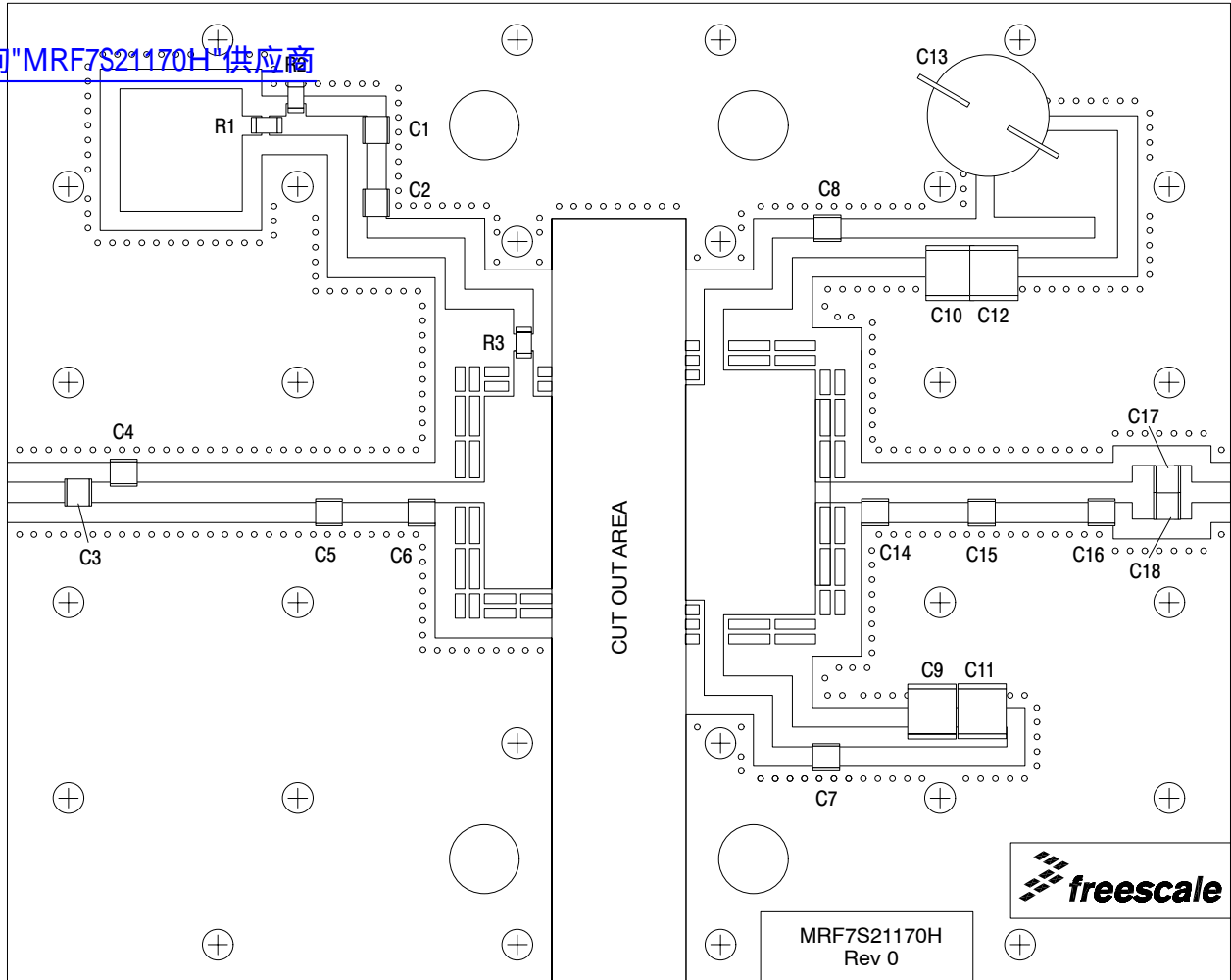
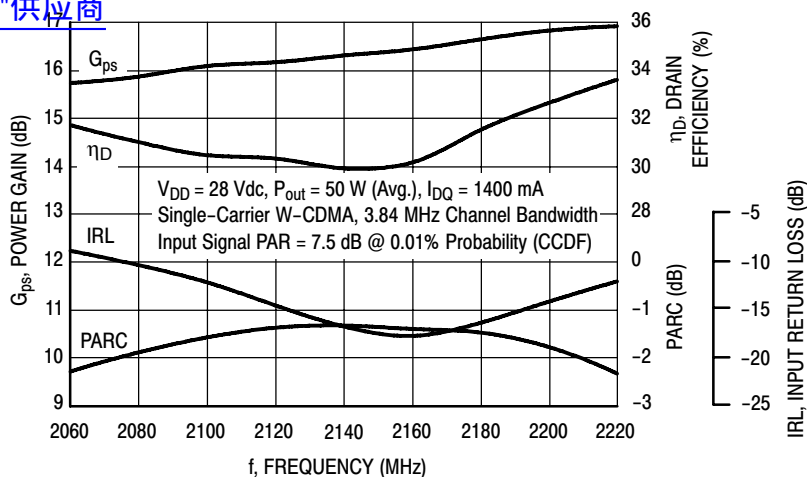


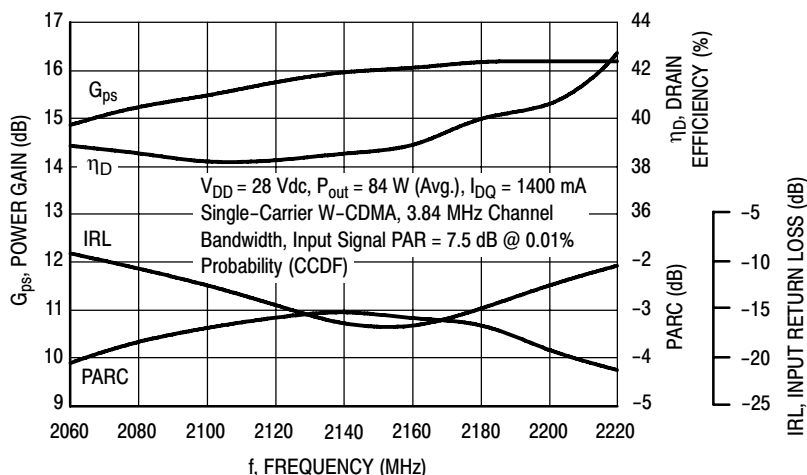
Figure 2. MRF7S21170HR3(HSR3) Test Circuit Component Layout

## TYPICAL CHARACTERISTICS

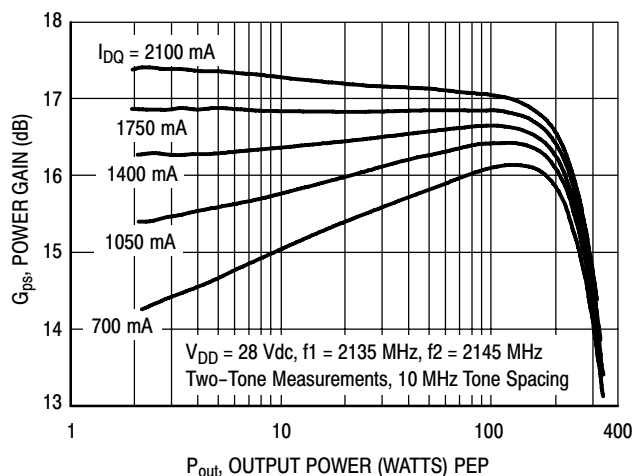
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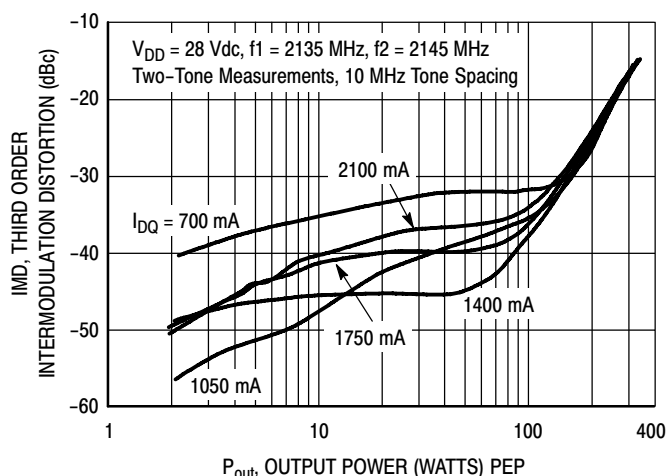
**Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 50$  Watts Avg.**



**Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 84$  Watts Avg.**



**Figure 5. Two-Tone Power Gain versus Output Power**



**Figure 6. Third Order Intermodulation Distortion versus Output Power**

## TYPICAL CHARACTERISTICS

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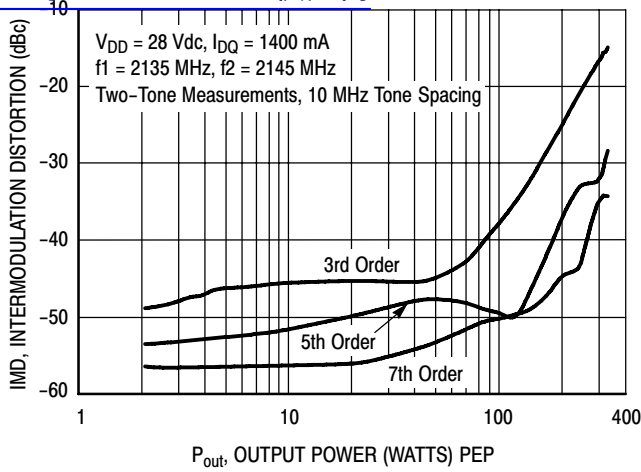


Figure 7. Intermodulation Distortion Products versus Output Power

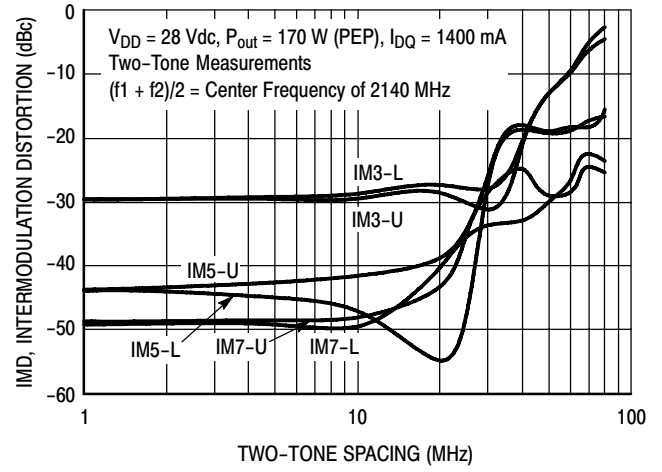


Figure 8. Intermodulation Distortion Products versus Tone Spacing

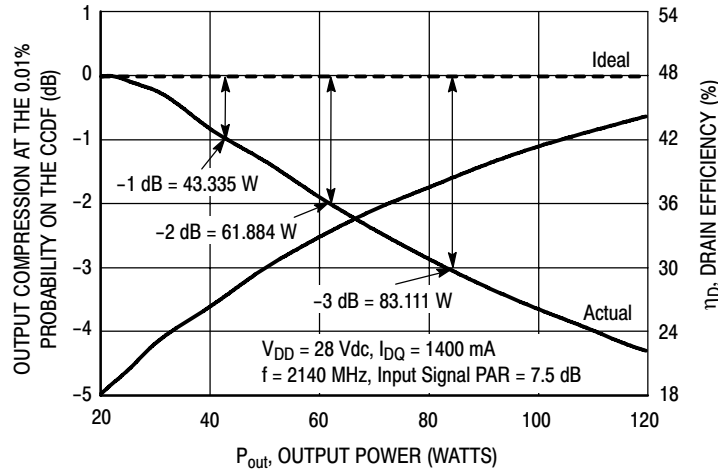


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

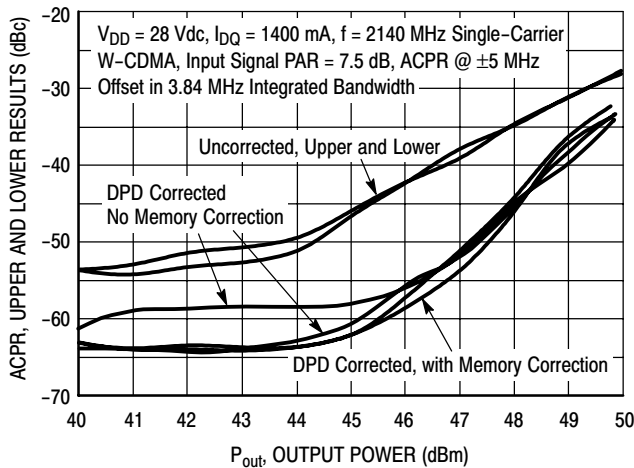


Figure 10. Digital Predistortion Correction versus ACPR and Output Power

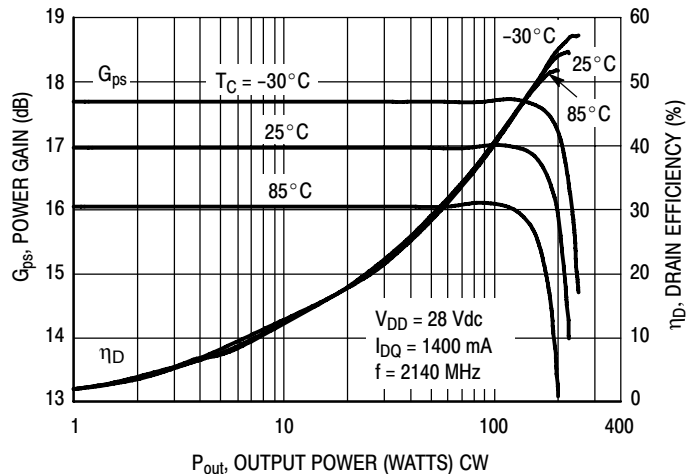


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

MRF7S21170HR3 MRF7S21170HSR3

## TYPICAL CHARACTERISTICS

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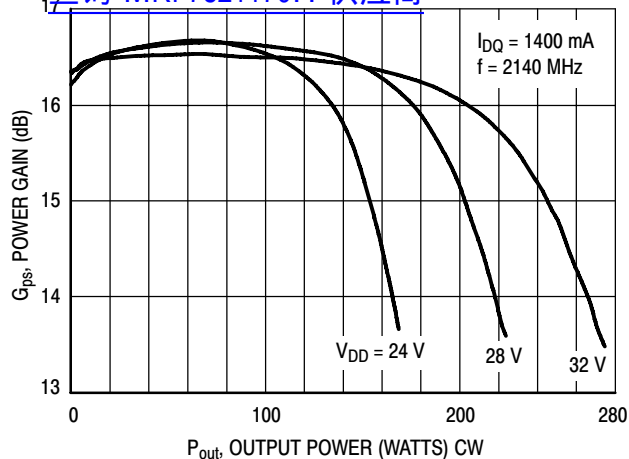
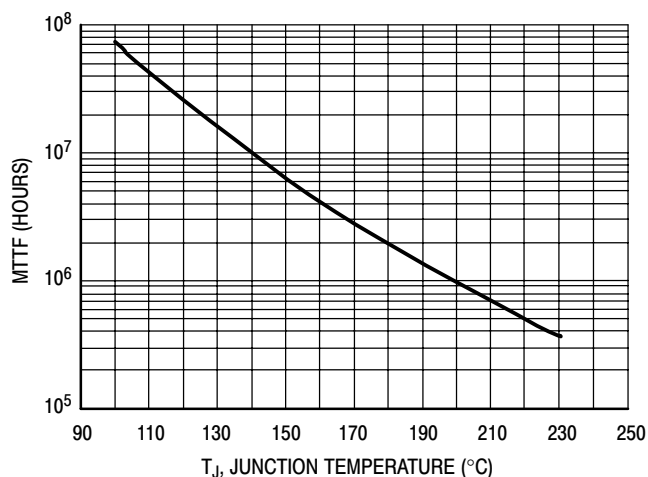


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 50$  W Avg., and  $\eta_D = 31\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

## W-CDMA TEST SIGNAL

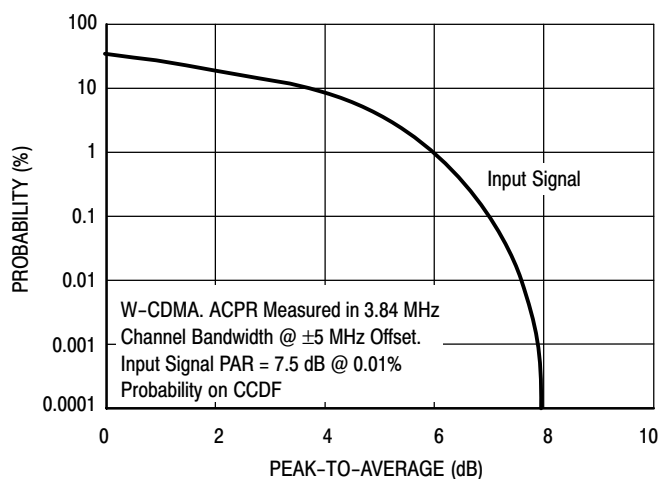


Figure 14. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

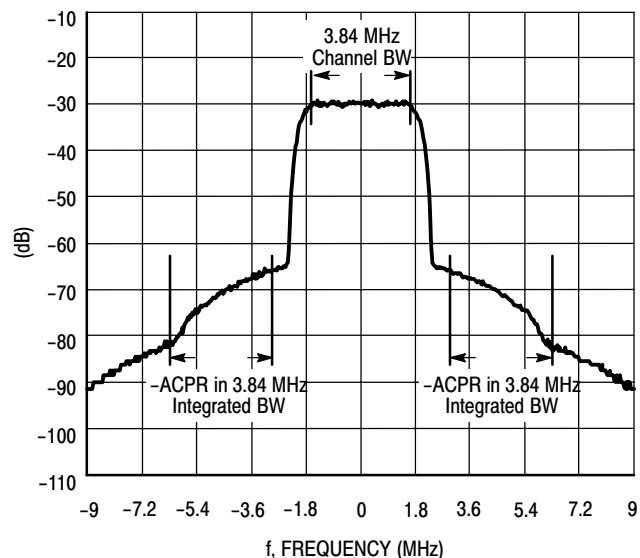
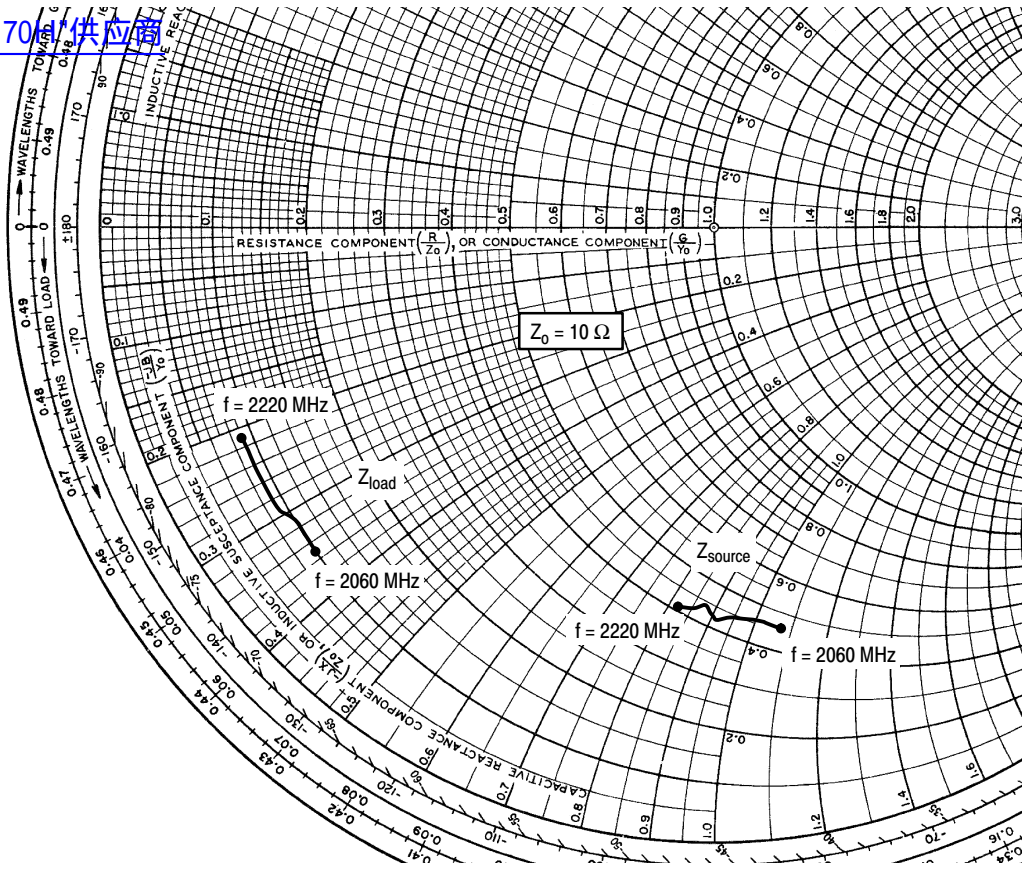


Figure 15. Single-Carrier W-CDMA Spectrum





$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1400 \text{ mA}$ ,  $P_{out} = 50 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2060	4.57 - j10.70	1.02 - j3.54
2080	4.57 - j10.38	0.99 - j3.34
2100	4.57 - j10.06	0.96 - j3.14
2120	4.52 - j9.72	0.93 - j2.94
2140	4.40 - j9.42	0.92 - j2.76
2160	4.15 - j9.12	0.91 - j2.59
2180	4.44 - j8.82	0.89 - j2.42
2200	4.19 - j8.53	0.88 - j2.25
2220	4.12 - j8.23	0.88 - j2.09

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

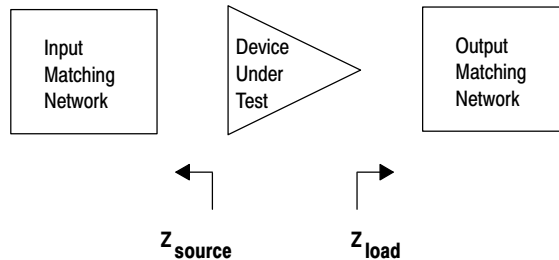
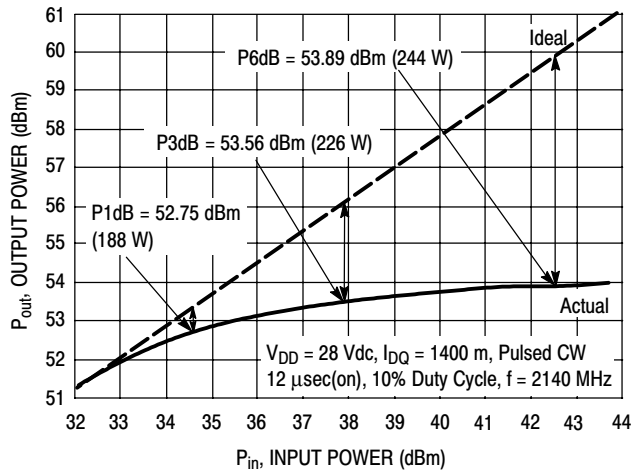


Figure 16. Series Equivalent Source and Load Impedance

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

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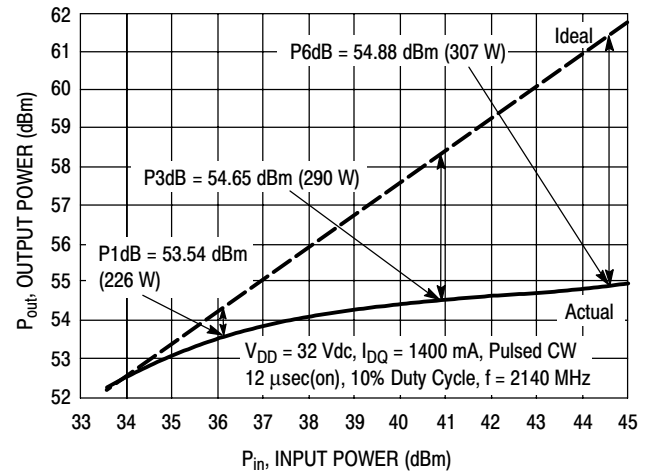


NOTE: Measured in a Peak Tuned Load Pull Fixture

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P3dB	4.43 - j11.85	0.81 - j2.87

Figure 17. Pulsed CW Output Power versus Input Power @ 28 V



NOTE: Measured in a Peak Tuned Load Pull Fixture

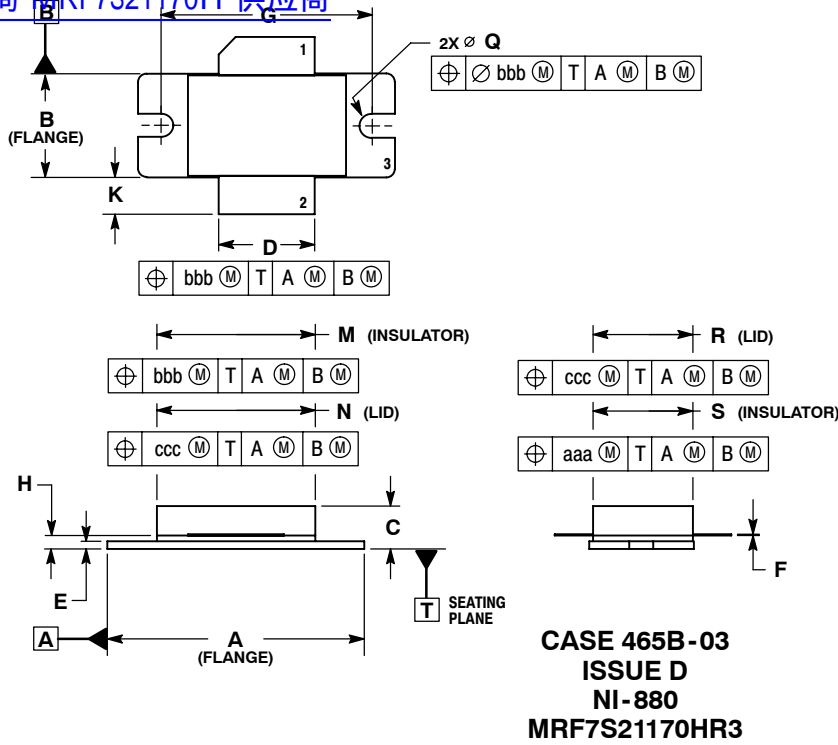
Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P3dB	4.43 - j11.85	0.72 - j2.87

Figure 18. Pulsed CW Output Power versus Input Power @ 32 V

## PACKAGE DIMENSIONS

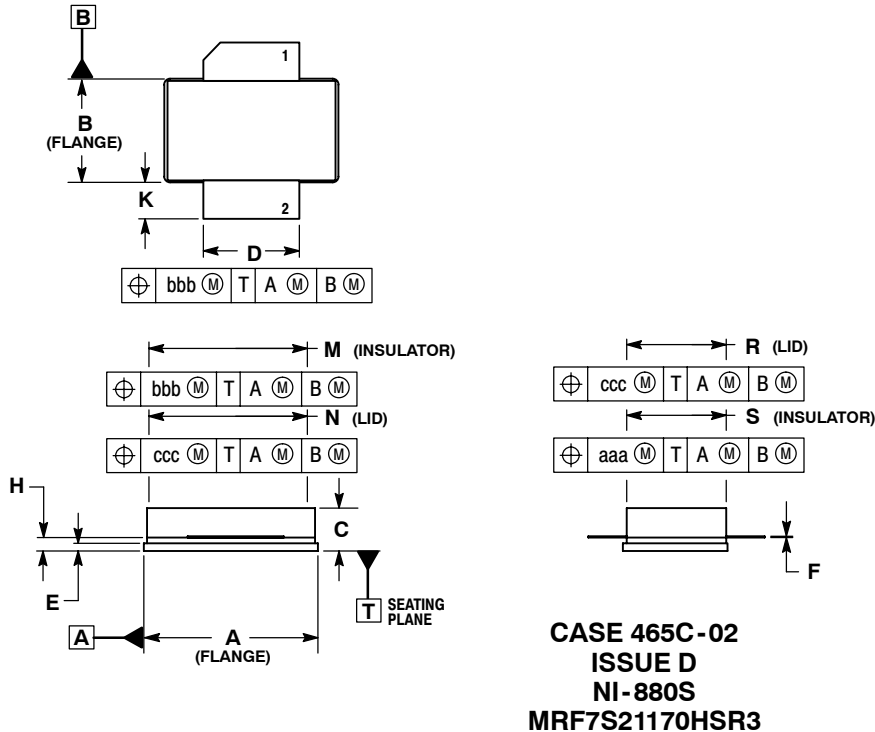
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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
  4. DELETED

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
PIN 1. DRAIN  
2. GATE  
3. SOURCE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
PIN 1. DRAIN  
2. GATE  
3. SOURCE

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2006	<ul style="list-style-type: none"> <li>Initial Release of Data Sheet</li> </ul>
1	June 2006	<ul style="list-style-type: none"> <li>Added Class C to description of parts, pg. 1</li> <li>Changeded “≥” to “-” in the Device Output Signal Par bullet, pg. 1</li> <li>Changed typ value from ±9 to 18 in Part-to-Part Phase Variation characteristic description in Table 4, Typical Performances, p. 2</li> <li>Expanded the characterization range in the MTTF Factor graph from 200°C to 230°C, Fig. 12, p. 7</li> </ul>
2	Aug. 2006	<ul style="list-style-type: none"> <li>Added Greater Negative Source bullet to Features section, p. 1</li> <li>Corrected Fig. 14, Single-Carrier W-CDMA Spectrum, to 3.84 MHz, p. 7</li> </ul>
3	Sept. 2006	<ul style="list-style-type: none"> <li>Changed “Capable of Handling” bullet from 10:1 VSWR @ 28 Vdc to 5:1 VSWR @ 32 Vdc, pg. 1</li> <li>Added “Insertion” to Part-to-Part Phase Variation characteristic description in Table 4, Typical Performances, p. 2</li> <li>Added Gain Flatness, Group Delay and Deviation from Linear Phase characteristics to Table 4, Typical Performances, p. 2</li> <li>Corrected Z6 value from “0.119” to “0.156”, corrected Z8 value from “0.156” to “0.119”, corrected Z9 value from “0.770” to “0.077”, corrected Z11 value from “0.076” to “0.760”, Fig. 1, Test Circuit Schematic, p. 3</li> <li>Added Part Number and Manufacturer for R1, R2 and R3 in Table 5, Test Circuit Component Designations and Values, p. 3</li> <li>Added Figure 10, Digital Predistortion Correction, p. 6</li> <li>Corrected Fig. 15, Single-Carrier W-CDMA Spectrum, to correctly reflect integrated bandwidth offsets, p. 7</li> <li>Added Figure 17, Pulsed CW Output Power versus Input Power @ 28 Vdc, p. 9</li> <li>Added Figure 18, Pulsed CW Output Power versus Input Power @ 32 Vdc, p. 9</li> </ul>
4	May 2007	<ul style="list-style-type: none"> <li>Removed “Designed for Digital Predistortion Error Correction Systems” bullet as functionality is standard, p. 1</li> <li>Added “Optimized for Doherty Applications” bullet to Features section, p. 1</li> <li>Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table and related “Continuous use at maximum temperature will affect MTTF” footnote added, p. 1</li> <li>Removed footnote and “Measured in Functional Test” from the RF test condition voltage callout for <math>V_{GS(Q)}</math>, and added Fixture Gate Quiescent Voltage, <math>V_{GG(Q)}</math> to On Characteristics table, p. 2</li> <li>Updated verbiage in Typical Performances table, p. 3</li> <li>Updated Part Numbers in Table 5, Component Designations and Values, to RoHS compliant part numbers and updated obsolete ATC600 series capacitors to ATC100 series, p. 4</li> <li>Adjusted scale for Fig. 8, Intermodulation Distortion Products versus Tone Spacing, to show wider dynamic range, p. 7</li> <li>Replaced Fig. 13, MTTF versus Junction Temperature with updated graph. Removed Amps<sup>2</sup> and listed operating characteristics and location of MTTF calculator for device, p. 8</li> <li>Fig. 14, CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal, updated to include output power level at functional test, p. 8</li> </ul>
5	Apr. 2008	<ul style="list-style-type: none"> <li>Corrected On Characteristics table <math>I_D</math> value for <math>V_{GS(th)}</math> from 270 <math>\mu</math>Adc to 372 <math>\mu</math>Adc and <math>V_{DS(on)}</math> from 2.7 Adc to 3.72 Adc; tightened <math>V_{GS(th)}</math> minimum and maximum values to match production test values, p. 2</li> <li>Updated Part Numbers in Table 5, Component Designations and Values, to latest RoHS compliant part numbers, p. 4</li> <li>Updated Fig. 14, CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal, to better represent production test signal, p. 8</li> </ul>

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