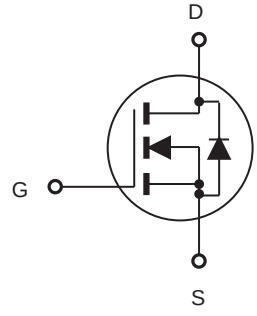
CEP04N7/CEB04N7
CEI04N7/CEF04N7

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

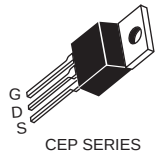
Type	V_{DSS}	$R_{DS(ON)}$	I_D	@V_{GS}
CEP04N7	700V	3.5Ω	4A	10V
CEB04N7	700V	3.5Ω	4A	10V
CEI04N7	700V	3.5Ω	4A	10V
CEF04N7	700V	3.5Ω	4A [d]	10V

- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.

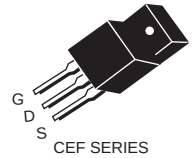


CEB SERIES
TO-263(DD-PAK)

CEI SERIES
TO-262(I2-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F

ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V_{DS}	700		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current-Continuous	I_D	4	4 [d]	A
Drain Current-Pulsed [a]	I_{DM} [e]	12	12 [d]	A
Maximum Power Dissipation @ T_C = 25°C	P_D	89	35	W
- Derate above 25°C		0.71	0.28	W/°C
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	3.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	65	°C/W

查询"CEF04N7"供应商

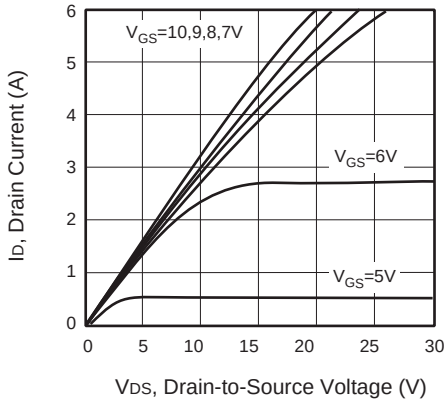


Figure 1. Output Characteristics

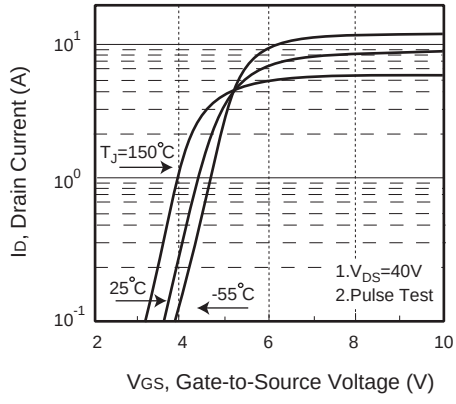


Figure 2. Transfer Characteristics

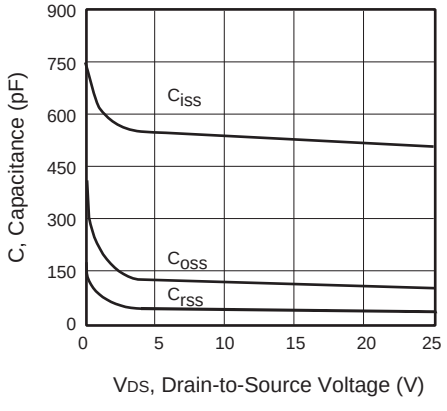


Figure 3. Capacitance

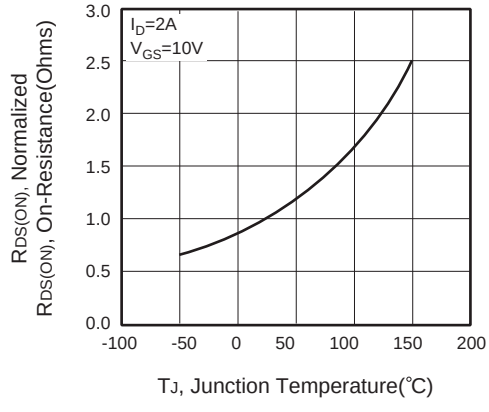


Figure 4. On-Resistance Variation with Temperature

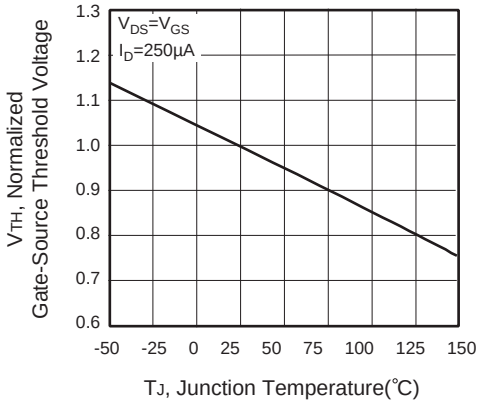


Figure 5. Gate Threshold Variation with Temperature

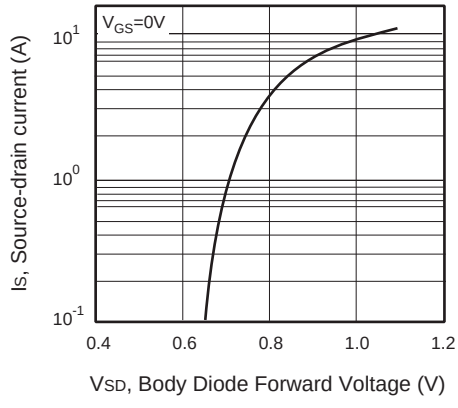


Figure 6. Body Diode Forward Voltage Variation with Source Current

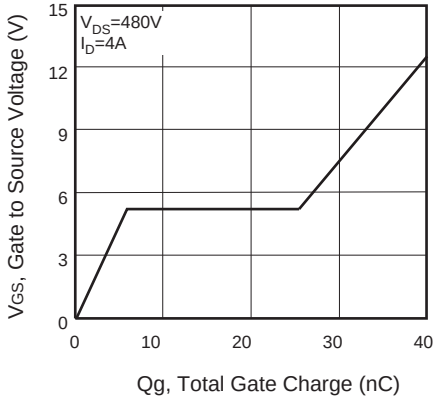


Figure 7. Gate Charge

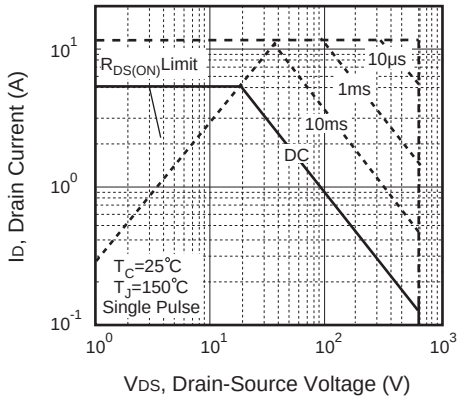


Figure 8. Maximum Safe Operating Area

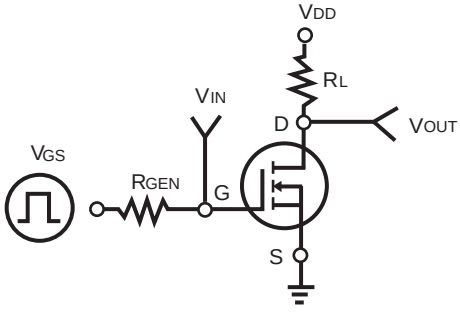


Figure 9. Switching Test Circuit

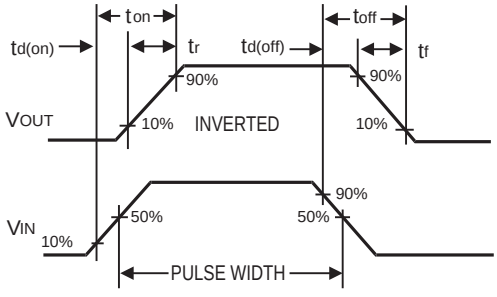


Figure 10. Switching Waveforms

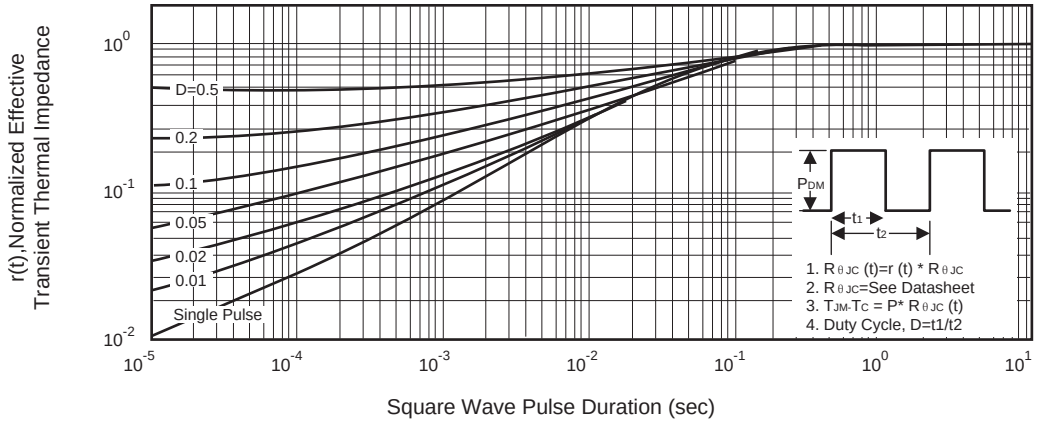


Figure 11. Normalized Thermal Transient Impedance Curve