NCP3101

Product Preview

Wide Input Voltage Synchronous Buck Converter

The NCP3101 is a high efficiency, wide input, high output current, synchronous PWM buck converter designed to operate from a 4.5 V to 13.2 V supply. The device is capable of producing an output voltage as low as 0.8 V. The NCP3101 can continuously output 6 A through MOSFET switches driven by an internally set 275 kHz oscillator. The 40−pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP3101 also incorporates an externally compensated transconductance error amplifier and a capacitor programmable soft−start function. Protection features include programmable short circuit protection and under voltage lockout (UVLO). The NCP3101 is available in a 40−pin QFN package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 275 kHz Internal Oscillator
- Greater than 90% Maximum Efficiency
- Boost Pin Operates to 25 V
- Voltage Mode PWM Control
- 0.8 V ±1% Internal Reference Voltage
- Adjustable Output Voltage by Resistor Divider
- Capacitor Programmable Soft−Start
- 80% Maximum Duty Cycle
- Input Undervoltage Lockout
- Resistor Programmable Current Limit
- This is a Pb−Free Device

Applications

- Servers/Networking
- DSP and FPGA Power Supply
- DC−DC Regulator Modules

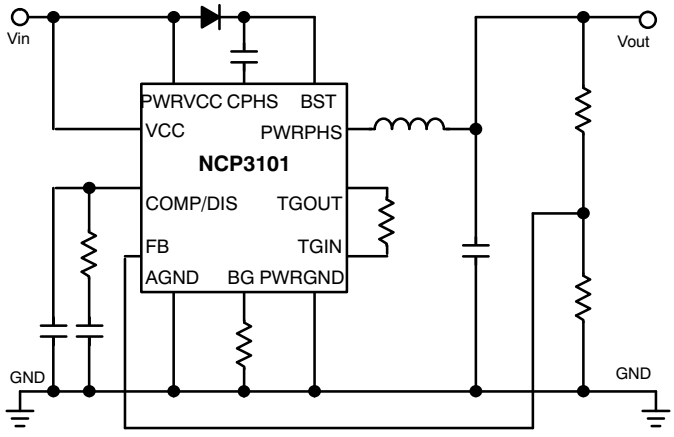

Figure 1. Typical Application Diagram

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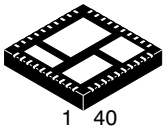
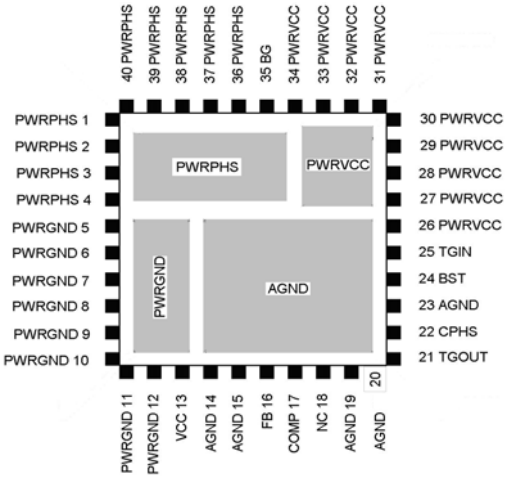


QFN40, 6x6
CASE 485AK

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

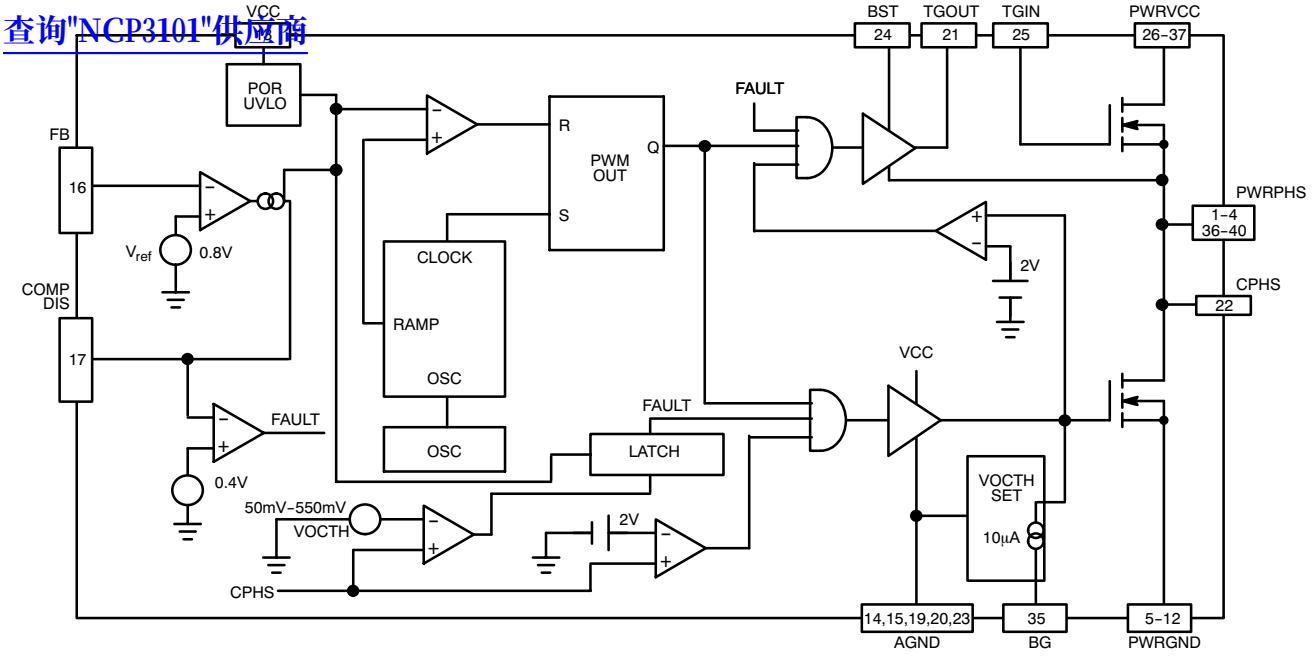


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No	Symbol	Description
1−4 , 36−40	PWRPHS	Power phase node. Drain of the low side power MOSFET and source of the high side MOSFET.
5−12	PWRGND	Power ground. Source of the low side power MOSFET. Connected with large copper area. High current return for the low side MOSFET.
13	V_{CC}	Supply for the internal driver. Decouple with a 0.1 μF − 1 μF capacitor to AGND as close to the IC as possible.
14,15,19,20,23	AGND	Internal driver ground. Reference ground for FB, COMP and other driver circuits.
16	FB	The input pin to the error amplifier.(inverted input error amplifier) Connect this pin to the output resistor divider (if used) or directly to the output voltage near the load connection.
17	COMP/DIS	Compensation or disable pin. (output error amplifier) Use this pin to compensate the voltage control feedback loop. The compensation capacitor also acts as a soft−start capacitor. Pulling the pin below 400 mV will disable the controller.
18	NC	No connect. This pin can be connected to AGND or not connected.
21	TGOUT	Output high side MOSFET driver. Connect to pin 25 with compensation circuit if used.
22	CPHS	The controller phase sensing.
24	BST	Supply rail for the floating top gate driver.
25	TGIN	Gate high side MOSFET
26−34	PWRVCC	Input supply pins for the high side MOSFET. (Drain)
35	BG	The current limit set pin.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Control Circuitry Input Voltage	V_{CC}	15 V	−0.3 V
Main Supply Voltage Input	PWRVCC	30 V	−0.3 V
Bootstrap Supply Voltage Input	BST	30 V wrt/GND 15 V wrt/PHASE	−0.3 V
Phase Node	PWRPHS	25 V	−0.7 V −5 V for < 50 nsec
Phase Node (Bootstrap Supply Return)	CPHS	25 V	−0.7 V −5 V for < 50 nsec
Current Limit Set	BG	15 V	−0.3 V −2.0 V for < 200 nsec
Feedback	FB	5.5 V	−0.3 V
COMP/DISABLE	COMP/DIS	5.5 V	−0.3 V

MAXIMUM RATINGS

Pin Name	Symbol	Value	Unit
Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	−40 to 150	°C
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Thermal Characteristics 6X6 QFN Plastic Package Maximum Power Dissipation @ T_A = 25°C	P_D	3000	mW
Lead Temperature Soldering (10 sec): Reflow (SMD Styles Only) Pb_Free (Note 1)		260 peak	°C
Moisture Sensitivity Level	MSL	3	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: These devices have limited built−in ESD protection. The devices should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the device.

1. 60−180 seconds minimum above 237°C

ELECTRICAL CHARACTERISTICS (0°C < T_J < 70°C for NCP3101, −40°C < T_J < 125°C for NCP3101B, 4.5 V < V_{CC} < 13.2 V, BST = V_{CC} * 2)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	–	4.5		13.2	V
Boost Voltage Range	–	4.5		30	V
Quiescent Supply Current	V_{FB} = 1.0 V , No Switching, V_{CC} = 13.2 V		2.3		mA
Quiescent Supply Current	V_{FB} = 1.0 V , No Switching, V_{CC} = 5 V		1.8		mA
V_{CC} Supply Current	V_{FB} = 1.0 V , Switching, V_{CC} = 13.2 V		10.3		mA
V_{CC} Supply Current	V_{FB} = 1.0 V , Switching, V_{CC} = 5 V		5.6		mA
Boost Quiescent Current	V_{FB} = 1.0 V , No Switching, V_{BST} = 25 V		600		μA
UVLO Threshold	V_{CC} Rising Edge	3.6	4.0		V
UVLO Hysteresis			0.4		V
V_{FB} Feedback Voltage	T_J = 0°C to 70°C	0.792	0.8	0.808	V
V_{FB} Feedback Voltage	T_J = −40°C to 125°C	0.788	0.8	0.812	V
Oscillator Frequency	T_J = 0°C to 70°C	250	275	300	kHz
Oscillator Frequency	T_J = −40°C to 125°C	233	275	317	kHz
Minimum Duty Cycle			4		%
Maximum Duty Cycle		70	75	80	%
Blanking Time			50		ns
Transconductance			4.0		mS
Open Loop DC Gain	Guaranteed by Design	55	70		dB
Output Source Current	V_{FB} = 100 mV	80	120		μA
Output Sink Current	V_{FB} = 100 mV	80	120		μA
Input Bias Current			0.1	1.0	μA
Unity Gain Bandwidth			4.0		MHz
Soft−Start Source Current	V_{FB} = 0.8 V		10		μA
Transient Response*	Undershot V_{OUT} Recovery Time		112 118		mV μs
OVERCURRENT PROTECTION					
OC Threshold	R_{BG} = 5 kΩ	25	50	75	mV
Fixed OC Threshold		–	−375	–	mV
OCSET Current Source	Sourced from BG Pin before Soft−Start		10		μA
OC Switch−Over Threshold			700		mV
OUTPUT POWER MOSFETS					
$R_{DS(on)}$ Low−Side	V = 13.2 V I_D = 6 A		18		mΩ
$R_{DS(on)}$ High−Side	V = 13.2 V I_D = 6 A		18		mΩ

*Transient response with 2.5 A/μs load step 50% − 100% defined at output parts: C_{OUT}= 2x100 uF MLCC + 0.82 mF OS−CON.

TYPICAL OPERATING CHARACTERISTICS

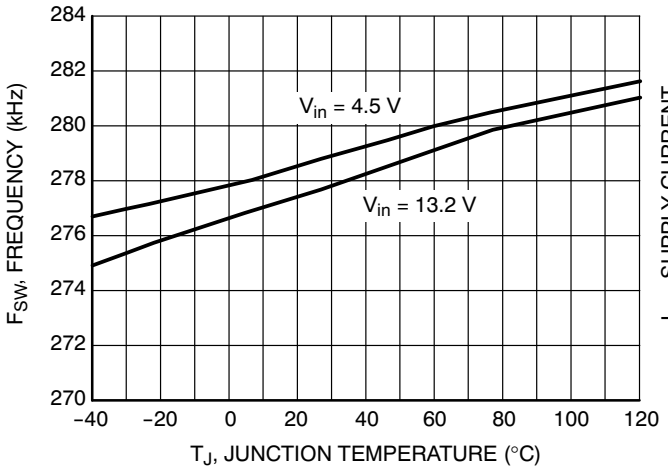


Figure 3. Oscillator Frequency (F_{SW}) vs. Temperature

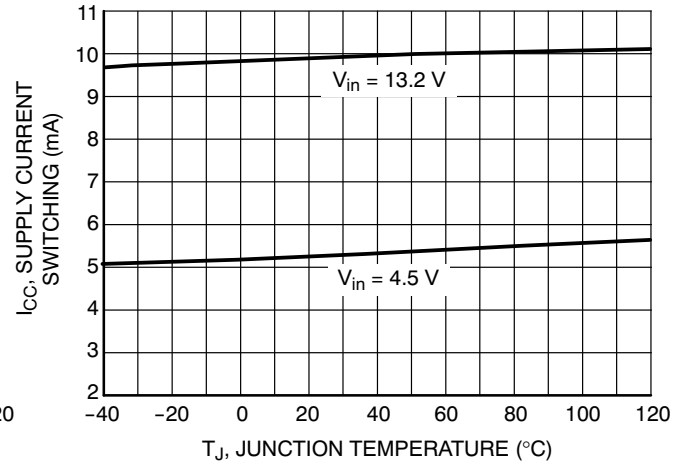


Figure 4. I_{CC} vs. Temperature

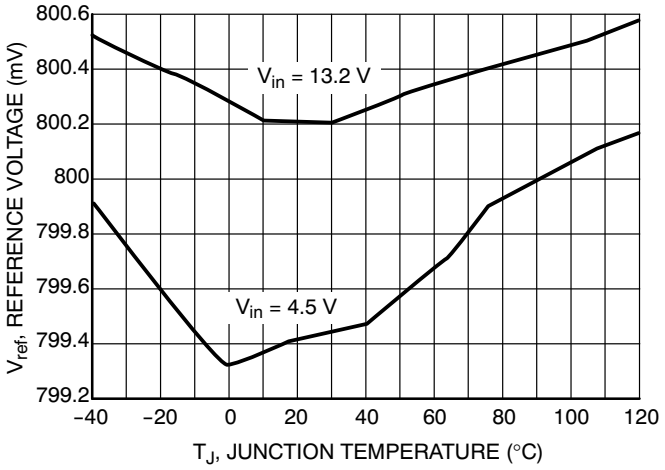


Figure 5. Reference Voltage (V_{ref}) vs. Temperature

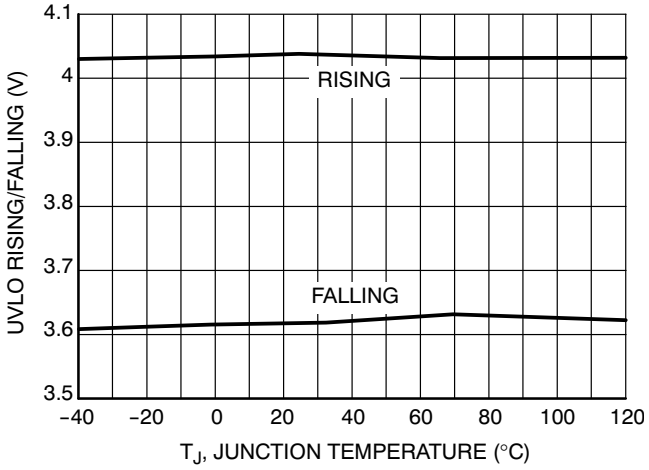


Figure 6. UVLO vs. Temperature

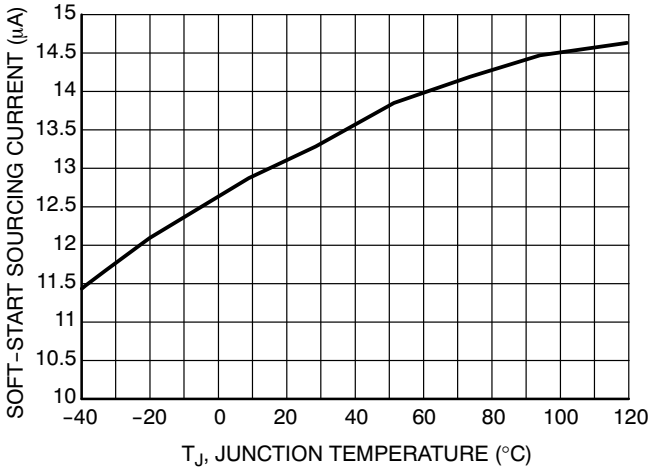


Figure 7. Soft−Start Sourcing Current vs. Temperature

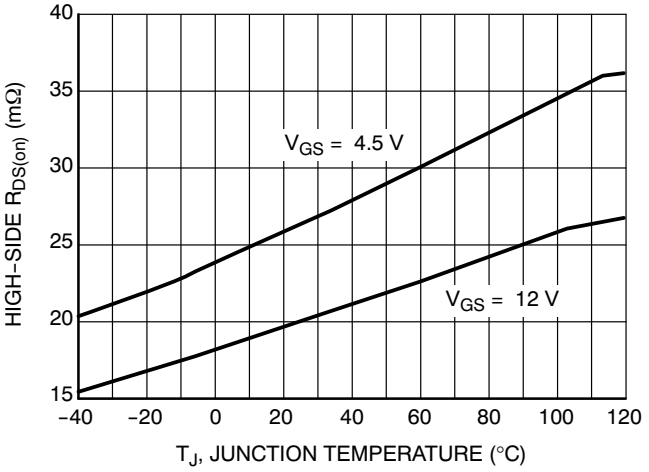


Figure 8. High−Side $R_{DS(on)}$ vs. Temperature

DETAILED OPERATING DESCRIPTION

General

NCP3101 is a high efficiency integrated wide input voltage 6 A synchronous PWM buck converter designed to operate from a 4.5 V to 13.2 V supply. The output voltage of the converter can be precisely regulated down to 800 mV ±1.0% when the V_{FB} pin is tied to V_{OUT}. The switching frequency is internally set to 275 kHz. A high gain Operational Transconductance Error Amplifier (OTA) is used for feedback and stabilizing the loop.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The NCP3101 can achieve an 80% duty cycle. There is a built in off−time which ensures that the bootstrap supply is charged every cycle. The NCP3101, which is capable of a 100 nsec pulse width (minimum), can allow a 12 V to 0.8 V conversion at 275 kHz. The duty cycle limit and the corresponding output voltage are shown below in graphical format in Figure 9 and 11. The light gray area represents the safe operating area for the lowest maximum operational duty cycle and the dark grey area represents the absolute maximum duty cycle and corresponding output voltage.

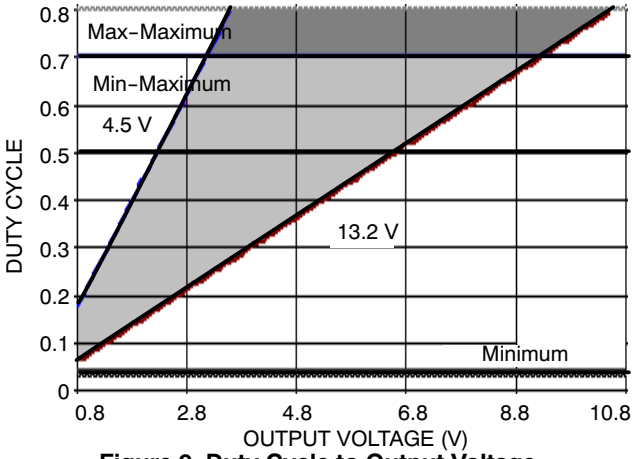


Figure 9. Duty Cycle to Output Voltage

Input Voltage Range (V_{CC} and BST)

The input voltage range for both V_{CC} and BST is 4.5 V to 13.2 V with reference to GND and PHS, respectively. Although BST is rated at 13.2 V with reference to PHS, it can also tolerate 25 V with respect to GND.

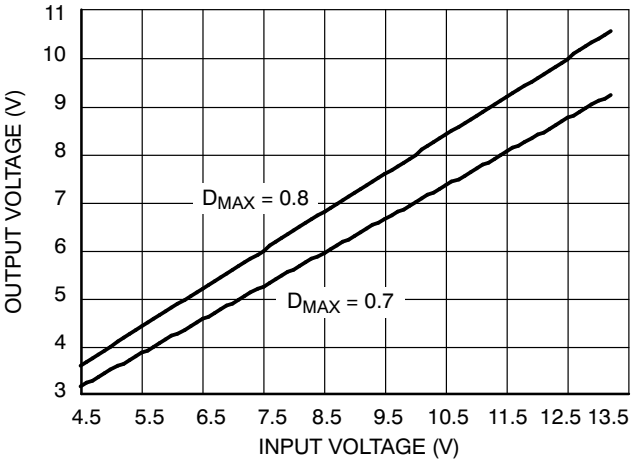


Figure 10. Maximum Input to Output Voltage

External Enable/Disable

When the Comp Pin voltage falls or is pulled externally below the 400 mV threshold as shown in Figure 11, it disables the PWM Logic and the gate drive outputs. In this disabled mode, the operational transconductance amplifier's (EOTA) output source current is reduced and limited to the Soft−Start mode of 10 μA.

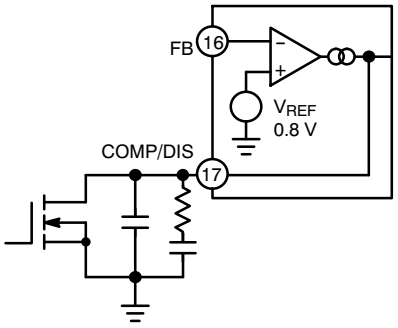


Figure 11. Disable Circuit

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal soft−start, SS, is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

External Soft−Start

The NCP3101 features an external soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−Start is achieved by using the internal current source of 10 μA (typ) which charges the external integrator capacitor of the transconductance amplifier. Figure 12 is a typical soft−start sequence. This sequence begins once V_{CC} surpasses its UVLO threshold. During soft−start, as the Comp Pin rises through 400 mV, the PWM Logic and gate drives are enabled. When the feedback voltage crosses 800 mV, the EOTA will be given control to switch to its higher regulation mode output current of 120 μA. In the event of an over current during the soft−start, the overcurrent logic will override the soft−start sequence and will shut down the PWM logic and both the high side and low side gates of the switching MOSFETS.

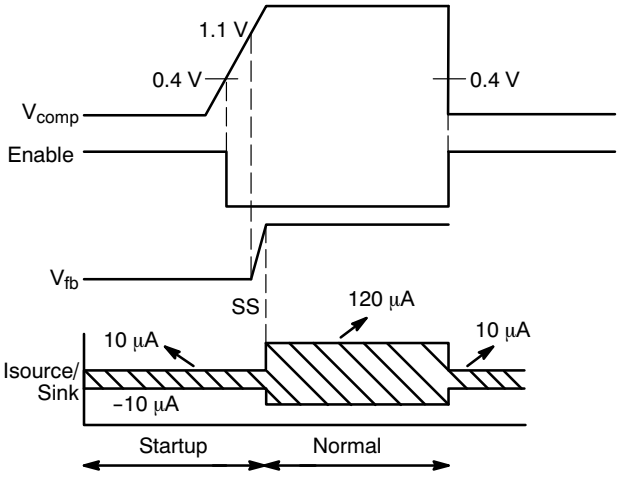


Figure 12. Soft−Start Implementation

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP3101, the UVLO is set to ensure that the IC will startup when V_{CC} reaches 4.0 V and shutdown when V_{CC} drops below 3.6 V. This permits smooth operation from a varying 5.0 V input source.

Current Limit Protection

In case of a short circuit or overload, the low side LS−FET will conduct large currents. The controller will shut down the regulator in this situation for protection against overcurrent. The low side $R_{DS(on)}$ sense is implemented by comparing the voltage at the phase node when BG starts going low to an internally generated fixed voltage. If the phase voltage is lower than OC trip voltage, an overcurrent condition occurs and a counter is initiated. When the counter completes, the PWM logic and both HS−FET and LS−FET are turned off. The converter will reinitialize through the soft−start cycle to determine if the short circuit or overload condition has been removed. The minimum turn−on time of the LS−FET is set to 500 ns. The trip thresholds have a −95 mV, +45 mV process and temperature variation when set to −375 mV. The operation of key nodes is displayed in Figure 13 for both normal operation and during over current conditions.

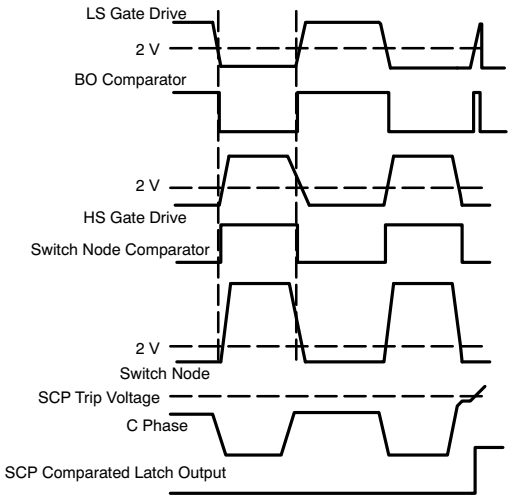


Figure 13. Switching and Current Limit Timing

Overcurrent Protection Setting

NCP3101 allows the setting of Overcurrent Threshold ranging from 50 mV to 550 mV, simply by adding a resistor (ROCSET) between BG and GND. During a short period of time following V_{CC} rising over UVLO threshold, an internal 10 μA current (IOCSET) is sourced from BG Pin, determining a voltage drop across ROCSET. This voltage drop will be sampled and internally held by the device as Overcurrent Threshold. The OC setting procedure overall time length is approximately 6 ms. When a ROCSET resistor is connected between BG and GND, the programmed threshold is set with an RSET values range from 5 kΩ to 45 kΩ.

$$IOCth = \frac{IOCSET * ROCSET}{R_{DS(on)}} \qquad \text{(eq. 1)}$$

In case ROCSET is not connected, the device switches the OCP threshold to a fixed 375 mV value: an internal safety clamp on BG is triggered as soon as BG voltage reaches 700 mV, enabling the 375 mV fixed threshold and ending OC setting phase.

Drivers

The NCP3101 drives the internal High and Low side Switching MOSFETS with 1 A gate drivers. The gate drivers also include adaptive nonoverlap circuitry. The nonoverlap circuitry increase efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

A detailed block diagram of the nonoverlap and gate drive circuitry used in the chip is shown in Figure 14.

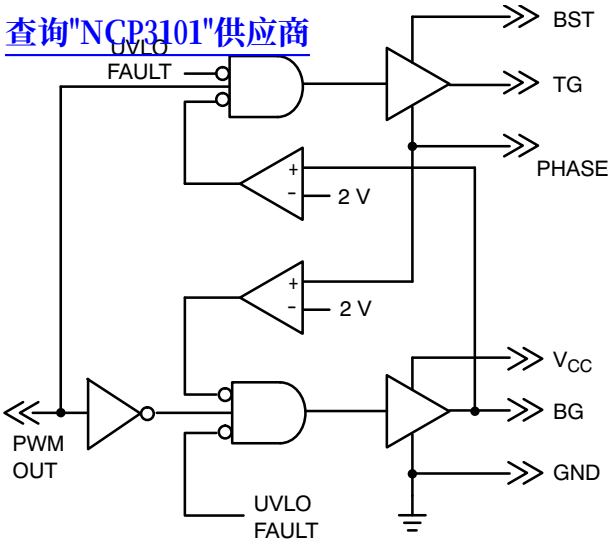


Figure 14. Block Diagram

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and PHASE must be placed as close as possible to the IC. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

APPLICATION SECTION

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$Iin_{RMS} = I_{OUT}\sqrt{D \times (1 - D)} \qquad \text{(eq. 2)}$$

Where D is the duty cycle, Iin_{RMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times Iin_{RMS}^{2} \qquad \text{(eq. 3)}$$

Where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum capacitor must be used, it must be surge protected. Otherwise, capacitor failure could occur.

Calculating Input Startup current

To calculate the input startup current, the following equation can be used:

$$I_{inrush} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}} \qquad \text{(eq. 4)}$$

where I_{inrush} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the soft−start interval.

If the inrush current is higher than the steady state input current during maximum load, then the input fuse should be rated accordingly, if one is used.

Calculating Soft−Start Time

To calculate the soft−start time, the following equation can be used.

$$t_{SS} = \frac{\left(C_p + C_c\right) * \Delta V}{I_{SS}} \qquad \text{(eq. 5)}$$

Where C_C is the compensation as well as the soft−start capacitor.

C_P is the additional capacitor that forms the second pole.

I_{SS} is the soft−start current

ΔV is the comp voltage from zero to until it reaches regulation.

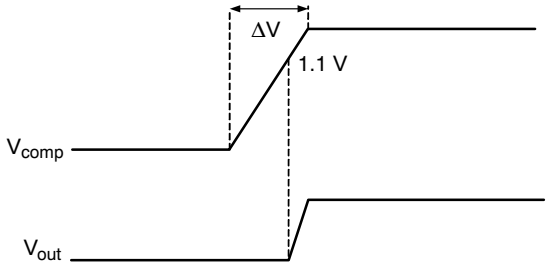


Figure 15. Soft−Start

The above calculation includes the delay from comp rising to when output voltage becomes valid.

To calculate the time of output voltage rising to when it reaches regulation; ΔV is the difference between the comp voltage reaching regulation and 1.1 V.

Output Capacitor Selection

Selection of the right value of input and output capacitors determines the behavior of the buck converter. In most high power density applications the capacitor size is most important. Ceramic capacitor is necessary to reduce the high frequency ripple voltage at the input of converter. This capacitor should be located as near the IC as possible. Added electrolytic capacitor improved response of relative slow load change.

The required output capacitor will be determined by planned transient deviation requirements. Usually a combination of two types of capacitors is recommended to meet the requirements. First, a ceramic output capacitor is needed for bypassing high frequency noise. Second, an electrolytic output capacitor is needed to achieve good transient response.

In fact, during load transient, for the first few microseconds the bulk capacitance supplies current to the

load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initially drops due to the current variation inside the capacitor and the ESR. (neglecting the effect of the effective series inductance (ESL)):

$$\Delta V_{OUT-ESR} = \Delta I_{out} \times ESR_{COUT} \quad \text{(eq. 6)}$$

where $V_{OUT-ESR}$ is the voltage deviation of V_{OUT} due to the effects of ESR and the ESR_{COUT} is the total effective series resistance of the output capacitors.

Table 1 shows values of voltage drop and recovery time of the NCP3101 demo board with the configuration shown in Figure 19. The transient response was measured for the load current step from 3 A to 6 A (50% to 100% load).

Input capacitors are 2x47 µF ceramic and 1x270 µF OS−CON, output capacitors are 2x100 µF ceramic and OS−CON as mentioned in Table 1. Typical transient response waveforms are shown in Figure 16.

More information about OS−CON capacitors is available at http://www.edc.sanyo.com.

Table 1. TRANSIENT RESPONSE VERSUS OUTPUT CAPACITANCE (50% to 100% Load Step)

C_{OUT} (µF) OS−CON	Drop (mV)	Recovery Time (µs)
0	384	336
100	224	298
150	192	278
220	164	238
270	156	212
560	128	198
820	112	118
1000	112	116

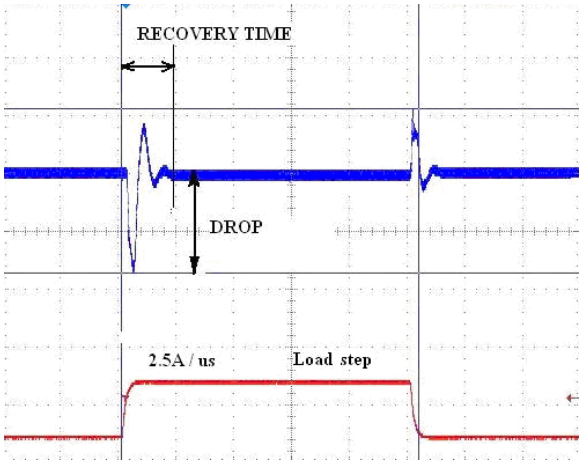


Figure 16. Typical Waveform of Transient Response

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DISCHARGE} = \frac{\Delta I_{OUT}{}^2 \times L_{OUT}}{2 \times C_{OUT} \times (V_{IN} \times D - V_{OUT})} \quad \text{(eq. 7)}$$

where $V_{OUT-DISCHARGE}$ is the voltage deviation of V_{OUT} due to the effects of discharge, L_{OUT} is the output inductor value and V_{IN} is the input voltage.

Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by:

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \quad \text{(eq. 8)}$$

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak−to−peak ripple current is given by the following equation:

$$Ipk\text{-}pk_{LOUT} = \frac{V_{OUT}(1 - D)}{L_{OUT} \times 275\ kHz} \quad \text{(eq. 9)}$$

where $Ipk\text{-}pk_{LOUT}$ is the peak to peak current of the output. From this equation it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current. In order to achieve high efficiency, coils with a low value of Direct Current Resistance (DCR) have to be used.

Feedback and Compensation

The output voltage is adjustable from 0.8 V to 5 V as shown in Table 1. The adjustment method requires an external resistor divider with its center tap tied to the FB pin. It is recommended to have a resistance between 1.5 kΩ and 5 kΩ. The selection of low value resistors reduces efficiency, alternatively high value resistance of R2 causes decrease in output voltage accuracy due to the bias current in the error amplifier. The output voltage error of this bias current can be estimated by using the following equation:

$$Error(\%) = \frac{R2 * I_{bias}}{V_{REF}} * 100 \quad \text{(eq. 10)}$$

Error = R2 * 1.25 * 10^{-5} (%)

Once R2 is calculated above R3 can be calculated to select the desired output voltage as shown in the following equation:

$$R3 = \frac{V_{REF}}{V_{OUT} - V_{REF}} * R2 \quad \text{(eq. 11)}$$

Table 1 shows R3 values for frequently used output voltages.

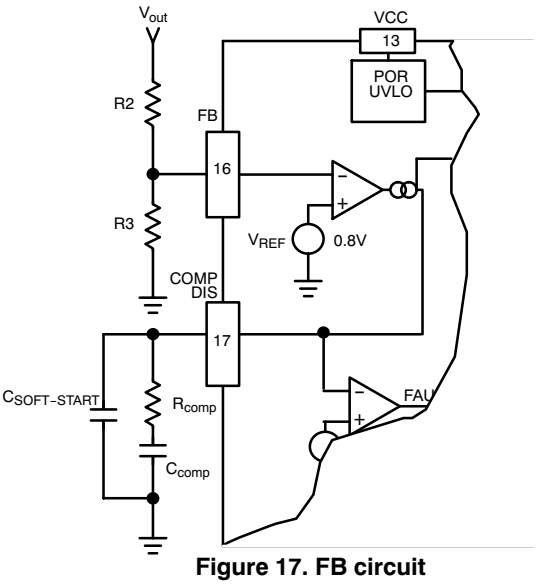


Figure 17. FB circuit

Table 1. OUTPUT VOLTAGES AND DIVIDER RESISTORS

V_{OUT} (V)	R2 (kΩ)	R3 (kΩ) E24	R3 (kΩ) Calculated
0.8	1.8	None	None
1.0	0.51	2.0	2.040
1.2	0.75	1.5	1.500
1.5	1.3	1.5	1.486
1.8	1.6	1.3	1.280
2.5	1.6	0.75	0.753
3.3	1.6	0.51	0.512
5.0	2.7	0.51	0.514

Figure 17 shows a typical Type II operational transconductance error amplifier (OTA). The compensation network consists of the internal error amplifier and the impedance networks ZIN (R1, R2) and external ZFB (R_{comp}, C_{comp} and $C_{soft-start}$). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response (but always lower than $f_{SW}/8$) and the highest gain in DC conditions to minimize the load regulation. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst−case component variations when determining phase margin. Loop stability is defined by the compensation network around the OTA, the output capacitor, output inductor and the output divider. Figure 18 shows the open loop and closed loop gain plots.

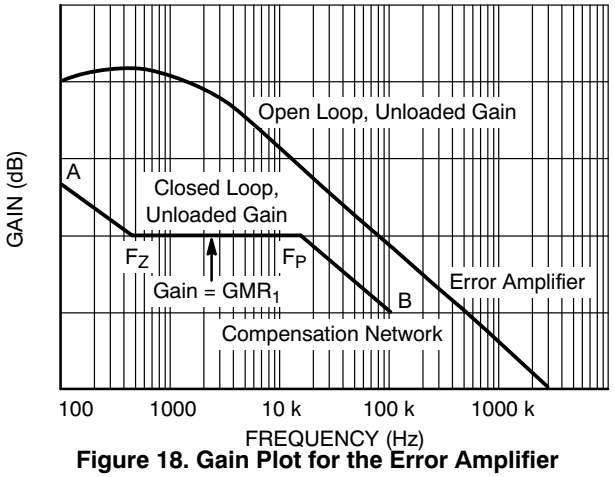


Figure 18. Gain Plot for the Error Amplifier

Thermal Considerations

The package thermal resistance can be obtained from the specifications section of this data sheet and a calculation can be made to determine the NCP3101 junction temperature. However, it should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the NCP3101, impact the temperature of the device. The PCB is used also as the heatsink. Double or multi layer PCBs with thermal vias between places with the same electrical potential increase cooling area. A 70 μm thick copper plating is a good solution to eliminate the need for an external heatsink.

Layout Considerations

When designing a high frequency switching converter, layout is very important. Using a good layout can solve many problems associated with these types of power supplies as transient occur.

External compensation components (R1, C9) are needed for converter stability. They should be placed close to the NCP3101. The feedback trace is recommended to be kept as far from the inductor and noisy power traces as possible. The resistor divider and feedback acceleration circuit (R2, R3, R6, C13) is recommended to be placed near to input FB (Pin 16, NCP3101).

Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located together as close as possible using ground plane construction or single point grounding. The inductor and output capacitors should be located together as close as possible to the NCP3101.

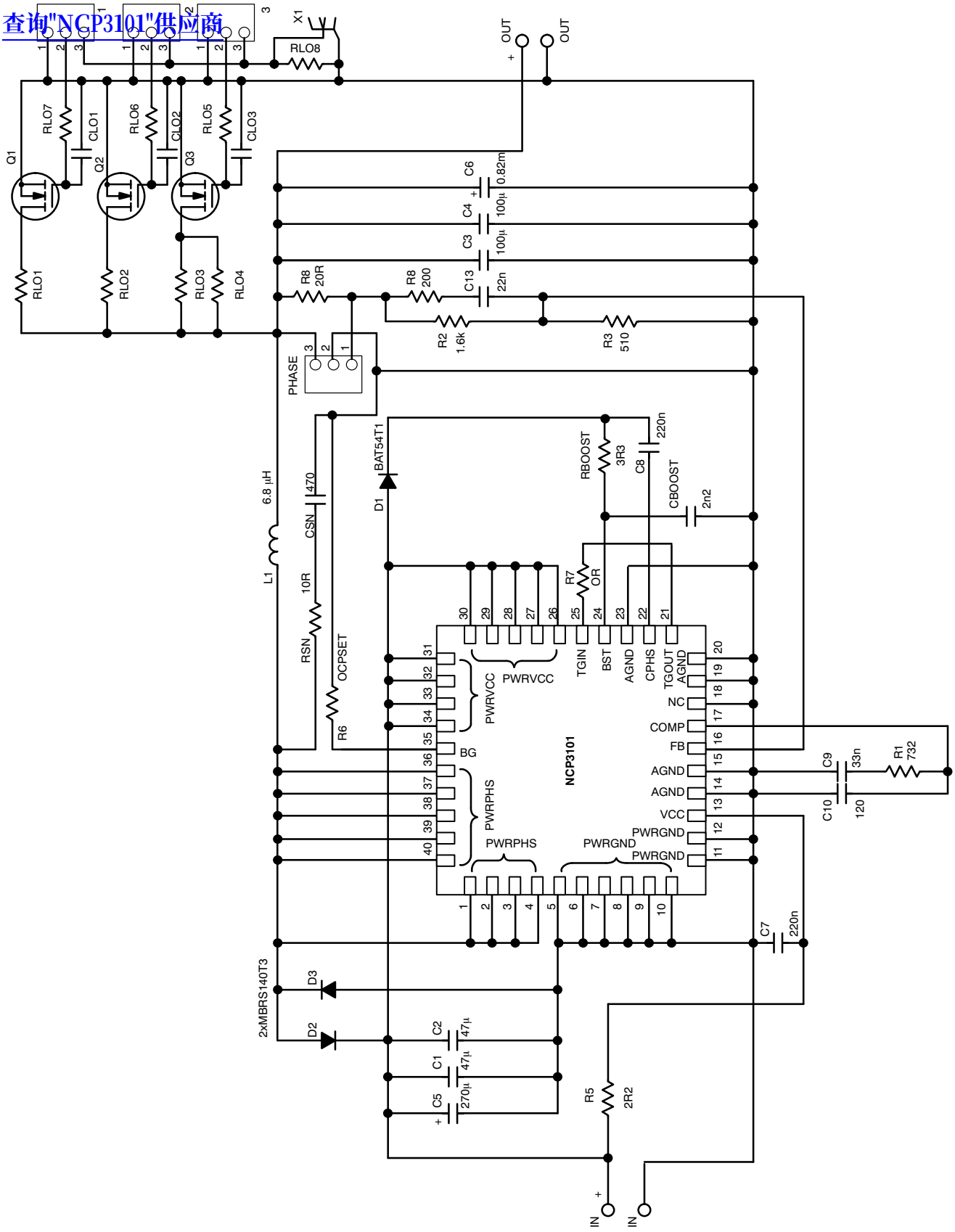


Figure 19. Schematic Diagram of NCP3101 Evaluation Board

Schematic diagram of the NCP3101 demoboard is shown in Figure 19 and the actual PCB layout is shown in Figure 20. The corresponding bill of material is summarized in Table 2. Parameters of the board were tested with Input voltage V_{in} = 4.5 V to 13.2 V and with various output loads between 0 A and 6 A. The board includes a few components used for transient measurements. The load current range can be selected by switches 1 to 3 to give a range of 0 A – 6 A with 2 A steps. A square wave signal with a 10% duty cycle and a 10 V amplitude has to be connected to the X1 connector to enable the load testing.

Table 2. BILL OF MATERIAL

Position	Value	Description	Part No:	Footprint	Quantity	Manufacturer
R1	732 Ω	Resist. SMD	RMC1/8W 1206 1% 732R	1206	1	MULTICOMP
R2	1.6 kΩ	Resist. SMD	RMC1/8W 1206 1% 1K6	1206	1	MULTICOMP
R3	510 Ω	Resist. SMD	RMC1/8W 1206 1% 510R	1206	1	MULTICOMP
R4	200 Ω	Resist. SMD	WCR 1206 200R 2%.	1206	1	WELWYN
R5	2.2 Ω	Resist. SMD	232272462208	1206	1	PHYCOMP
R6	OCP set.	Resist. SMD		1206	1	
R7	0 Ω	Resist. SMD	TL2BR010FTE	1206	1	TYCO ELECT.
R8*	20 Ω	Resist. SMD	232272462208	1206	1	PHYCOMP
RSN	10 Ω	Resist. SMD	232271161109	1206	1	PHYCOMP
RBOOST	3.3 Ω	Resist. SMD	232273463308	1206	1	PHYCOMP
RLO1*	2.2 Ω	Resistor 1W	MCF 1W 2R2	Special	1	MULTICOMP
RLO2*	2.2 Ω	Resistor 1W	MCF 1W 2R2	Special	1	MULTICOMP
RLO3*	2.2 Ω	Resistor 1W	MCF 1W 2R2	Special	1	MULTICOMP
RLO4*	2.2 Ω	Resistor 1W	MCF 1W 2R2	Special	1	MULTICOMP
RLO5*	1 kΩ	Resist. SMD	232272461002	1206	1	PHYCOMP
RLO6*	1 kΩ	Resist. SMD	232272461002	1206	1	PHYCOMP
RLO7*	1 kΩ	Resist. SMD	232272461002	1206	1	PHYCOMP
RLO8*	75 Ω	Resist. SMD	RMC1/8W 1206 1% 75R	1206	1	MULTICOMP
C1−C2	47 μF	Capac. Ceram	C1210C476M9PAC7800	1210	2	KEMET
C3−C4	100 μF	Capac. Ceram	CS1210C107M9PAC7800	1210	2	KEMET
C5	0.27 mF	Cap.OS−CON	16SP270M	Special	1	SANYO
C6	0.82 mF	Cap.OS−CON	4SP820M	Special	1	SANYO
C7	220 nF	Capac. Ceram	12065G224ZAT2A	1206	1	AVX
C8	220 nF	Capac. Ceram	12065G224ZAT2A	1206	1	AVX
C9	33 nF	Capac. Ceram	B37872K5333K−MR	1206	1	TYCO ELECT.
C10	120 pF	Capac. Ceram	2250 001 11537	1206	1	PHYCOMP
C13	22 nF	Capac. Ceram	2238 581 15641	1206	1	PHYCOMP
CSN	470 pF	Capac. Ceram	12067A471JAT1A	1206	1	AVX
CS	470 pF	Capac. Ceram	12067A471JAT1A	1206	1	AVX
CBOOST	2.2 nF	Capac. Ceram	12067C222KAT2A	1206	1	AVX
CLO1−3*	4.7 nF	Capac. Ceram	12065C472KAT2A	1206	3	AVX
D1	BAT51T1	Diode	BAT51T1G	SOD123	1	ON Semiconductor
D2−3	MBRS140T3	Diode	MBRS140T3G	SMB	2	ON Semiconductor
L1	6.8 μH	Coil	74457068	WE−PD4	1	Wurth Electronik
Q1−3*	NTD4810	MOSFET	NTD4810NH	DPAK	3	ON Semiconductor
IC1	NCP3101	I.C.	NCP3101MNTXG	QFN40	1	ON Semiconductor

Parts marked with “” and highlighted in grey are only necessary for transient response and PHASE−GAIN feedback measuring.

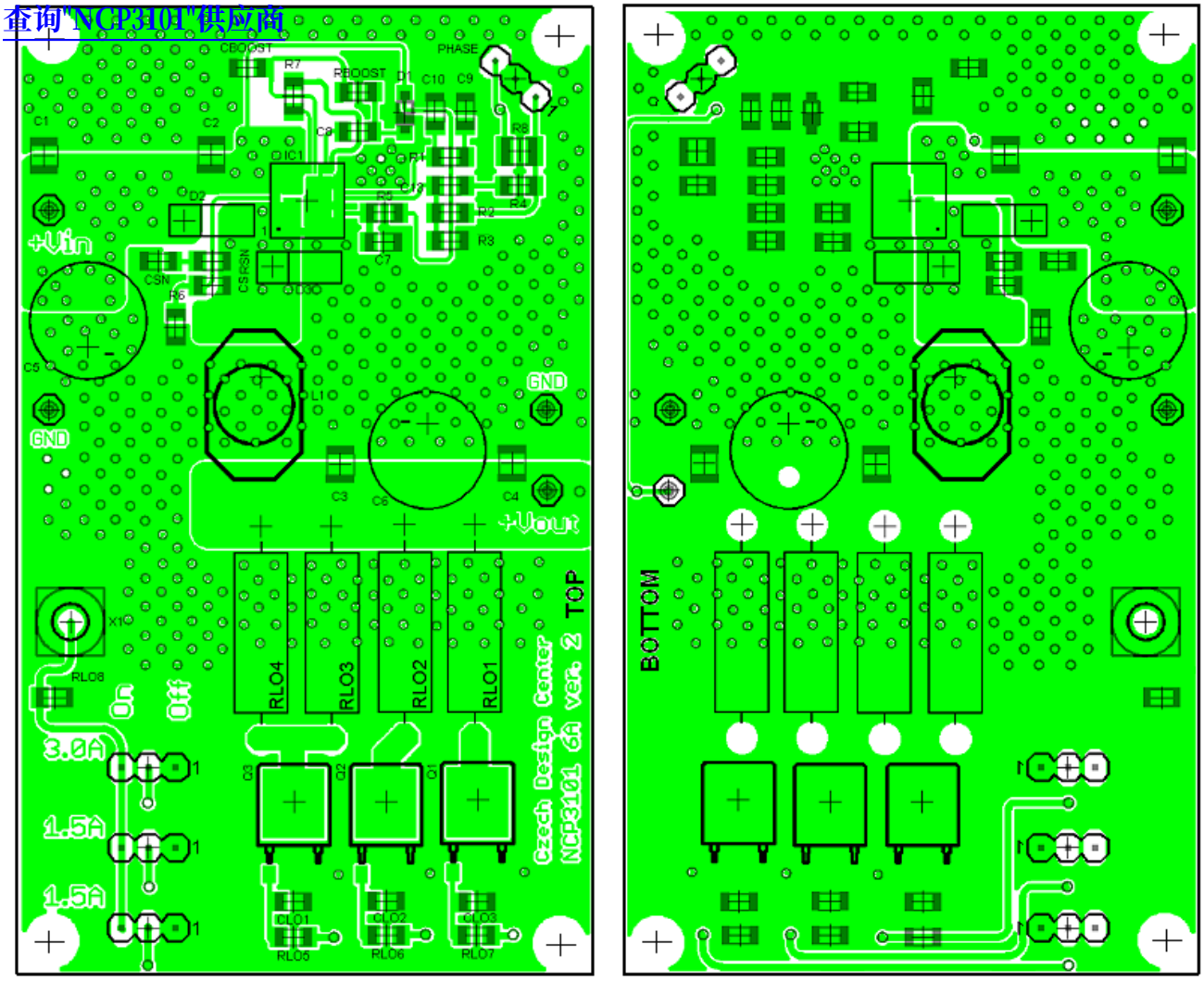


Figure 20. PCB Layout Evaluation Board (55mm x 90mm)

Measured Performance of NCP3101 Demoboard is Shown in Figures 21 Through 24.

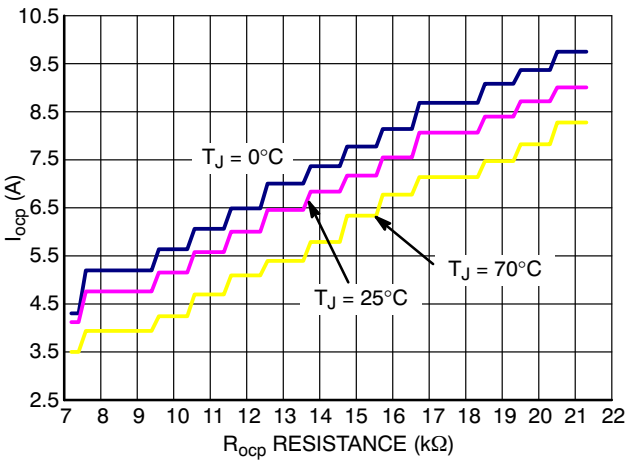


Figure 21. Overcurrent Protection

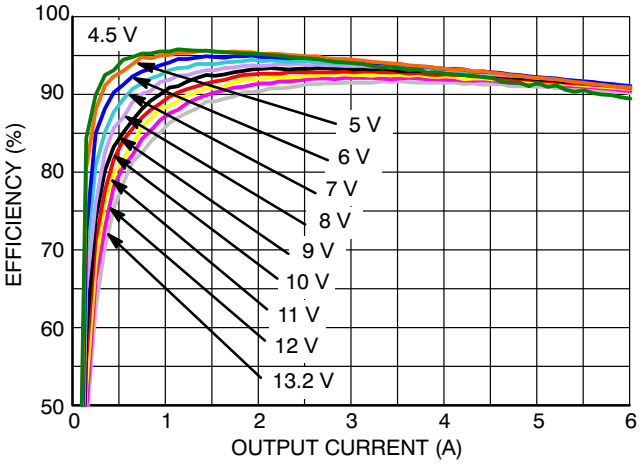


Figure 22. Efficiency (V_{out} = 3.3 V)

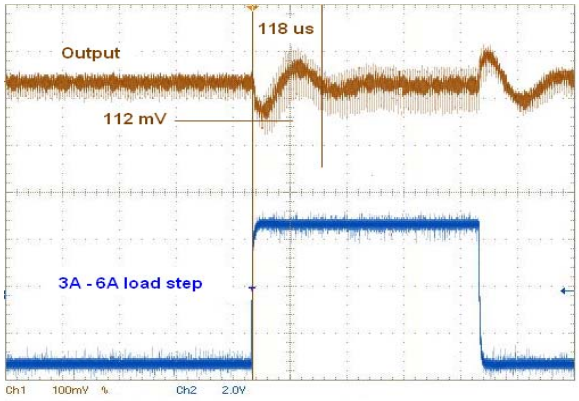


Figure 23. Transient Response (V_{in} = 13.2 V, V_{out} = 3.3 V, I_{out} = 3 A to 6 A Step) Output Capacitors: 2x MLCC 100 μF and 820 μF OS−CON

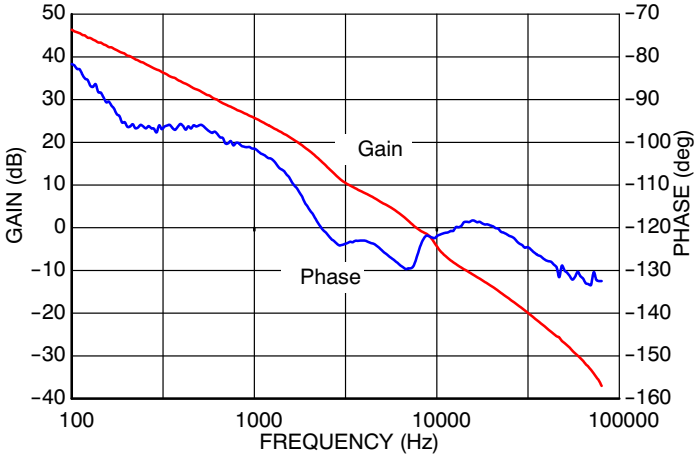


Figure 24. Feedback Frequency Response (V_{in} = 13.2 V, V_{out} = 3.3 V)

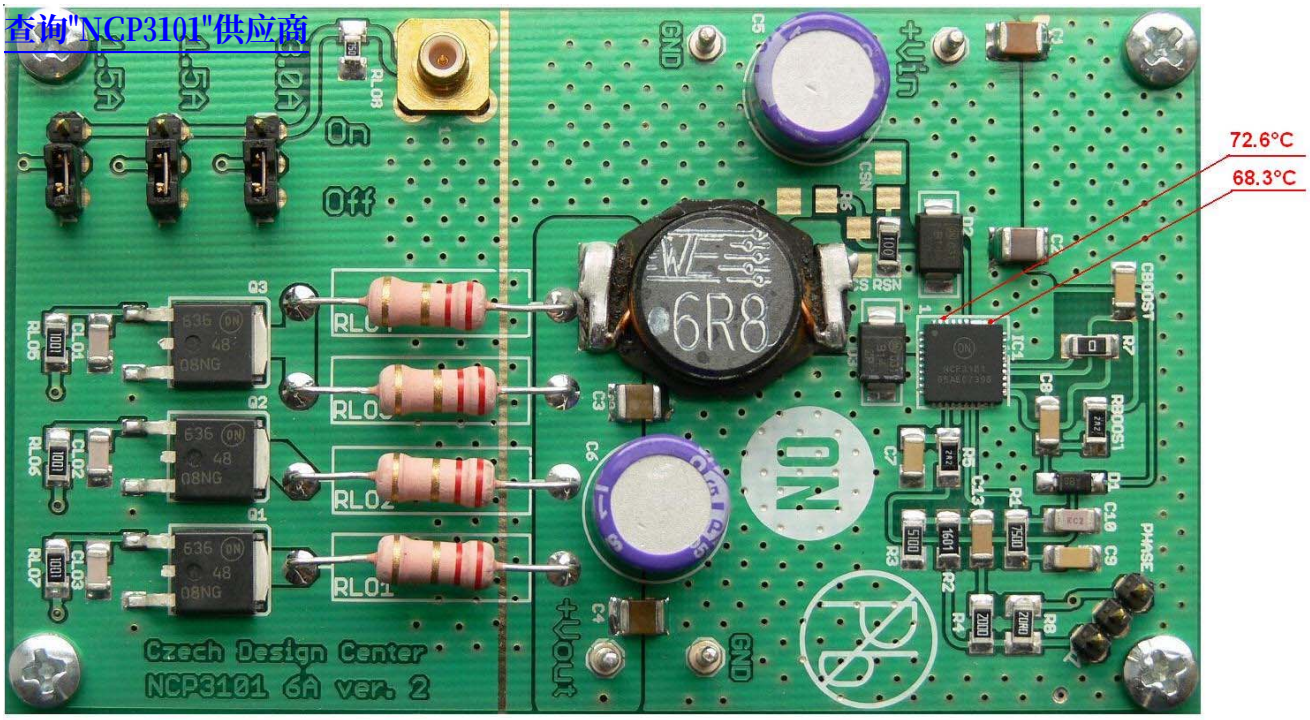


Figure 25. Temperature Conditions (V_{in} = 13.2 V, V_{out} = 3.3 V, I_{out} = 6 A) Steady State, No Additional Cooling, Ambient Temperature 25°C

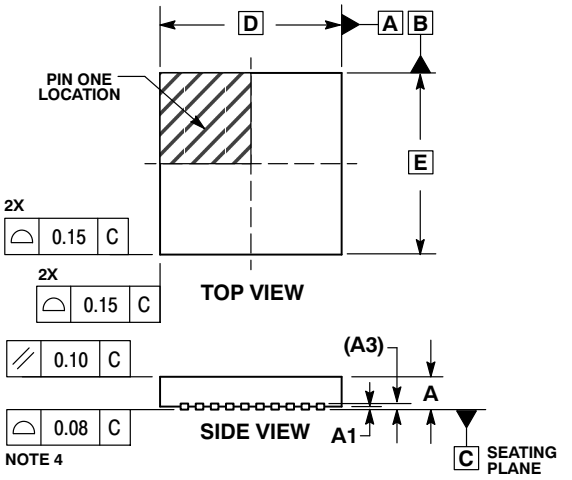
ORDERING INFORMATION

Device	Package	Temperature Grade	Shipping†
NCP3101MNTXG	QFN40 (Pb−Free)	For 0°C to +70°C	2500 / Tape & Reel
NCP3101BMNTXG	QFN40 (Pb−Free)	For −40°C to +85°C	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

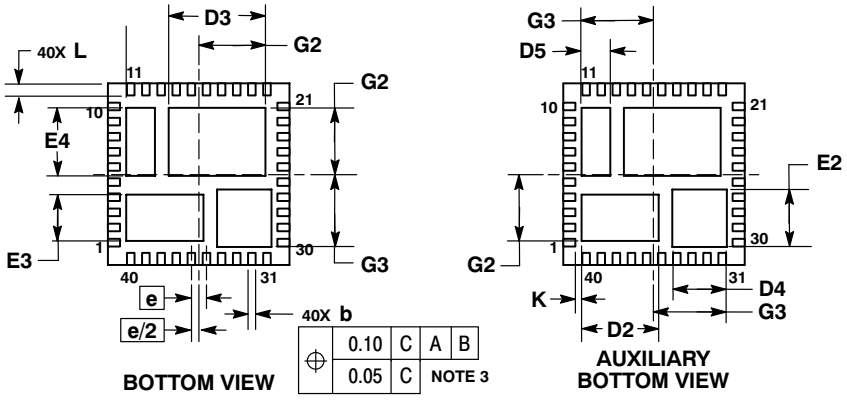
PACKAGE DIMENSIONS

QFN40 6x6, 0.5P
CASE 485AK-01
ISSUE A

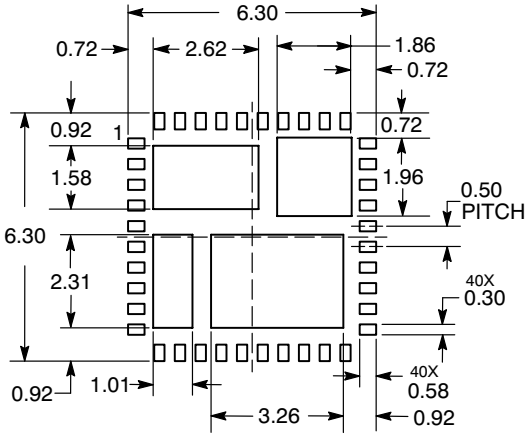


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.45	2.65
D3	3.10	3.30
D4	1.70	1.90
D5	0.85	1.05
E	6.00 BSC	
E2	1.80	2.00
E3	1.43	1.63
E4	2.15	2.35
e	0.50 BSC	
G2	2.10	2.30
G3	2.30	2.50
K	0.20	---
L	0.30	0.50



SOLDERING FOOTPRINT



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