REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																							
SHEET																							
REV																							
SHEET	22	23																					
REV STATUS OF SHEETS	REV																						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 91-05-06

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 8-BIT ANALOG I/O SYSTEM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89629

SHEET 1

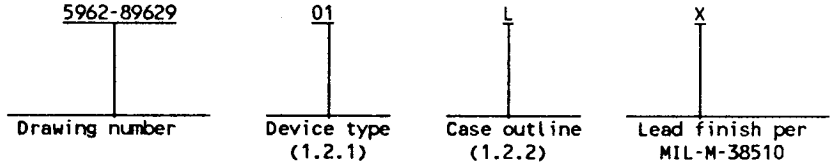
DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Relative accuracy
01	AD7569S	8-bit analog I/O system	±1 LSB for DAC and ADC
02	AD7569T	8-bit analog I/O system	±1/2 LSB for DAC and ADC

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (V_{DD}) to $AGND_{DAC}$ or $AGND_{ADC}$	-0.3 V dc to +7.0 V dc
Supply voltage (V_{DD}) to DGND	-0.3 V dc to +7.0 V dc
V_{DD} to V_{SS}	-0.3 V dc to +14 V dc
$AGND_{DAC}$ or $AGND_{ADC}$ to DGND	-0.3 V dc to V_{DD} +0.3 V dc
$AGND_{DAC}$ to $AGND_{ADC}$	±5.0 V dc
Logic voltage to DGND	-0.3 V dc to V_{DD} +0.3 V dc
CLK input voltage to DGND	-0.3 V dc to V_{DD} +0.3 V dc
Output voltage to $AGND_{DAC}$ 1/	V_{SS} - 0.3 V dc to V_{DD} + 0.3 V dc
Input voltage to $AGND_{ADC}$	V_{SS} - 0.3 V dc to V_{DD} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	450 mW 2/
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (Θ_{JA})	120°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage to ground (V_{SS})	-4.75 V dc to -5.25 V dc
Supply voltage to ground (V_{DD})	+4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Output may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded.
2/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Pin discriptions. The pin discriptions shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Input/output voltage ranges and unipolar/bipolar code tables. The input/output voltage ranges and unipolar/bipolar code tables shall be as specified on figure 4.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 5.

3.2.6 Load circuits. The load circuits shall be as specified on figure 6.

3.2.7 Write cycle timing waveforms . The write cycle timing waveforms shall be as specified on figure 7.

3.2.8 ADC mode 1 interface timing waveforms. The ADC mode 1 interface timing waveforms shall be as specified on figure 8.

3.2.9 ADC mode 2 interface timing waveforms. The ADC mode 2 interface timing waveforms shall be as specified on figure 9.

3.2.10 Equivalent input voltage circuit. The equivalent input voltage circuit shall be as specified on figure 10.

3.2.8 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ C_L = 100 pF to $AGND_{DAC}$, R_L = 2.0 kΩ, -55°C ≤ T_A ≤ +125°C unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
DAC specifications							
Relative accuracy	INL		01	1,2,3		±1	LSB
			02	1		±1	
				2,3,12		±1/2	
Differential nonlinearity	DNL	Guaranteed monotonic	01	1,2,3		±1	
			02	1		±1	
				2,3,12		±3/4	
Unipolar offset error		DAC data is all zeros, V_{SS} = 0 V	ALL	1		±2.0	
			01	2,3		±2.5	
			02	2,3		±2.0	
				1,12		±1.5	
Bipolar zero offset error		DAC data is all zeros, V_{SS} = -5.0 V	ALL	1		±2.0	
			01	2,3		±2.5	
			02	2,3		±2.0	
				1,12		±1.5	
Full-scale error		V_{DD} = 5.0 V, 2/	ALL	1		±2.0	
			01	2,3		±4.0	
			02	2,3		±3.0	
				12		±1.0	
Delta full scale/ delta V_{DD}		T_A = +25°C, V_{OUT} = 2.5 V, delta V_{DD} = ± 5%	ALL	1		0.5	
Delta full scale/ delta V_{SS}		T_A = +25°C, V_{OUT} = -2.5 V, delta V_{SS} = ± 5%	ALL	1		0.5	
Digital input voltage low level	V_{IL}		ALL	1,2,3		0.8	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ C_L = 100 pF to $AGND_{DAC}$, R_L = 2.0 kΩ, -55°C ≤ T_A ≤ +125°C unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
DAC specifications - Continued							
Digital Input voltage high level	V_{IH}		ALL	1,2,3	2.4		V
Input leakage current	I_{IL}	V_{IN} = 0 to V_{DD}	ALL	1,2,3		10	µA
Positive power supply current	I_{DD}	V_{OUT} = V_{IN} = 2.5 V, logic inputs = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1,2,3		13	mA
Negative power supply current (dual supplies)	I_{SS}	V_{OUT} = V_{IN} = -2.5 V, logic inputs = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1,2,3		4.0	
Input capacitance	C_{IN}	See 4.3.1b	ALL	4		10	pF
Signal-to-noise ratio	SNR	V_{OUT} = 20 kHz full scale sine wave with $f_{SAMPLING}$ = 400 kHz	01	4,5,6	44		dB
			02		46		
Total harmonic distortion	THD	V_{OUT} = 20 kHz full-scale sine wave with $f_{SAMPLING}$ = 400 kHz	ALL	4,5,6		48	
Functional test		See 4.3.1.c	ALL	7,8			
$\overline{WR}$ pulse width	t_1	See figure 7 3/	ALL	9	80		ns
				10,11	90		
$\overline{CS}$, A/$\overline{B}$ to $\overline{WR}$ setup time	t_2		ALL	9,10,11	0		
$\overline{CS}$, A/$\overline{B}$ to $\overline{WR}$ hold time	t_3		ALL	9,10,11	0		
Data valid to $\overline{WR}$ setup time	t_4		ALL	9	60		
				10,11	80		
Data valid to $\overline{WR}$ hold time	t_5		ALL	9,10,11	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
ADC specifications							
Relative accuracy	INL		01	1,2,3		±1	LSB
			02	2,3,12		±1/2	
				1		±1	
Differential nonlinearity	DNL	No missing codes	01	1,2,3		±1	
			02	2,3,12		±3/4	
				1		±1	
Unipolar offset error		V_{SS} = 0 V	ALL	1		±2.0	
			01	2,3		±3.0	
			02	2,3		±2.5	
				1,12		±1.5	
Bipolar zero offset error		V_{SS} = -5.0 V ±1.25 V range	ALL	1		±3.0	
			01	2,3		±4.0	
			02	2,3		±3.5	
				12		±2.5	
Full-scale error		V_{DD} = 5.0 V, 2/	ALL	1	-4.0	0	
				2,3	-7.5	2.0	
Delta full scale/ delta V_{DD}		V_{IN} = 2.5 V, delta V_{DD} = ± 5%	ALL	1		0.5	
Delta full scale/ delta V_{SS}		V_{IN} = -2.5 V, delta V_{SS} = ± 5%	ALL	1		0.5	
Input voltage low level	V_{IL}		ALL	1,2,3		0.8	V
Input voltage high level	V_{IH}		ALL	1,2,3	2.4		
Analog Input current	I_{IN}	See figure 10	ALL	1,2,3		±300	µA
Input leakage current	I_{IL}	$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, RANGE, $\overline{RESET}$	ALL	1,2,3		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
ADC specifications - Continued							
CLK Input current low level	I_{INL}	V_{IN} = 0 V	ALL	1,2,3		-1.6	mA
CLK Input current high level	I_{INH}	$V_{IN} = V_{DD}$	ALL	1,2,3		40	µA
Output voltage low level	V_{OL}	I_{SINK} = 1.6 mA	ALL	1,2,3		0.4	V
Output voltage high level	V_{OH}	I_{SOURCE} = 200 µA	ALL	1,2,3	4.0		
Floating state leakage current	I_{OUT}		ALL	1,2,3		±10	µA
Positive power supply current	I_{DD}	$V_{OUT} = V_{IN}$ = 2.5 V, logic inputs = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1,2,3		13	mA
Negative power supply current (dual supplies)	I_{SS}	$V_{OUT} = V_{IN}$ = -2.5 V, logic inputs = 2.4 V, CLK = 0.8 V, output unloaded	ALL	1,2,3		4.0	
Input capacitance	C_{IN}	See 4.3.1b	ALL	4		10	pF
Floating state output capacitance	C_{OUT}	See 4.3.1b	ALL	4		10	pF
Signal-to-noise ratio	SNR	V_{IN} = 100 kHz full-scale sine wave with $f_{SAMPLING}$ = 400 kHz 4/	01 02	4,5,6	44 45		dB
Total harmonic distortion	THD	V_{IN} = 100 kHz full-scale sine wave with $f_{SAMPLING}$ = 400 kHz 4/	ALL	4,5,6		48	
Conversion time with external clock		f_{CLK} = 5.0 MHz	ALL	9,10,11		2.0	µs
Conversion time with internal clock			ALL	7,8	1.6	2.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz $-55°C \le T_A \le +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
ADC specifications - Continued							
Functional test		See 4.3.1c	ALL	7,8			
$\overline{ST}$ pulse width	t_6	See figure 8 3/	ALL	9,10,11	50		ns
$\overline{ST}$ to $\overline{BUSY}$ delay	t_7		ALL	9		110	
				10,11		150	
$\overline{BUSY}$ to $\overline{INT}$ delay	t_8		ALL	9		20	
				10,11		30	
$\overline{BUSY}$ to $\overline{CS}$ delay	t_9		ALL	9,10,11	0		
$\overline{CS}$ to $\overline{RD}$ setup time	t_{10}		ALL	9,10,11	0		
$\overline{RD}$ pulse width determined by t_{13}	t_{11}	See figure 8 3/ 5/	ALL	9	60		ns
				10,11	90		
$\overline{CS}$ to $\overline{RD}$ hold time	t_{12}		ALL	9,10,11	0		
Data access time after RD	t_{13}	See figure 8 C_L = 20 pF, 3/, 6/	ALL	9	60		
				10,11	90		
Data access time after RD		See figure 8 C_L = 100 pF, 3/, 6/	ALL	9	95		
				10,11	135		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ f_{CLK} = 5.0 MHz $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Device types	Group A subgroups	Limits Min	Limits Max	Unit
ADC specifications - Continued							
Bus relinquish time after RD 5/, 7/	t_{14}	See figure 8 3/ 7/	ALL	9	10	60	
				10,11	10	85	
$\overline{RD}$ to $\overline{INT}$ delay	t_{15}	See figure 8 3/	ALL	9		65	
				10,11		85	
$\overline{RD}$ to $\overline{BUSY}$ delay	t_{16}		ALL	9		120	
				10,11		160	
Data valid after BUSY	t_{17}	See figure 9 C_L = 20 pF 3/ 6/	ALL	9		60	
				10,11		90	
		See figure 9 C_L = 100 pF 3/ 6/	ALL	9		90	
				10,11		135	

1/ Unless otherwise specified, V_{DD} = 5.0 ±5%, V_{SS} = RANGE = $AGND_{ADC}$ = DGND = 0 V; specifications apply for all output ranges including bipolar ranges with dual supply operation.

2/ Includes internal voltage reference error and is calculated after offset error has been adjusted out.

For DAC specifications:
a) Ideal unipolar full scale voltage is (FS - 1 LSB).
b) Ideal bipolar positive full scale voltage is (FS/2 - 1 LSB).
c) Ideal bipolar negative full scale voltage is (-FS/2).

For ADC specifications:
a) Ideal unipolar last code transition occurs at (FS - 3/2 LSB).
b) Ideal bipolar last code transition occurs at (FS/2 - 3/2 LSB).

3/ All input control signals are specified with $t_R = t_F$ = 5.0 ns (10% to 90% of +5.0 V) and timed from a voltage level of 1.6 V. ADC is sampled tested in mode 1 only.

4/ Exact frequencies are 101 kHz and 384 kHz to avoid harmonics coinciding with sampling frequency.

5/ Tested initially and after process and design changes only.

6/ t_{13} and t_{17} are measured with the load circuits on figure 6 and defined as the time required for an output to cross either 0.8 V or 2.4 V.

7/ t_{14} is defined as the time required for the data line to change 0.5 V when loaded with circuit on figure 6.

Device types	01 and 02	01
Case outline	L	3
Terminal number	Terminal symbol	
1	$AGND_{DAC}$	NC
2	V_{OUT}	$AGND_{DAC}$
3	V_{SS}	V_{OUT}
4	RANGE	V_{SS}
5	$\overline{RESET}$	RANGE
6	DB7	$\overline{RESET}$
7	DB6	DB7
8	DB5	NC
9	DB4	DB6
10	DB3	DB5
11	DB2	DB4
12	DGND	DB3
13	DB1	DB2
14	DB0	DGND
15	$\overline{WR}$	NC
16	$\overline{CS}$	DB1
17	$\overline{RD}$	DB0
18	$\overline{ST}$	$\overline{WR}$
19	$\overline{BUSY}$	$\overline{CS}$
20	$\overline{INT}$	$\overline{RD}$
21	CLK	$\overline{ST}$
22	$AGND_{ADC}$	NC
23	V_{IN}	$\overline{BUSY}$
24	V_{DD}	$\overline{INT}$
25		CLK
26		$AGND_{ADC}$
27		V_{IN}
28		V_{DD}

FIGURE 1. Terminal connections.

Pin	Description
$AGND_{DAC}$	Analog ground for the DAC(s). Separate ground return paths are provided for the DAC(s) and ADC to minimize crosstalk.
V_{OUT}	Output voltage. V_{OUT} is the buffered output voltage from the device DAC. Four different output voltage ranges can be achieved (see input/output ranges table shown on figure 4).
V_{SS}	Negative supply voltage (-5.0 V for dual supply or 0 V for single supply). This pin is also used with the RANGE pin to select the different input/output ranges and changes the data format from binary (V_{SS} = 0 V) to 2s complement (V_{SS} = -5.0 V) (see input/output ranges table shown on figure 4).
RANGE	Range selection input. This is used with the V_{SS} input to select the different ranges as per input/output ranges table shown on figure 4. The range selected applies to both the analog input voltage of the ADC and the output voltage from the DAC(s).
$\overline{RESET}$	Reset input (active low). This is an asynchronous system reset which clears the DAC register(s) to all zeros and clears the $\overline{INT}$ line of the ADC (i.e., makes the ADC ready for new conversion). In unipolar operation this input sets the output voltage to 0 V; in bipolar operation it sets the output to negative full scale.
DB7	Data bit 7. Most significant bit (MSB).
DB6 - DB2	Data bit 6 to data bit 2.
DGND	Digital ground.
DB1	Data bit 1.
DB0	Data bit 0. Least significant bit

FIGURE 2. Pin descriptions.

Pin	Description
$\overline{WR}$	Write input (edge triggered). This is used in conjunction with CS to write data into the device DAC register. It is used in conjunction with CS and A/B to write data into the selected DAC register of the device. Data is transferred on the rising edge of WR.
$\overline{CS}$	Chip select input (active low). The device is selected when this input is active.
$\overline{RD}$	Read input (active low). This input must be active to access data from the part. In the mode 2 interface, RD going low starts conversion. It is used in conjunction with the CS input.
$\overline{ST}$	Start conversion (edge triggered). This is used when precise sampling is required. The falling edge of ST starts conversion and drives BUSY low. The ST signal is not gated with CS.
$\overline{BUSY}$	BUSY status output (active low). When this pin is active the ADC is performing a conversion. The input signal is held prior to the falling edge of BUSY.
$\overline{INT}$	Interrupt output (active low). $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ goes high on the rising edge of CS or RD and is also set high by a low pulse on RESET.
CLK	A TTL compatible clock signal may be used to determine the ADC conversion time. Internal clock operation is achieved by connecting a resistor and capacitor to ground.
$AGND_{ADC}$	Analog ground for the ADC.
V_{IN}	Analog input. Various input ranges can be selected (see input/output ranges table shown on figure 4).
V_{DD}	Positive supply voltage (+5.0 V).

FIGURE 2. Pin descriptions - Continued.

$\overline{CS}$	$\overline{WR}$	$\overline{RESET}$	DAC FUNCTION
H	H	H	DAC register unaffected
L	L	H	DAC register unaffected
L	_|‾	H	DAC register updated
_|‾	L	H	DAC register updated
X	X	L	DAC register loaded with all zeros

L = Low H = High X = Don't care

FIGURE 3. Truth table.

Range	V_{SS}	Input/output voltage range	DB0-DB7 Data format
0	0 V	0 to +1.25 V	Binary
1	0 V	0 to +2.5 V	Binary
0	-5.0 V	± 1.25 V	2s Complement
1	-5.0 V	± 2.5 V	2s Complement

FIGURE 4a. Input/output ranges.

DAC register contents MSB LSB	Analog output, V_{OUT}
1111 1111	$+V_{REF}(255/256)$
1000 0001	$+V_{REF}(129/256)$
1000 0000	$+V_{REF}(128/256) = +V_{REF}/2$
0111 1111	$+V_{REF}(127/256)$
0000 0001	$+V_{REF}(1/256)$
0000 0000	0 V

FIGURE 4b. Unipolar (0 to +1.25 V) code table.

DAC register contents MSB LSB	Analog output, V_{OUT}
0111 1111	$+V_{REF}(127/128)$
0000 0001	$+V_{REF}(1/128)$
0000 0000	0 V
1111 1111	$-V_{REF}(1/128)$
1000 0001	$-V_{REF}(127/128)$
1000 0000	$-V_{REF}(128/128) = -V_{REF}$

FIGURE 4c. Bipolar (-1.25 to +1.25 V) code table.

FIGURE 4. Input/output voltage ranges and unipolar/bipolar code tables.

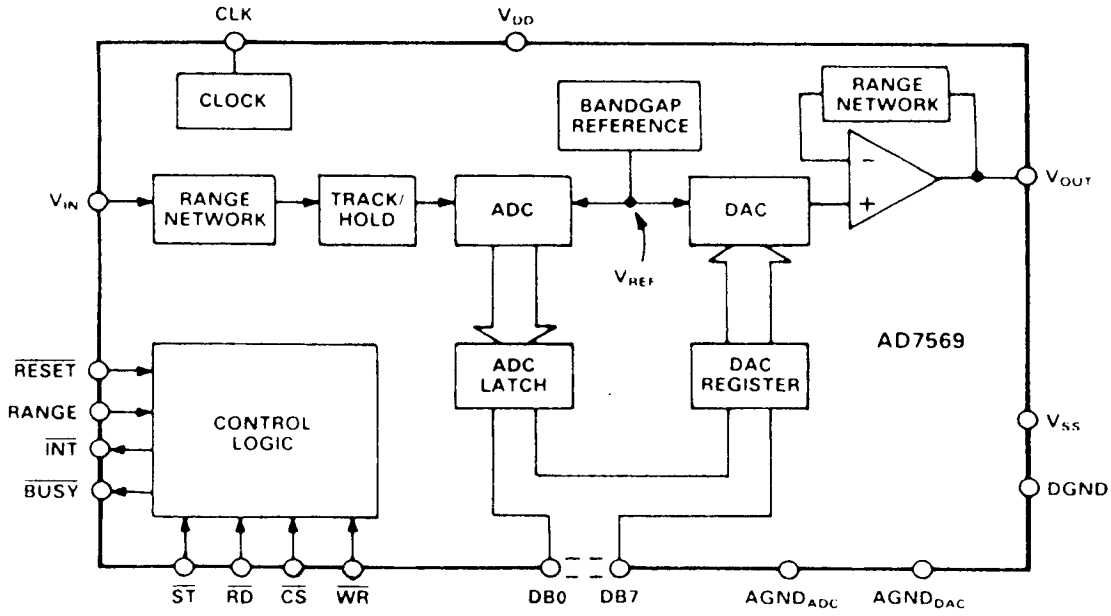
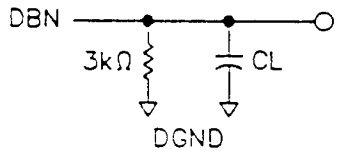
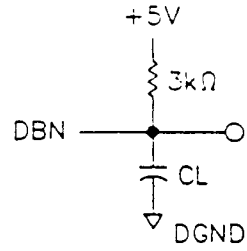


FIGURE 5. Logic diagram.

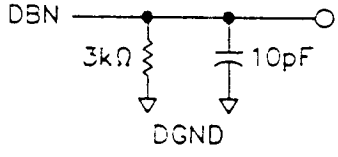


HIGH-Z TO V_{OH}

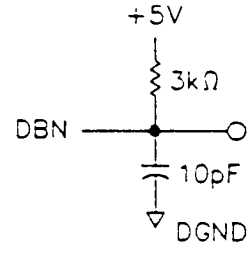


HIGH-Z TO V_{OL}

Load circuits for data access time test.



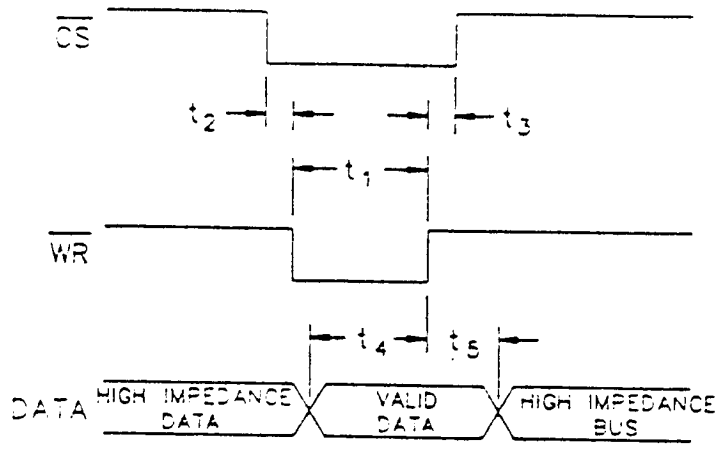
V_{OH} TO HIGH-Z



V_{OL} TO HIGH-Z

Load circuits for bus relinquish time test.

FIGURE 6. Load circuits.



NOTES:
1. All input rise and fall times measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
2. Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$.

FIGURE 7. Write cycle timing waveforms.

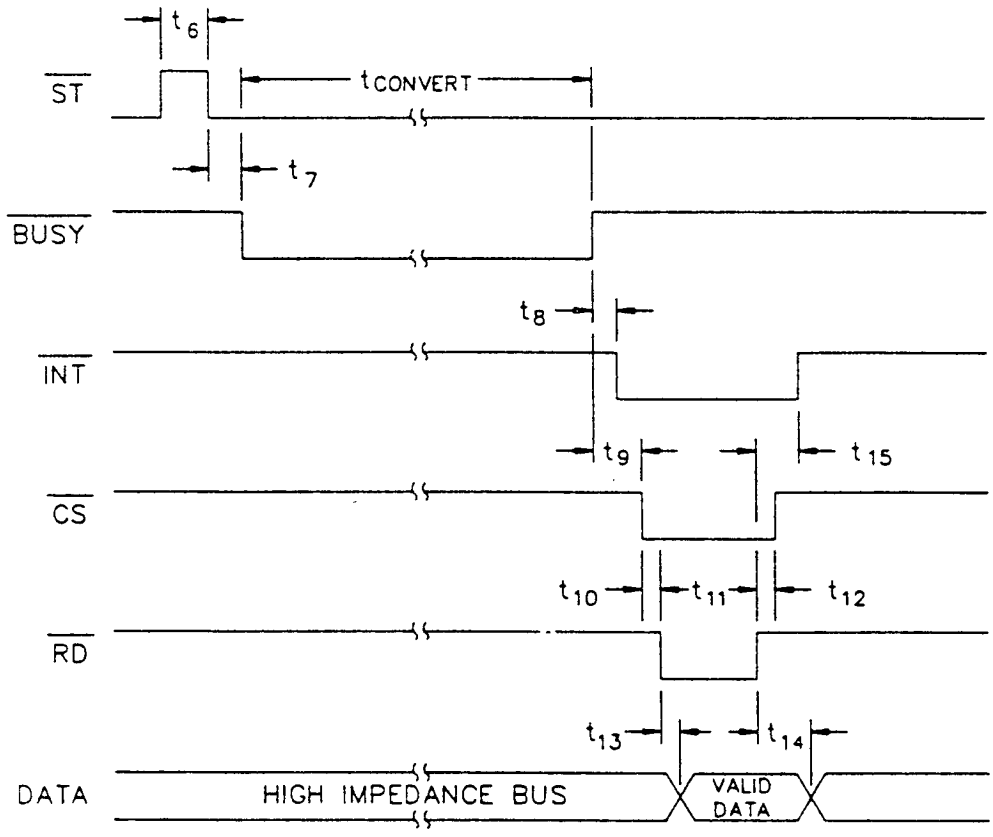


FIGURE 8. ADC mode 1 interface timing waveforms.

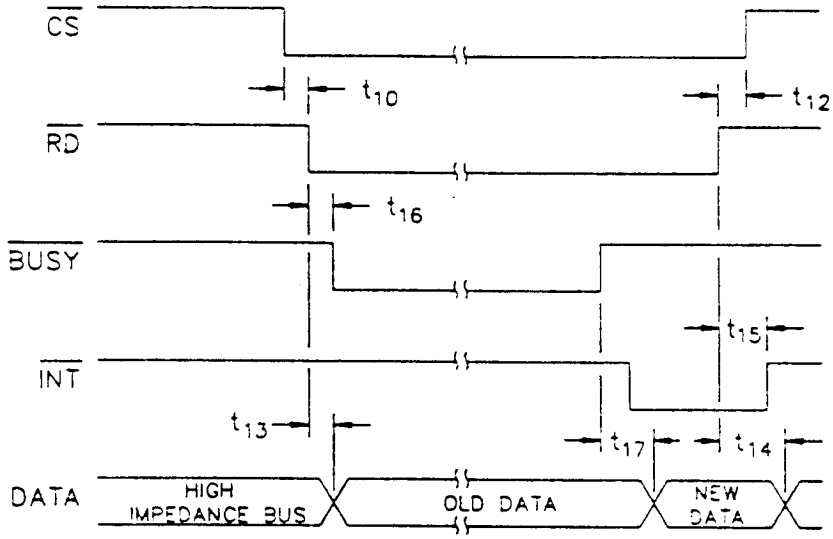
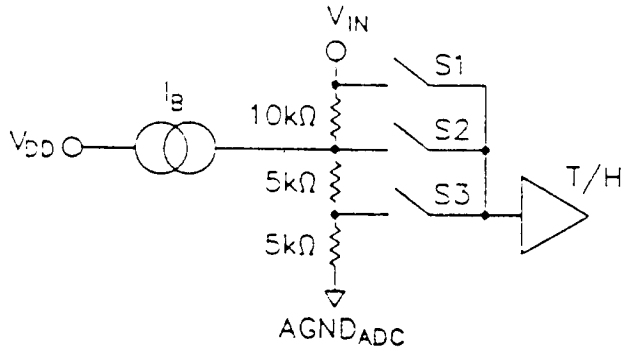


FIGURE 9. ADC mode 2 interface timing waveforms.



Voltage range	On switch	I_B
0 to +1.25 V	S1	20 µA
0 to +2.5 V	S2	20 µA
-1.25 to +1.25 V	S2	140 µA
-2.5 to +2.5 V	S3	280 µA

FIGURE 10. Equivalent input voltage circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

c. Subgroups 7 and 8 shall include verification of the truth table.

d. Subgroup 12 is used for parts grading and selection.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,4, 5,6,12
Group A test requirements (method 5005)	1,2,3,4,5,6, 9,10**,11**,12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.