OKI Semiconductor

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ML7005

DTMF Transceiver

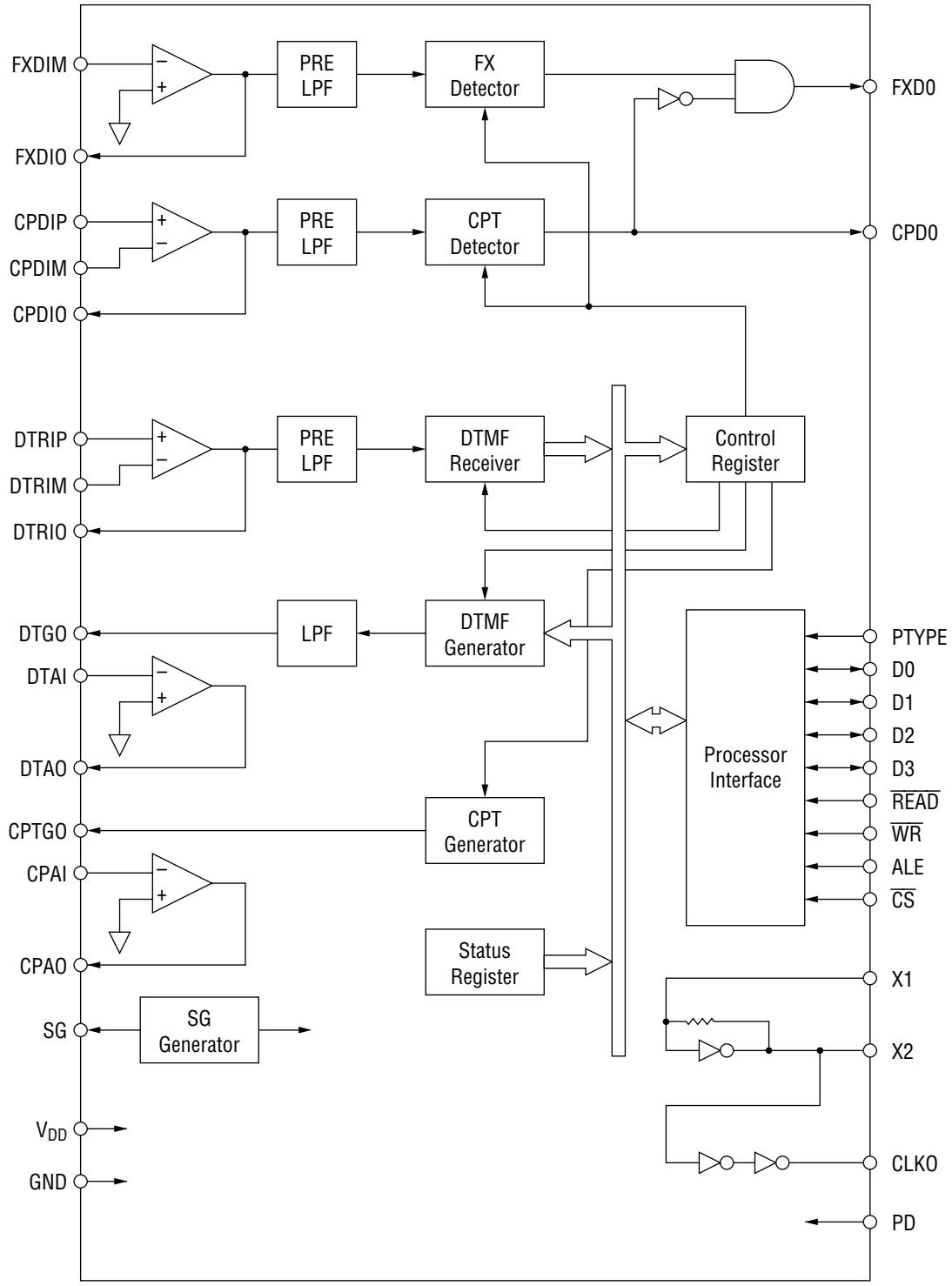
GENERAL DESCRIPTION

The ML7005 is a multi-functional DTMF transceiver LSI with built-in a DTMF signal generator, a DTMF signal receiver, a call progress tone generator, a call progress tone detector, and a FAX (FX) signal detector.
Each functional block can be controlled by an external MCU via a 4-bit processor interface.
The ML7005 does not contains a modem. However, the DTMF system data transmission is possible at less than 66 bps by setting the DTMF receiver to the high-speed detection mode.
The ML7005 operates with low-power consumption and is suitable for remote control systems, especially for ACR (Automatic Cost Routing) controllers.

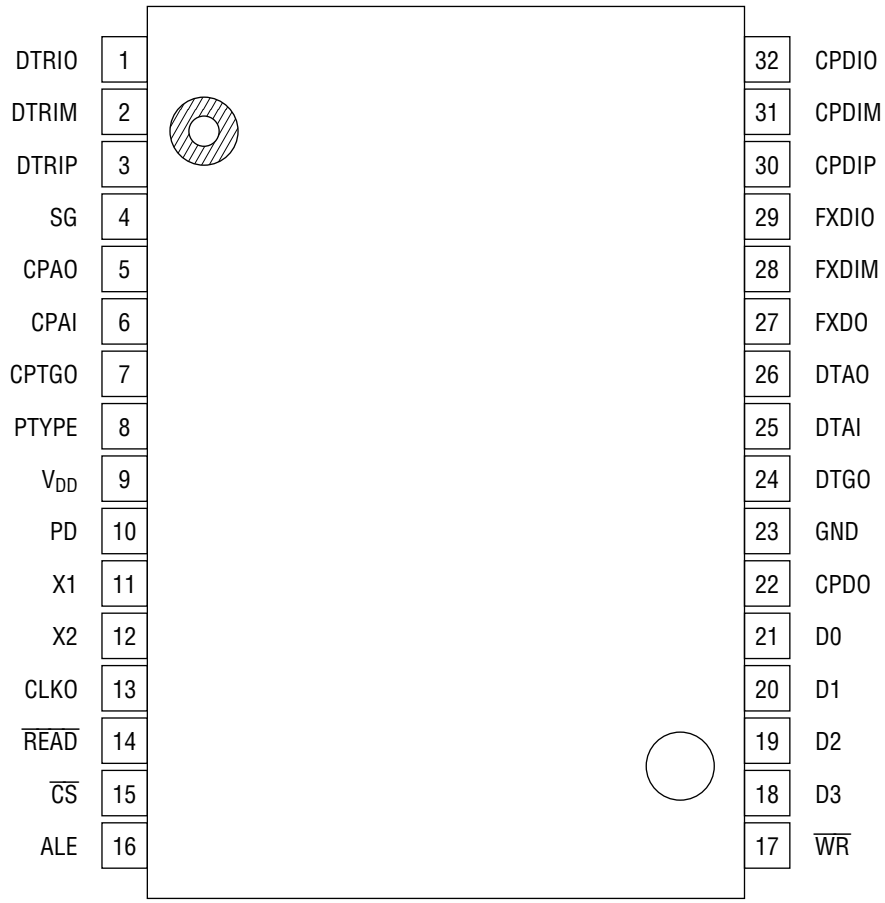
FEATURES

- Wide range of power supply voltage : +2.7 V to +5.5 V
- Low power consumption
  Operating mode : 4.0 mA (V_{DD} = 3 V) Typ.
  Operating mode : 5.0 mA (V_{DD} = 5 V) Typ.
  Power down mode : 1 µA Typ.
- The 4-bit processor interface supports both the Intel processor mode in which a read signal and a write signal are used independently of each other, and the Motorola processor mode in which a read signal and a write signal are used in common.
- The DTMF receiver can select either the high-speed detection mode (signal repeat time: more than 60 ms) or the normal detection mode (signal repeat time: more than 90 ms).
- Built-in call progress tone generator
- Built-in FAX signal (FX: 1300 Hz) detector
- The DTMF signal generator, DTMF signal detector, call progress tone generator, and call progress tone detector can operate concurrently.
- Built-in 3.579545 MHz crystal oscillator circuit
- Package :
  32-pin plastic SSOP (SSOP32-P-430-1.00-K) (Product name: ML7005MB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic SSOP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	DTRIO	O	Output pin for DTMF signal receiver input amplifier. See the figure 8 for adjusting the receive signal level. See the figure 10 when the DTMF signal receiver is not used.
2	DTRIM	I	Inverting input pin for DTMF signal receiver input amplifier.
3	DTRIP	I	Non-inverting input pin for DTMF signal receiver input amplifier.
4	SG	O	Output pin for signal ground. The output voltage is half of V_{DD}. Connect SG and GND by a 1 µF capacitor. This pin goes to a high impedance state when in power down mode.
5	CPAO	O	Output pin for amplifier used for adjusting the transmit output level of CPT (Call Progress Tone) signal generator. The non-inverting input of this amplifier is internally connected to SG. See the figure 11 for adjusting the transmit signal level. When this amplifier is not used, the CPAO pin should be shorted to the CPAI pin.
6	CPAI	I	Inverting input pin for amplifier used to adjust the transmit level of the CPT signal generator.
7	CPTGO	O	Analog output pin for CPT signal generator. The tone amplitude is approximately - 3 dBm. The transmit signal level can be changed by using the CPAO and CPAI pins. See the figure 11 for adjusting the transmit signal level. Control the ON/OFF of CPT transmission by using CPGC of the control register.
8	PTYPE	I	Input pin for selecting the processor mode. This selection determines the functions of $\overline{READ}$, $\overline{CS}$, ALE, $\overline{WR}$, D1 and D0 pins. When this pin is "1", the Intel processor mode is selected. When this pin is "0", the Motorola processor mode (MSM7524-compatible) is selected. This pin should be fixed at "0" or "1".
9	V_{DD}	—	Power supply pin.
10	PD	I	Input pin for controlling the power down mode. When this pin is set to "1", the entire LSI enters the power down mode and each functional operation stops. The DC level of the analog output pin becomes undefined. The digital output pins (FXD0, CPD0) and status register indicate a non-detection state. At that time, the control register CR and DTMF transmit register DTMFT are cleared. ("0" is written) The internal circuits (timer, etc. for each detector) also are reset. After turning on the power, set this pin to "1" to reset the LSI before using this LSI. When this pin is set to "0", the normal operation starts.
11	X1	I	X1 and X2 are connected to a 3.579545 MHz crystal. See "Oscillation Circuit" of the FUNCTIONAL DESCRIPTION for reference.
12	X2	O	
13	CLKO	O	3.579545 MHz clock output pin. This pin can drive one ML7005 device.

Pin	Symbol	Type	Description
14	$\overline{\text{READ}}$	I	Input pin for processor interface. When PTYPE is "1" (Intel processor mode) : This pin is the read control input pin. When this pin is set to "0", data in the specified register is output to the bus lines (D3 to D0). At that time, $\overline{\text{CS}}$ must be "0". See the figure 4 for processor interface timing. When PTYPE is "0" (Motorola processor mode) : This pin is the clock input pin (equivalent to SCLK of the MSM7524). When in Write mode, data in D3 to D0 is written to the specified register at the falling edge of the $\overline{\text{READ}}$ signal. When in Read mode, data in the specified register is output to D3 to D0 when the $\overline{\text{READ}}$ signal is "1", and D3 to D0 is opened when the $\overline{\text{READ}}$ signal is "0". The $\overline{\text{READ}}$ signal is not necessarily a periodical signal. See the figure 5 for processor interface timing.
15	$\overline{\text{CS}}$	I	Chip select input pin for processor interface. When the $\overline{\text{CS}}$ signal is "0", read and write operations are possible. When the $\overline{\text{CS}}$ signal is "1", read and write operations are impossible.
16	ALE	I	Input pin for processor interface. When PTYPE is "1" (Intel processor mode) : This pin is the address latch enable input pin. The register address data in D1 to D0 is latched at the falling edge of ALE. When PTYPE is "0" (Motorola processor mode) : This pin is the address data input pin (equivalent to AD0 of the MSM7524). When this pin is "1", data can be written to the control register (CR) and data can be read from the status register (STR). When this pin is "0", data can be written to the DTMF transmit register (DTMFT) and data can be read from the DTMF receive register (DTMFR).
17	$\overline{\text{WR}}$	I	Input pin for processor interface. When PTYPE is "1" (Intel processor mode) : This pin is the Write control input. Data in the data bus lines (D3 to D0) is written to the specified register. At that time, $\overline{\text{CS}}$ must be "0". When PTYPE is "0" (Motorola processor mode) : This is the signal input pin for controlling the Read and Write modes (equivalent to R/$\overline{\text{W}}$ of the MSM7524). When this pin is "1", the LSI enters the Read mode. When this pin is "0", the LSI enters the Write mode.
18 - 21	D3 - D0	I/O	4-bit data bus I/O pins for processor interface. When PTYPE is "1" (Intel processor mode), D1 and D0 are also used for addressing.
22	CPDO	O	Digital output pin for CPT detector. When a 400 Hz signal is input to the CPDIP and CPDIM pins, this pin is "1". When the DOEN register is "0", this pin is fixed at "0".
23	GND	—	Ground pin.
24	DTGO	O	Analog output pin for DTMF signal generator. The tone amplitude is approximately - 9.0 dBm for a low group and approximately - 7.0 dBm for a high group. The transmit signal level can be changed by using the DTAI and DTAO pins. See the figure 11 for adjusting the transmit signal level. Control the ON/OFF of signal transmission by using MFC of the control register.

Pin	Symbol	Type	Description
25	DTAI	I	Inverting input pin for operational amplifier used for adjusting the transmit output level of the DTMF signal generator. The non-inverting input of this amplifier is internally connected to SG. See the figure 11 for adjusting the transmit signal level. When this amplifier is not used, the DTAO pin should be shorted to the DTAI pin.
26	DTAO	O	Output pin for operational amplifier used for adjusting the transmit output level of the DTMF signal generator.
27	FXDO	O	Digital output pin for FAX signal (FX) detector. When a 1300 Hz signal is input to the FXDIM, this pin is "1". When a call progress tone (CPT) is received (CPD0="1"), this pin is forced to be "0". When the DOEN register is "0", this pin is fixed at "0".
28	FXDIM	I	Inverting input pin for input amplifier used for detecting the FAX signal (FX). See the figure 9 for adjusting the receive signal level. When the FX detector is not used, the FXDIM pin should be shorted to the FXDIO pin.
29	FXDIO	O	Output pin for input amplifier used for detecting the FAX signal (FX).
30	CPDIP	I	Non-inverting input pin for input amplifier used for detecting the CPT. See the figure 8 for adjusting the receive signal level. When the CPT detector is not used, see the figure 10.
31	CPDIM	I	Inverting input pin for input amplifier used for detecting the CPT.
32	CPDIO	O	Output pin for input amplifier used for detecting the CPT.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C With respect to GND	–0.3 to +7.0	V
Input Voltage	V_I		–0.3 to V_{DD} + 0.3	
Storage Temperature	T_{stg}	—	–55 to +150	°C
Output Short Current	I_{SHT}	Short to V_{DD} or GND	35	mA
Power Dissipation	P_D	—	100	mW

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage		V_{DD}	—	2.7	3.6	5.5	V
Operating Temperature Range		T_{OP}	—	–30	—	+85	°C
Input Clock Frequency Deviation		f_{CLK}	An external clock is applied to X1	–0.1	—	+0.1	%
Input Clock duty		DUTY		40	—	60	%
X1, X2 Load Capacitance		C1, C2	—	18	20	22	pF
SG Bypass Capacitance		C3	SG - GND	1	—	—	µF
V_{DD} Bypass Capacitance		C4	V_{DD} - GND	10	—	—	
		C5		0.1	—	—	
Digital Input Rise Time		T_{IR}	PD, $\overline{READ}$, $\overline{CS}$, ALE, $\overline{WR}$, D3 to D0	—	—	50	ns
Digital Input Fall Time		T_{IF}		—	—	50	
Digital Ouput Load Capacitance		C_{DL1}	FCDO, CPDO, D3 to D0	—	—	40	pF
		C_{DL2}	CLKO	—	—	20	
Crystal	Frequency Deviation	—	+25°C ±5°C	–100	—	+100	ppm
	Temperature Characteristics	—	–30°C to +85°C	–100	—	+100	
	Equivalent Series Resistance	—	—	—	—	90	Ω
	Load Capacitance	—	—	—	16	—	pF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition or Applicable pin		Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode	V_{DD} = 2.7 to 5.5 V	—	—	9.0	mA
			V_{DD} = 3 V	—	4.0	—	
			V_{DD} = 5 V	—	5.0	—	
	I_{DD2}	Power Down Mode		—	1	40	µA
Digital Input Voltage	V_{IH}	—		0.7 V_{DD}	—	V_{DD}	V
	V_{IL}			0.0	—	0.3V_{DD}	
Digital Input Current	I_{IH}	V_I = V_{DD}		–10	0	+10	µA
	I_{IL}	V_I = 0 V		–10	0	+10	
Digital Output Voltage	V_{OH}	Other than CLKO	I_{OH} = –100 µA	V_{DD} – 0.2	V_{DD} – 0.06	V_{DD}	V
	V_{OL}		I_{OL} = 100 µA	0.0	0.06	0.2	
	V_{OHCK}	CLKO, CL ≤ 20pF		V_{DD} – 0.5	—	V_{DD}	
	V_{OLCK}			0.0	—	0.5	
Analog Input Resistance	R_{IN}	*1		—	10	—	MΩ
Analog Output DC Potential	V_{SG}	SG		V_{DD} /2–0.1	V_{DD}/2	V_{DD} /2–0.1	V
	V_{AO}	*2		—	V_{DD}/2	—	
Analog Output Load Resistance	R_{OUT}	*3		20	—	—	KΩ

*1 DTRIM, DTRIP, CPAI, DTAI, FXDIM, CPDIP, CPDIM
*2 DTRIO, CPAO, CPTGO, DTGO, DTAO, FXDIO, CPDIO
*3 DTRIO, CPAO, CPTGO, DTGO, DTAO, FXDIO, CPDIO, SG

AC CHARACTERISTICS

AC Characteristics 1 DTMF Signal Generator

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
DTMF Tone Transmit Amplitude	V_{DTTL}	Measured at DTGO	Low Group Tone	–10.5	–9.0	–7.5	dBm *1
	V_{DTTH}		High Group Tone	–8.5	–7.0	–5.5	
Tone Transmit Amplitude Ratio	V_{DTDF}		V_{DTTH} – V_{DTTL}	1.0	2.0	3.0	dB
Tone Frequency Accuracy	f_{DDT}		To Nominal Frequency	–1.5	—	+1.5	%
Total Harmonic Distortion	THD_{DT}		Harmonics - Fundamental	—	–40	–23	dB
Out-of-Band Spurious	V_{S1}	With respect to output signal level measured at DTGO	4kHz to 8kHz	—	P–51	P–20	dB
	V_{S2}		8kHz to 12kHz	—	P–60	P–40	
	V_{S3}		12 kHz to each 4 kHz band	—	P–75	P–60	

*1 0dBm = 0.775 Vrms (For all AC characteristics)

AC Characteristics 2 Call Progress Tone (CPT) Generator

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Tone Transmit Amplitude	V_{CPT}	—	–4	–2.5	–1	dBm
Output Frequency	f_{CPT}	—	380	400	420	Hz
Total Harmonic Distortion	THD_{CPT}	Harmonics - Fundamental	—	–39	–23	dB

AC Characteristics 3 Call Progress Tone (CPT) Detector

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
CPT Detect Amplitude	V_{DETCP}		2.7 V ≤ V_{DD} ≤ 5.5 V	–46	—	–6	dBm
			4.5 V ≤ V_{DD} ≤ 5.5 V	–46	—	0	
CPT Non-detect Amplitude	V_{REJCP}	f_{in} = 350 to 450 Hz at CPDIO		—	—	–60	
Time to Detect	t_{DETCP}		Detect	30	—	—	ms
Time to Reject	t_{REJCP}		Non-detect	—	—	10	
CPT Detect Delay Time	t_{DELCP}	See Figure 1.		10	18	30	ms
CPT Detect Hold Time	t_{HOLCP}			10	18	30	
CPT Detect Frequency	f_{DETCP}	—		350	—	450	Hz
CPT Non-detect Frequency	f_{RETCP}	—		530	—	—	Hz
				—	—	290	

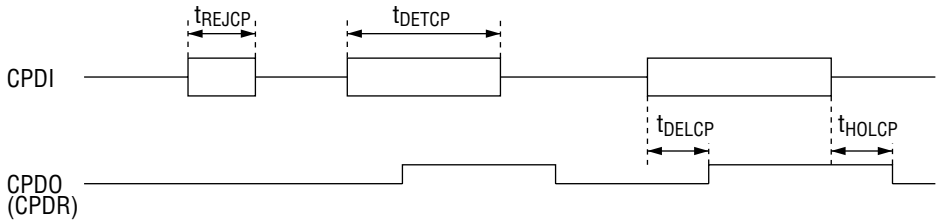


Figure 1 CPT Detect Timing

AC Characteristics 4 FAX Signal (FX) Detector

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
FX Detect Amplitude	V_{DETFX}		2.7 V ≤ V_{DD} ≤ 5.5 V	–40	—	–6	dBm
			4.5 V ≤ V_{DD} ≤ 5.5 V	–40	—	0	
FX Non-detect Amplitude	V_{REJFX}	f_{in} = 1280 to 1320 Hz at FXDIO		—	—	–60	
Time to Detect	t_{DETFX}		Detect	65	—	—	ms
Time to Reject	t_{REJFX}		Non-detect	—	—	30	
FX Detect Delay Time	t_{DELFX}	See Figure 2.		35	50	65	
FX Detect Hold Time	t_{HOLFX}			35	50	65	
FX Detect Frequency	f_{DETFX}	—		1280	—	1320	Hz
FX Non-detect Frequency	f_{REJFX}	—		1380	—	—	Hz
				—	—	1200	

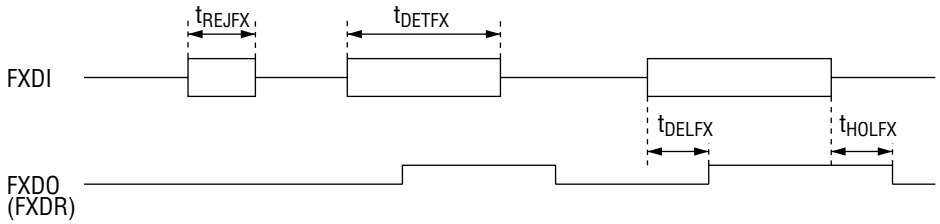


Figure 2 FX Detect Timing

AC Characteristics 5 DTMF Receiver

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
DTMF Detect Amplitude	V_{DETDT1}		2.7 V ≤ V_{DD} ≤ 5.5 V		–42	—	–10	dBm
	V_{DETDT2}		4.5 V ≤ V_{DD} ≤ 5.5 V		–42	—	0	
DTMF Non-detect Amplitude	V_{REJDT}	Per Frequency at DTRIO			—	—	–60	
Detect Frequency	f_{DETDT}	To Nominal Frequency			–1.8	—	+1.8	%
Non-detect Frequency	f_{REJDT}				3.8	—	—	
					—	—	–3.8	
Level Twist	V_{TWIST}	V_{High} Group - V_{Low} Group			–6.0	—	+6.0	dB
Noise to Signal Ratio	$V_{N/S}$	N/S (N : 0.3 to 3.4 kHz)			—	–12	—	
Dial Tone Rejection Ratio	V_{REJDT}	360 to 440 Hz			—	45	—	
Signal Repetition Time	t_{CYCDT0}	*1		DTTIM = "1"	60	—	—	ms
	t_{CYCDT1}			DTTIM = "0"	90	—	—	
Time to Detect	t_{DETDT0}		Detect	DTTIM = "1"	35	—	—	
	t_{DETDT1}			DTTIM = "0"	49	—	—	
Time to Reject	t_{REJDT0}		Non-detect	DTTIM = "1"	—	—	10	
	t_{REJDT1}			DTTIM = "0"	—	—	24	
Interdigit Pause Time	t_{POSDT0}			DTTIM = "1"	21	—	—	
	t_{POSDT1}			DTTIM = "0"	30	—	—	
Acceptable Drop Out Time	$t_{BRKDT10}$		$\overline{SP}$ = "1" (Before output)	DTTIM = "1"	—	—	0.4	
	$t_{BRKDT11}$			DTTIM = "0"	—	—	0.4	
	$t_{BRKDT20}$		$\overline{SP}$ = "0" (During output)	DTTIM = "1"	—	—	3	
	$t_{BRKDT21}$			DTTIM = "0"	—	—	10	
Detect Delay Time	t_{DELDT0}			DTTIM = "1"	12	26	37	
	t_{DELDT1}			DTTIM = "0"	24	41	49	
Detect Hold Time	t_{HOLDT0}			DTTIM = "1"	15	20	27	
	t_{HOLDT1}			DTTIM = "0"	24	28	35	
SP Delay Time	t_{SP}		DTTIM = "1", "0"		0.2	0.6	1.0	

*1 See the figure 3 for timing.
The input level includes the entire range indicated in V_{DETDT1} and V_{DETDT2}.
The input frequency includes the entire range indicated in f_{DETDT}.

Timing When DTMF is received

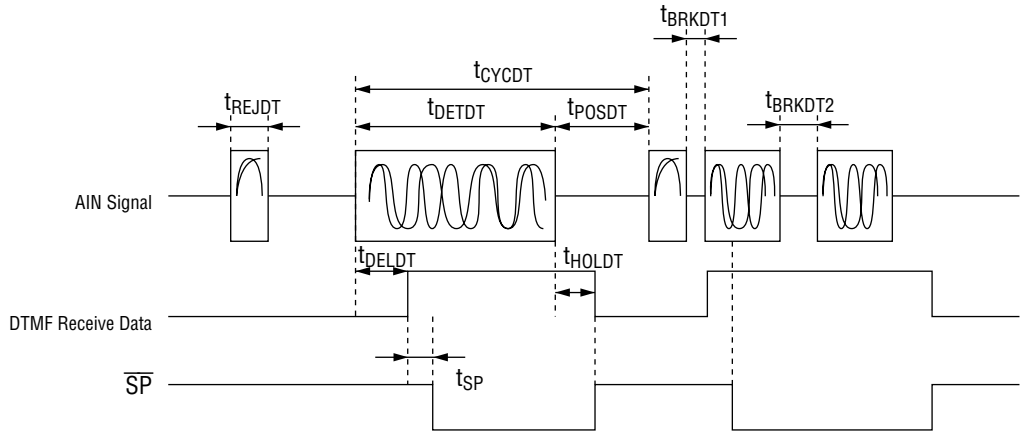


Figure 3 Timing When DTMF is Received

t_{DETDT} : Time to Detect
When Time to Detect is the specified value of t_{DETDT} or more, the DTMF signal is normally received.

t_{REJDT} : Time to Reject
When Time to Reject is the specified value of t_{REJDT} or less, the input signal is ignored and the $\overline{SP}$ and DTMF receive data are not output.

t_{POSDT} : Interdigit Pause
When there is no input signal for the period of t_{POSDT} or more, the DTMF receive data and $\overline{SP}$ are reset. Even if the receive data is changed, when Interdigit Pause Time is the value of t_{POSDT} or less (including the change without Drop Out), $\overline{SP}$ remains at "0" and the DTMF receive data may maintain its initial value.

t_{BRKDT1} : Acceptable Drop Out Time 1
Acceptable Drop Out Time 1 is applied between when the input signal comes and when $\overline{SP}$ becomes "0". Even if there is no input signal for the period of t_{BRKDT1} or less, the $\overline{SP}$ and DTMF receive data are normally output.

t_{BRKDT2} : Acceptable Drop Out Time 2
Acceptable Drop Out Time 2 is applied when $\overline{SP}$ is "0" (when receive data is output). Even if there is no input signal during signal reception for the period of t_{BRKDT2} or less, $\overline{SP}$ and DTMF receive data are not reset.

t_{CYCDT} : Signal Repetition Time
Signal Repetition Time should be the specified value of t_{CYCDT} or more so that a signal is normally received.

t_{DELDT} : Detect Delay Time
The DTMF receive data is output with a delay of the specified value of t_{DELDT} after the input signal appears.

t_{HOLDT} : Detect Hold Time The $\overline{SP}$ and DTMF receive data outputs stop with a delay of the specified value of t_{HOLDT} after the input signal disappears.

t_{SP} : SP Delay Time
The $\overline{SP}$ data is output with a delay of the specified value of t_{SP} after the DTMF receive data is output. The DTMF receive data should be latched after detecting the fall of $\overline{SP}$.

Processor Interface Charactceristics (Intel Processor Mode)

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Data Setup Time	t_{AL}	—	80	—	—	ns
Address Data Hold Time	t_{LA}	—	30	—	—	ns
ALE Signal Time	t_{LL}	—	80	—	—	ns
Chip Select Setup Time before Read	t_{CRS}	—	30	—	—	ns
Chip Select Hold Time after Read	t_{CRH}	—	30	—	—	ns
$\overline{\text{READ}}$ Data Output Delay Time	t_{RD}	$V_{OL} \leq 0.4$ V, $V_{OH} \geq V_{DD} - 0.4$ V	0	90	180	ns
Data Float Time after Read	t_{RDF}	—	5	37	60	ns
$\overline{\text{READ}}$ Signal Time	t_{RW}	—	200	—	—	ns
Chip Select Setup Time before Write	t_{CWS}	—	30	—	—	ns
Chip Select Hold Time after Write	t_{CWH}	—	30	—	—	ns
$\overline{\text{WR}}$ Signal Time	t_{WW}	—	140	—	—	ns
Data Setup Time before Write	t_{DW}	—	80	—	—	ns
Data Hold Time	t_{WD}	—	30	—	—	ns

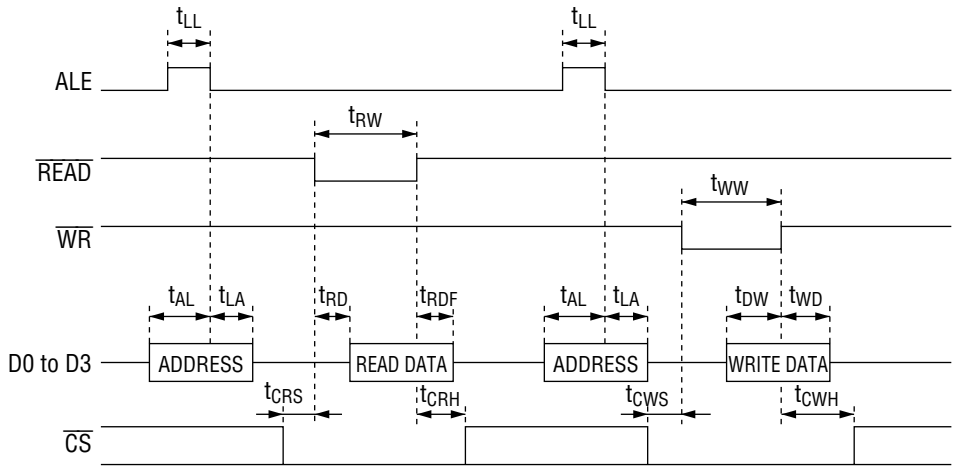


Figure 4 Processor Interface Timing (Intel Processor Mode : PTYPE="1")

Processor Interface Characteristics (Motorola Processor Mode)

(V_{DD} = 2.7 to 5.5 V, Ta = –30 to +85°C)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
$\overline{READ}$ Signal Period		t_{CYC}	See Figure 5	—	1	—	—	µs
$\overline{READ}$ Signal Pulse Width		t_{HI}		"H" period	200	—	—	ns
		t_{LO}		"L" period	200	—	—	
ALE	SETUP Time	t_{AS}		ALE → $\overline{READ}$	80	—	—	
	HOLD Time	t_{AH}		$\overline{READ}$ → ALE	20	—	—	
$\overline{CS}$	SETUP Time	t_{CS}		$\overline{CS}$ → $\overline{READ}$	80	—	—	
	HOLD Time	t_{CH}		$\overline{READ}$ → $\overline{CS}$	20	—	—	
$\overline{WR}$	SETUP Time	t_{WRS}		$\overline{WR}$ → $\overline{READ}$	80	—	—	
	HOLD Time	t_{WRH}		$\overline{READ}$ → $\overline{WR}$	20	—	—	
D3 to D0 (Write)	SETUP Time	t_{DWS}		D3 to D0 → $\overline{READ}$	80	—	—	
	HOLD Time	t_{DWH}		$\overline{READ}$ → D3 to D0	30	—	—	
D3 to D0 (Read)	Delay Time	t_{DRD}		$\overline{READ}$ → D3 to D0 $V_{OL} \leq 0.4$ V, $V_{OH} \geq V_{DD} - 0.4$ V	0	90	180	
	Hold Time	t_{DRH}		D3 to D0 → $\overline{READ}$	5	37	60	

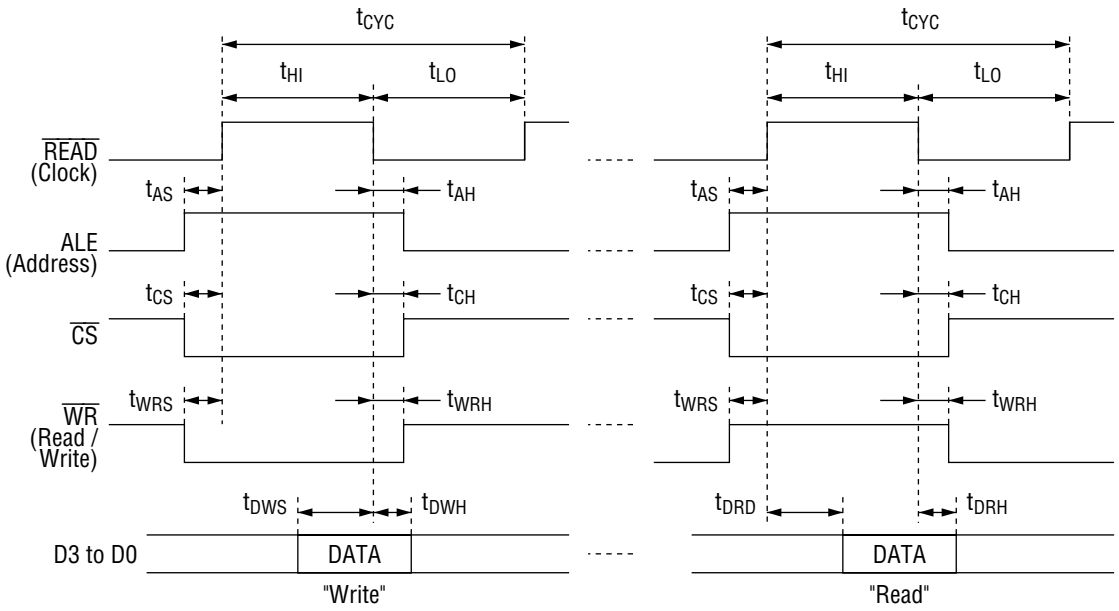


Figure 5 Processor Interface Timing (Motorola Processor Mode)

REGISTER DESCRIPTION

Register Interface Description

The ML7005 contains a 4-bit DTMF transmit data register (DTMFT), a 4-bit DTMF receive data register (DTMFR), a 4-bit control register (CR), and a 4-bit status register (STR). The DTMFT and CR registers are for Write-only and the DTMFR and STR registers are for Read-only.
When the PTYPE pin is "1", accessing the registers is possible in the Intel processor mode. When the PTYPE pin is "0", accessing the registers is possible in the Motorola processor mode.
In the Intel processor mode (PTYPE="1"), when $\overline{CS}$ is "0", data can be written to the DTMFT and CR registers by fetching data from D3 to D0 at the rising edge of the $\overline{WR}$ signal. When $\overline{CS}$ is "0", the contents of DTMFR and STR can be transferred to D3 to D0 by setting $\overline{READ}$ to "0".
In the Motorola processor mode (PTYPE="0"), when $\overline{CS}$ and $\overline{WR}$ are "0", data can be written to the DTMFT and CR registers by fetching D3 to D0 data and ALE at the falling edge of $\overline{READ}$. When $\overline{CS}$ is "0" and $\overline{WR}$ is "1", the contents of DTMFR and STR are transferred to D3 to D0 by latching ALE at the rising edge of $\overline{READ}$.
When the PD pin is set to "1" the DTMFT and CR registers are reset.

Table 1 Outline of Registers

Register name	Accessing (address) in Intel processor mode		Accessing in Motorola processor mode		Description
	D1	D0	ALE	$\overline{WR}$	
DTMFT	0	0	0	0	Writing to DTMFT
DTMFR	0	1	0	1	Reading from DTMFR
CR	1	0	1	0	Writing to CR
STR	1	1	1	1	Reading from STR

Note: The contents of the DTMFT and CR registers cannot be read.

Table 2 Register Names

Register name	D3	D2	D1	D0
DTMFT	DTT3	DTT2	DTT1	DTT0
DTMFR	DTR3	DTR2	DTR1	DTR0
CR	CPGC	DTTIM	DOEN	MFC
STR	$\overline{SP}$	FXDR	CPDR	DETF

DTMFT and DTMFR Registers

16 kinds of DTMF transmit signals can be determined by setting the DTMFT register.
16 kinds of DTMF receive signals can be monitored from the DTMFR register.
The table 3 shows the DTMF signal codes.
Even if the DTMF transmit code is changed while the DTMF signal is being transmitted (MFC="1"), the output frequency is not changed.

Table 3 DTMF Signal Code List

DTT3 DTR3	DTT2 DTR2	DTT1 DTR1	DTT0 DTR0	DIGIT	Low group signal (Hz)	High group signal (Hz)
0	0	0	1	1	697	1209
0	0	1	0	2	697	1336
0	0	1	1	3	697	1477
0	1	0	0	4	770	1209
0	1	0	1	5	770	1336
0	1	1	0	6	770	1477
0	1	1	1	7	852	1209
1	0	0	0	8	852	1336
1	0	0	1	9	852	1477
1	0	1	0	0	941	1336
1	0	1	1	*	941	1209
1	1	0	0	#	941	1477
1	1	0	1	A	697	1633
1	1	1	0	B	770	1633
1	1	1	1	C	852	1633
0	0	0	0	D	941	1633

Control Register CR

D3	D2	D1	D0
CPGC	DTTIM	DOEN	MFC

Bit No.	Name	Description
D3	CPGC	This bit is used to control the ON/OFF of call progress tone transmitting. "0" : The GPTGO output is OFF and the SG level is output. "1" : The GPTGO output is ON and CPT is output.
D2	DTTIM	This bit is used to control the detect time of DTMF receiver. "0" : Normal detect "1" : High-speed detect When there is enough time, set to the normal detect mode (DTTIM = "0") because the high-speed detect mode sometimes causes erroneous detection by noise or voice signal.
D1	DOEN	This bit is used to control the call progress tone detector and FX detector. "0" : The CPDO and FXDO output pins and CPDR and FXDR registers are fixed to "0". "1" : The CPDO and FXDO output pins and CPDR and FXDR registers become valid.
D0	MFC	This bit is used to control the ON/OFF of DTMF transmit output. "0" : The DTGO output is OFF and the SG level is output. "1" : The DTGO output is ON and the DTMF signal is output.

Status Register STR

D3	D2	D1	D0
$\overline{SP}$	FXDR	CPDR	DETF

Bit No.	Name	Description
D3	$\overline{SP}$	This bit is used to indicate whether the DTMF receive signal is being received. "0" : Indicates that the valid DTMF signal is being received. "1" : Indicates that the DTMF signal is not being received.
D2	FXDR	This bit is used to indicate whether the FAX signal (FX) is being received. "0" : Indicates that the FAX signal (FX) is not being received. "1" : Indicates that the valid FAX signal (FX: 1300 Hz) is being received. When a call progress tone is received (CPDO="1"), this bit is forced to be "0". When the DOEN register is "0", this bit also is fixed at "0". This bit has the same function as that of the FXDO.
D1	CPDR	This bit is used to indicate whether the call progress tone is being received. "0" : Indicates that the call progress tone is not being received. "1" : Indicates that the valid call progress tone (400 Hz) is being received. When the DOEN register is "0", this bit is fixed at "0". This bit has the same function as that of the CPDO pin.
D0	DETF	This is a flag to indicate that a detector has changed its status from a non-detect state to a detect state. This bit is "1" when: (1) $\overline{SP}$ is changed from "1" to "0", (2) FXDR is changed from "0" to "1", or (3) CPDR is changed from "0" to "1". This bit remains "0" even if a 1300 Hz or 400 Hz signal is input, because the FXDR and CPDR are fixed at "0" when the DOEN regsiter is "0". When the processor has read the status register, this bit is reset to "0". When the processor does not read the status register after a signal is detected, this bit is "0" after the detected signal disappears.

FUNCTIONAL DESCRIPTION

Oscillation Circuit

The X1 and X2 should be connected by a 3.579545 MHz crystal.
When the load capacitance of the crystal is 16pF, X1 and GND should be connected by a 20 pF capacitor, and X2 and GND also should be connected by a 20 pF capacitor.
If necessary, an external clock should be input to X1 via a 1000 pF capacitor, and X2 should be left open.

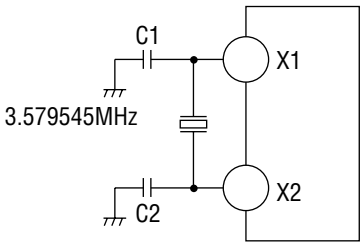


Figure 6 Crystal Connection

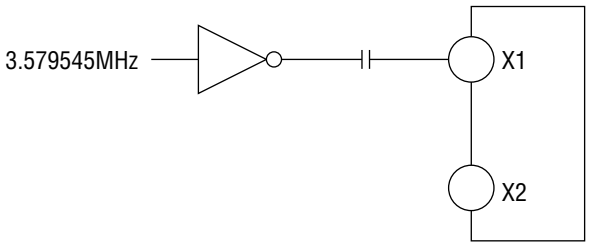


Figure 7 External Clock Connection

DTMF Receiver, CPT Detector Input Level Adjustment

Adjust the input level according to the method shown in the figure 8.
Determine the value of a usable resistor so that the levels of the outputs (DTIO, CPDIO) of each amplifier at a maximum input level are less than the maximum detect level described in the AC Characteristics.

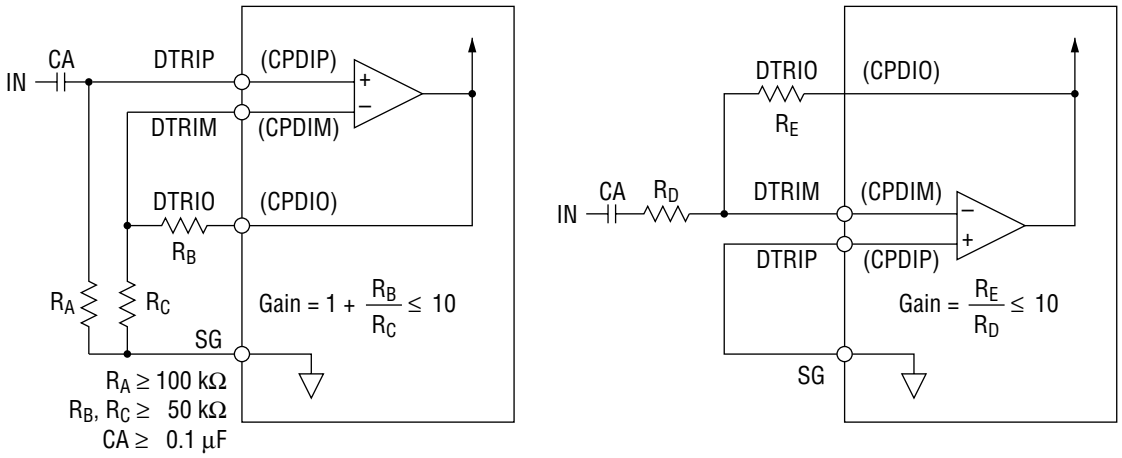


Figure 8 DTMF, CPT Input Level Adjustment

FX Detector Input Level Adjustment

Adjust the input level according to the method shown in the figure 9.
Determine the value of a usable resistor so that the output level of FXDIO is less than the maximum detect level described in the AC Characteristics.

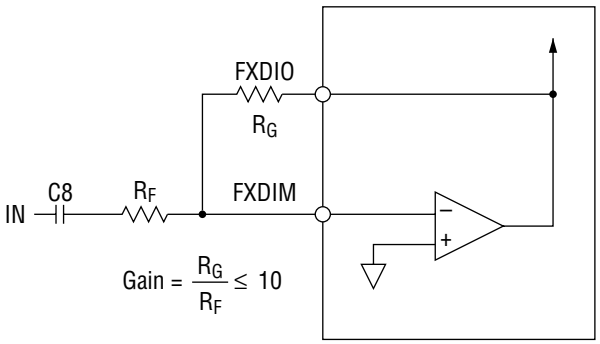


Figure 9 FX Input Level Adjustment

Processing the Input Pin when the DTMF Receiver and CPT Detector are not Used

Process the Input pin according to the method shown in the figure 10.

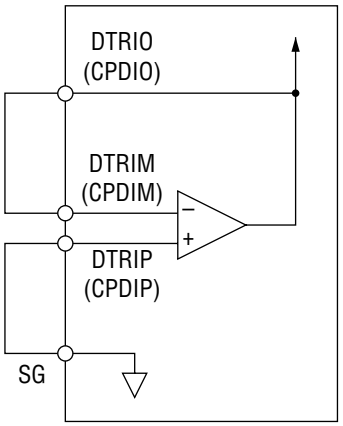


Figure 10 Processing the Unused Input Pin

Adjusting the Analog Output Level

Adjust the analog output level according to the method shown in the figure 11.
$R_I/R_H \leq 1.6$ is always required when $V_{DD} \geq 4.5$ V.
In the case of $R_I/R_H > 1$, if $R_I/R_H = A$, the maximum analog output load resistance is 20*A (kΩ).
If V_{DD} is less than 4.5 V, $R_I/R_H \leq 1$ is required.

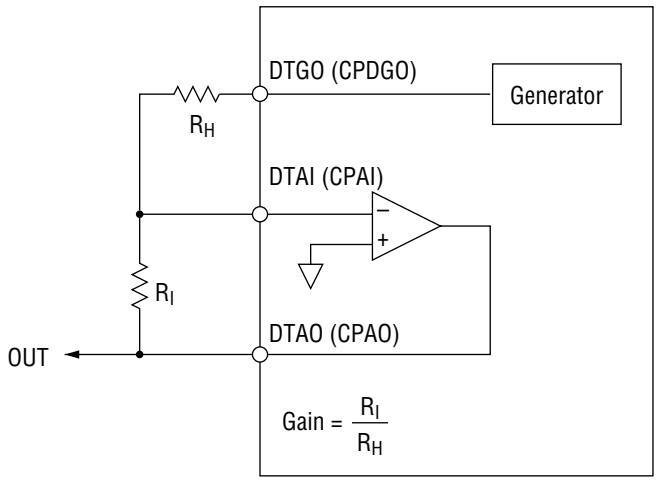


Figure 11 Analog Output Level Adjustment

Concurrent Operation of 4 Functions

The DTMF signal generator, DTMF signal detector, call progress tone generator, and call progress tone detector can operate concurrently.
When both the DTMF signal generator and call progress tone generator operate concurrently, the DTMF signal sometimes cannot be detected if the receive level of the DTMF signal is less than -36 dBm.

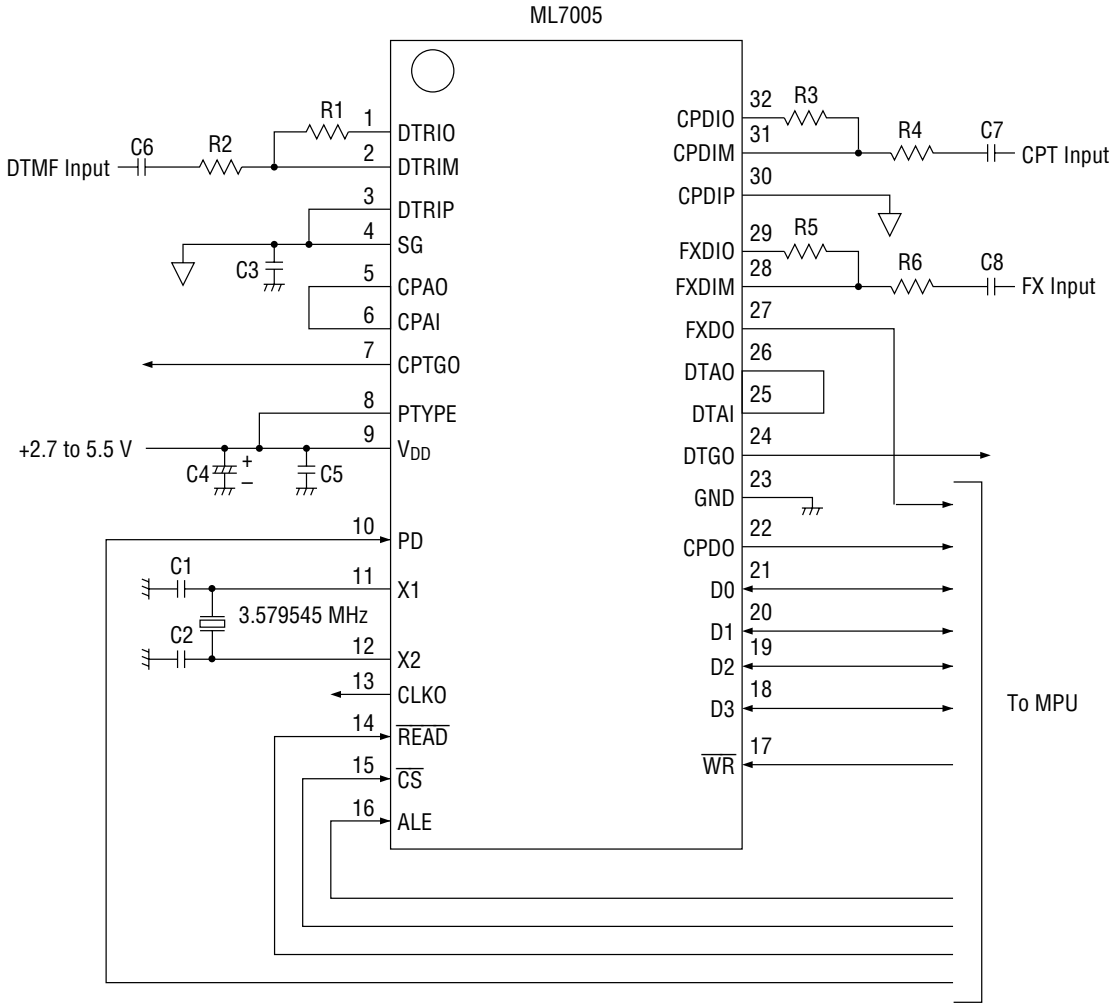
Register Settings for Each Mode

An example of register settings for each mode is shown below.

Table 4 Register Setting

Mode	Description	Address in Intel processor mode	Motorola processor mode		D3	D2	D1	D0	Active register
		D1, D0	ALE	$\overline{WR}$					
Power ON	(1) Wait until power supply is stabilized	—	—	—	—	—	—	—	—
	(2) PD pin = "1" (internal circuit is reset)	—	—	—	—	—	—	—	—
	(3) Wait 200 µs or more	—	—	—	—	—	—	—	—
	(4) PD pin = "0"	—	—	—	—	—	—	—	—
	(5) CR setting	10	1	0	X	X	X	X	CR
DTMF Detect (High Speed)	(1) Detect timing setting	10	1	0	0	1	0	0	CR
	(2) STR monitoring (when not detected)	11	1	1	1	0	0	0	STR
	(3) STR monitoring (when detected)	11	1	1	0	0	0	1	STR
	(4) DTMF receive data reading	01	0	1	X	X	X	X	DTMFR
	(5) STR monitoring (when detected and after reading STR)	11	1	1	0	0	0	0	STR
	(6) STR monitoring (after making the input signal OFF)	11	1	1	1	0	0	0	STR
CPT Detect	(1) CPT detect enable setting	10	1	0	0	0	1	0	CR
	(2) STR monitoring (when not detected)	11	1	1	1	0	0	0	STR
	(3) STR monitoring (when detected)	11	1	1	1	0	1	1	STR
	(4) STR monitoring (when detected and after reading STR)	11	1	1	1	0	1	0	STR
DTMF Transmit	(1) DTMF transmit data setting	00	0	0	X	X	X	X	DTMFT
	(2) DTMF transmit ON	10	1	0	0	0	0	1	CR
	(3) Wait transmit ON time	—	—	—	—	—	—	—	—
	(4) DTMF transmit OFF	10	1	0	0	0	0	0	CR
	(5) Wait transmit OFF time	—	—	—	—	—	—	—	—
	(6) To transmit next data, return to (1)	—	—	—	—	—	—	—	—
CPT Transmit	(1) CPT transmit ON	10	1	0	1	0	0	0	CR
	(2) Wait transmit ON time	—	—	—	—	—	—	—	—
	(3) CPT transmit OFF	10	1	0	0	0	0	0	CR

APPLICATION CIRCUIT EXAMPLE

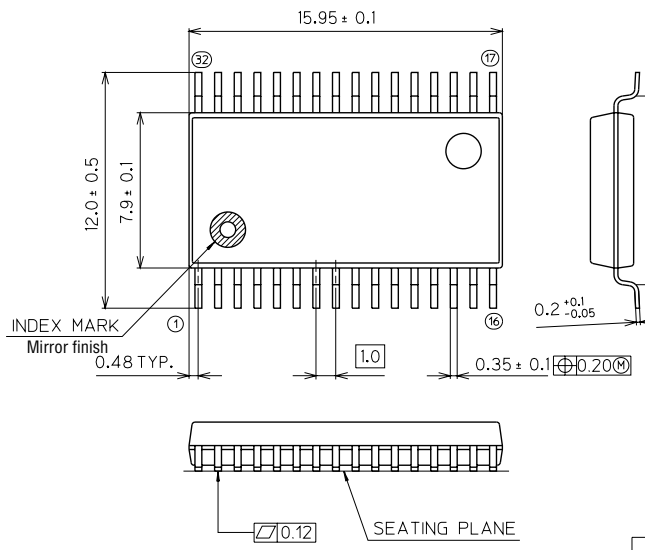


Note : ⏚ indicates connection to the SG pin.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.60 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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