Philips Semiconductors Product specification

Quad 2-input OR gate 查询"74AC32D"供应商

74AC32 **74ACT32**

FEATURES

- **DESCRIPTION** • 74ACT32 has TTL-compatible inputs
- 74AC32 has CMOS-compatible inputs
- Meets or exceeds JEDEC standard standard for 74AC(T)XX
- Superior ground bounce noise immunity
- Output source/sink 24mA

The 74AC32/74ACT32 provides the 2-input OR function.

QUICK REFERENCE DATA

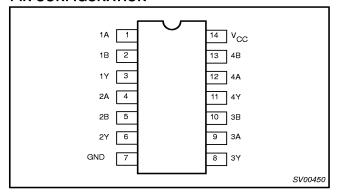
SYMBOL	PARAMETER	CONDITIONS	Α	С	ACT	UNIT
			V _{CC} = 3.3V	V _{CC} = 5.0V	V _{CC} = 5.0V	
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	C _L = 50pF	3.5	2.5	3.8	ns
CI	Input capacitance		4.5 V _{CC} ¹ 26			pF
C _{PD}	Power dissipation capacitance per gate	V _I = GND to V _{CC} ¹			28	pF

NOTE:

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER	
14-Pin Plastic SO	−40°C to +85°C	74AC32D 74ACT32D	74AC32D 74ACT32D	SOT108-1	
14-Pin Plastic SSOP Type II	−40°C to +85°C	74AC32DB 74ACT32DB	74AC32DB 74ACT32DB	SOT337-1	
14-Pin Plastic TSSOP Type I	−40°C to +85°C	74AC32PW 74ACT32PW	74AC32PW DH 74ACT32PW DH	SOT402-1	

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION			
1, 4, 9, 12	1A – 4A	Data inputs			
2, 5, 10, 13	1B – 4B	Data inputs			
3, 6, 8, 11	1Y – 4Y	Data outputs			
7	GND	Ground (0 V)			
14	V _{CC}	Positive supply voltage			

^{1.} C_{PD} is used to determine the dynamic power dissipation (P_D in μW): $\begin{array}{l} P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \; (C_L \times V_{CC}^2 \times f_o) \; \text{where:} \\ f_i = \text{input frequency in MHz;} \; C_L = \text{output load capacity in pF;} \\ f_o = \text{output frequency in MHz;} \; V_{CC} = \text{supply voltage in V;} \end{array}$

 $[\]Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}.$

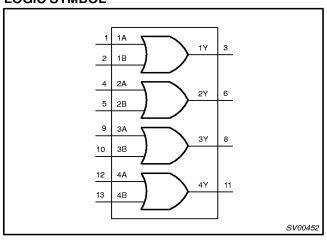
FUNCTION TABLE

INP	JTS	OUTPUTS		
nA	nA nB			
L	L	L		
L	Н	Н		
Н	L	Н		
Н	Н	Н		

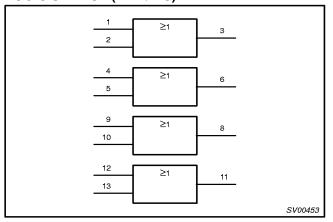
NOTES:

H = HIGH voltage level L = LOW voltage level

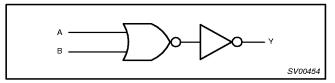
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	
Vaa	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	1 °
V _{IN}	DC input voltage range	0	V _{CC}	٧
Vo	DC output voltage range	0	V _{CC}	٧
T _{amb}	Operating free-air temperature range	-40	+85	°C
ΔV/Δt	Minimum input edge rate — AC devices V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V _{IN} from 0.8V to 2.0V V _{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS¹

in accordance with the Absolute Maximum Rating System (IEC134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
_	DO in and diede comment	V _{IN} = -0.5V	-20	0
liK	DC input diode current	$V_{IN} = V_{CC} + 0.5V$	+20	mA
V _{IN}	DC input voltage		-0.5 to V _{CC} +0.5	V
1	DC subsub die de sussessi	V _O = -0.5V	-20	0
loк	DC output diode current	$V_{O} = V_{CC} + 0.5V$	+20	mA
Vo	DC output voltage		-0.5 to V _{CC} +0.5	٧
lo	DC output source or sink current		±50	mA
	DC V _{CC} or GND current per output		±50	A
I _{CC} , I _{GND}	DC V _{CC} or GND current		±200	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
absolute-maximum-rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS FOR THE AC FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

					LIMITS		UNIT			
SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} (V)	Temp	= -40°C to	+85°C				
			``'	MIN	TYP	MAX				
			3.0	2.1	1.5					
V_{IH}	HIGH level Input voltage	$V_{OUT} = 0.1V \text{ or } (V_{CC} - 0.1V)$	4.5	3.15	2.25		V			
			5.5	3.85	2.75					
			3.0		1.5	0.9				
V _{IL}	LOW level Input voltage	$V_{OUT} = 0.1V \text{ or } (V_{CC} - 0.1V)$	4.5		2.25	1.35	V			
			5.5		2.75	1.65				
			3.0	2.9	2.99					
	HIGH level output voltage	I _{OUT} = -50 μA	4.5	4.4	4.49					
			5.5	5.4	5.49					
V _{OH}		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -12mA^1$	3.0	2.46						
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -24 \text{mA}^1$	4.5	3.76						
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -24 \text{mA}^1$	5.5	4.76						
			3.0		0.01	0.1				
		I _{OUT} = 50 μA	4.5		0.01	0.1				
M	LOW lovel autout valtage		5.5		0.01	0.1] ,			
V_{OL}	LOW level output voltage	$V_{IN} = V_{IL}$ or V_{IH} , $I_{OL} = 12mA^1$	3.0			0.44	7 °			
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OL} = 24mA^1$	4.5			0.44				
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OL} = 24 \text{mA}^1$	5.5			0.44				
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			±1.0	μΑ			
I _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA			
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			- 75	mA			
Icc	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μΑ			

NOTES:

^{1.} All outputs loaded

^{2.} Maximum test duration 2.0 ms; one output loaded at a time

DC CHARACTERISTICS FOR THE ACT FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

					LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	Temp	= -40°C to	+85°C	UNIT	
			, ,	MIN	TYP	MAX		
V	LICH level input voltage	V 0.1V or (V 0.1V)	4.5	2.0	1.5		V	
V _{IH}	HIGH level Input voltage	$V_{OUT} = 0.1V \text{ or } (V_{CC} - 0.1V)$	5.5	2.0	1.5] '	
V.	LOW level Input voltage	$V_{OLIT} = 0.1V \text{ or } (V_{CC} - 0.1V)$	4.5		1.5	0.8	V	
V _{IL} LOW level Input voltage	LOW level input voitage	VOUT = 0.1V OF (VCC - 0.1V)	5.5		1.5	0.8] '	
		504	4.5	4.4	4.49			
V _{OH} H		I _{OUT} = -50 μA	5.5	5.4	5.49			
	HIGH level output voltage	$V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -24 \text{mA}^1$	4.5	3.76			V	
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OH} = -24 \text{mA}^1$	5.5	4.76				
		504	4.5		0.01	0.1	-	
V	LOW lovel autout valtage	l _{OUT} = 50 μA	5.5		0.01	0.1		
V _{OL}	LOW level output voltage	$V_{IN} = V_{IL}$ or V_{IH} , $I_{OL} = 24 \text{mA}^1$	4.5			0.44	- V	
		$V_{IN} = V_{IL}$ or V_{IH} , $I_{OL} = 24 \text{mA}^1$	5.5			0.44		
I _{IN}	Input leakage current	V _{IN} = V _{CC} , GND	5.5			±1.0	μΑ	
Δl _{CC}	Additional quiescent supply current per input pin	$V_{IN} = V_{CC} - 2.1V$ Other inputs at V_{CC} or GND; $I_{OUT} = 0$	5.5			1.5	mA	
l _{OLD}	Dynamic output current ²	V _{OLD} = 1.65V max	5.5	75			mA	
I _{OHD}	Dynamic output current ²	V _{OHD} = 3.85V min	5.5			- 75	mA	
Icc	Quiescent supply current	V _{IN} = V _{CC} or GND	5.5			40	μΑ	

NOTES:

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All outputs loaded
 Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR 74AC32

GND = 0V; $t_r = t_f \le 2.5 ns;$ $C_L = 50 pF;$ $R_L = 500 \Omega;$.

					LIMITS					
SYMBOL	PARAMETER	V _{CC} ¹	T _{amb} = +25°C			T _{am} –40°C to	ь = o +85°C	UNIT	WAVEFORM	
			MIN	TYP	MAX	MIN	MAX]		
t _{PLH}	Propagation delay nA, nB to nY	3.3 5.0	2.0 1.5	3.6 2.5	8.0 5.5	1.5 1.0	9.0 6.0	ns	1, 2	
t _{PHL}	Propagation delay nA, nB to nY	3.3 5.0	2.0 1.5	3.5 2.6	8.0 5.5	1.5 1.0	9.0 6.0	ns	1, 2	

NOTE:

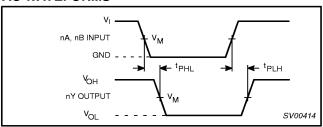
AC CHARACTERISTICS FOR 74ACT32

GND = 0V; t_{f} = t_{f} \leq 2.5ns; C_L = 50pF; R_L = 500 $\!\Omega$; .

					LIMITS				
SYMBOL	PARAMETER	V _{CC} 1	T _{amb} = +25°C			T _{am} –40°C to		UNIT	WAVEFORM
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay nA, nB to nY	5.0	2.0	4.2	9.0	1.5	10.0	ns	1, 2
t _{PHL}	Propagation delay nA, nB to nY	5.0	2.0	3.4	9.0	1.5	10.0	ns	1, 2

NOTE:

AC WAVEFORMS

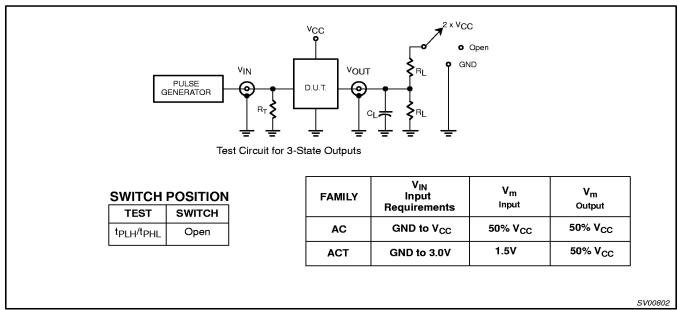


Waveform 1. Inputs (nA, nB) to output (nY) propagation delays

^{1.} Voltage range 3.3V is V_{CC} = 3.3V \pm 0.3V Voltage range 5.0V is V_{CC} = 5.0V \pm 0.5V

^{1.} Voltage range 5.0V is $V_{CC} = 5.0V \pm 0.5V$

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

DEFINITIONS

R_L = Load resistor; see AC Characteristics for value

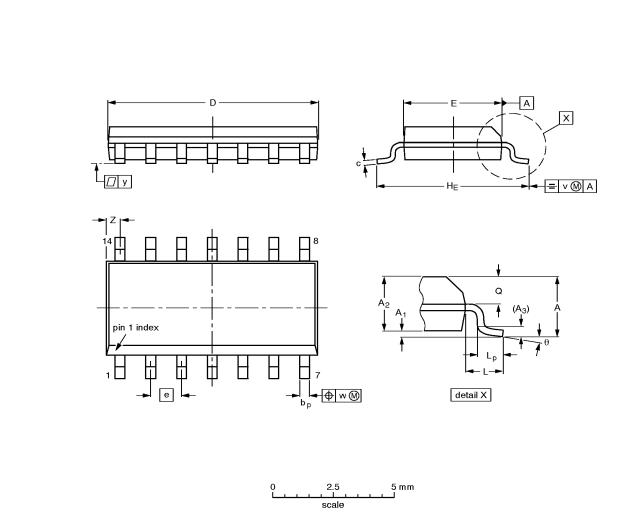
C_L = Load capacitance; see AC Characteristics

Termination resistance should be equal to Z_{OUT} of pulse generators

Quad 2-input OR gate 查询"74AC32D"供应商 74AC32 74ACT32

SO14: plastic small outline package; 14 leads; body width 3.9 mm





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

						OIII tile	·			,								
UNIT	A max.	A ₁	A ₂	A ₃	bp	c	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Ø	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	। ന നടവ	0.0098 0.0039		0.01		0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

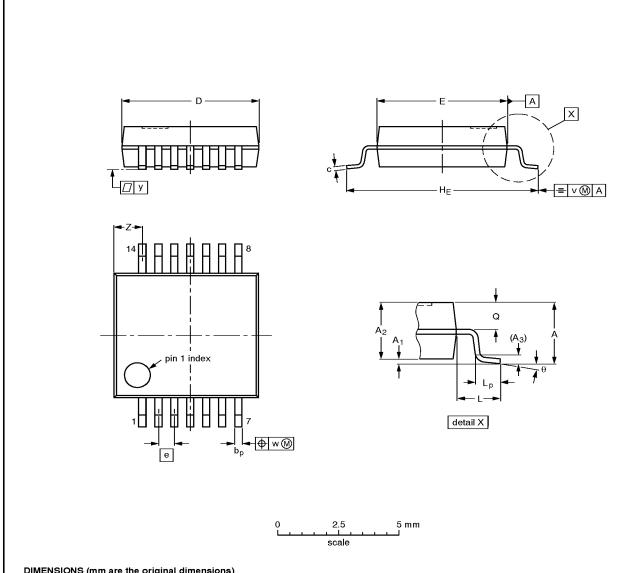
1	OUTLINE		REFER	EUROPEAN	ISSUE DATE	l		
	VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	١
	SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23	

Quad 2-input OR gate 查询"74AC32D"供应商

74AC32 74ACT32

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

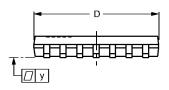
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

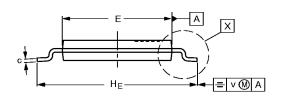
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT337-1		MO-150AB				-95-02-04 96-01-18	

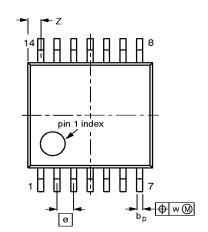
1997 Aug 22 10 Quad 2-input OR gate 查询"74AC32D"供应商 74AC32 74ACT32

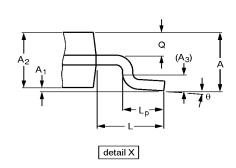
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

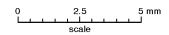
SOT402-1











DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	Аз	bр	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Ø	ν	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1990E DATE	
SOT402-1		MO-153				-94-07-12 95-04-04	

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