

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.090 at $V_{GS} = - 4.5$ V	- 4 ^c	3.8 nC
	0.180 at $V_{GS} = - 2.5$ V	- 4 ^c	

FEATURES

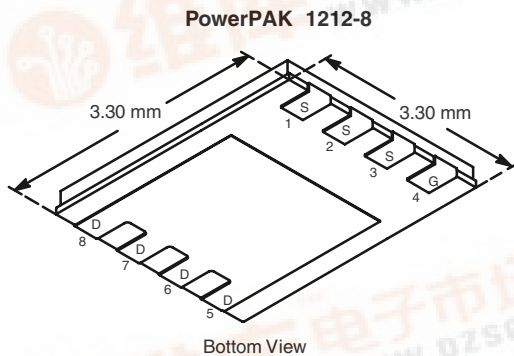
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET: 2.5 V Rated
- PowerPAK® Package
 - Low Thermal Resistance
 - Low 1.07 mm Profile
- 100 R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

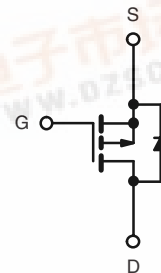
APPLICATIONS

- Load Switching
- HDD



Bottom View

Ordering Information: Si7621DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150$ °C) ^{a, b}	$T_C = 25$ °C	- 4 ^c	A
	$T_C = 70$ °C	- 4 ^c	
	$T_A = 25$ °C	- 4 ^{a, b, c}	
	$T_A = 70$ °C	- 3.8 ^{a, b}	
Pulsed Drain Current	I_{DM}	- 15	
Continuous Source-Drain Diode Current ^{a, b}	$T_C = 25$ °C	- 4 ^c	
	$T_A = 25$ °C	- 2.6 ^{a, b}	
Maximum Power Dissipation ^{a, b}	$T_C = 25$ °C	12.5	W
	$T_C = 70$ °C	8	
	$T_A = 25$ °C	3.1 ^{a, b}	
	$T_A = 70$ °C	2 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t = 10$ s.

c. Package limited.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	8	10	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 81 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 15.1		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.7		- 2	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3.9 A		0.074	0.090	Ω
		V _{GS} = - 2.5 V, I _D = - 2.9 A		0.150	0.180	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 3.9 A		8.2		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		300		pF
Output Capacitance	C _{oss}			95		
Reverse Transfer Capacitance	C _{rss}			65		
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 5 V, I _D = - 3.9 A		4.1	6.2	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 3.9 A		3.9	5.9	
Gate-Source Charge	Q _{gs}			0.7		
Gate-Drain Charge	Q _{gd}			1.25		
Gate Resistance	R _g	f = 1 MHz	1.6	8	16	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 3.2 Ω I _D ≅ - 3.1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		8	12	ns
Rise Time	t _r			75	113	
Turn-Off Delay Time	t _{d(off)}			25	38	
Fall Time	t _f			60	90	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 4	A
Pulse Diode Forward Current	I _{SM}				- 15	
Body Diode Voltage	V _{SD}	I _S = - 1.5 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 1.5 A, dI/dt = 100 A/μs, T _J = 25 °C		18	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}			10	15	nC
Reverse Recovery Fall Time	t _a			14		ns
Reverse Recovery Rise Time	t _b			4		

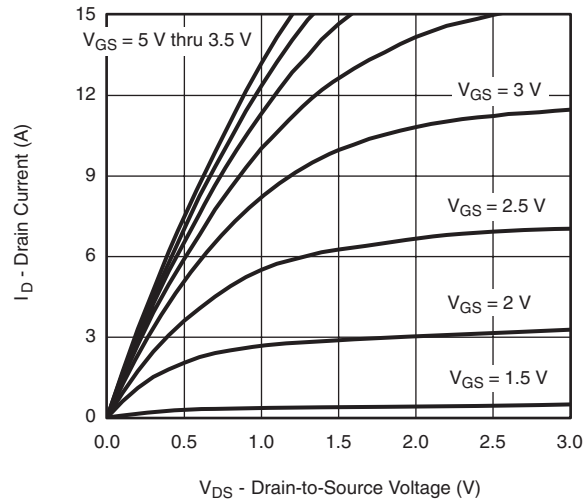
Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

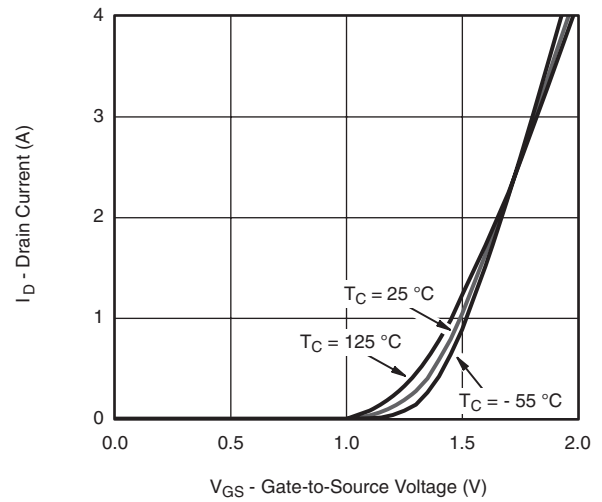
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

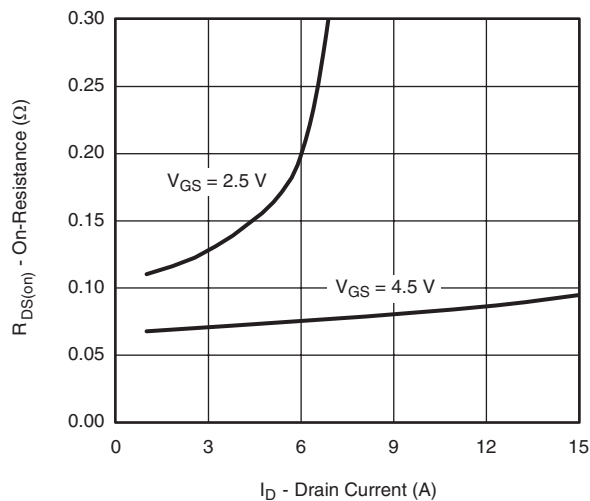
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



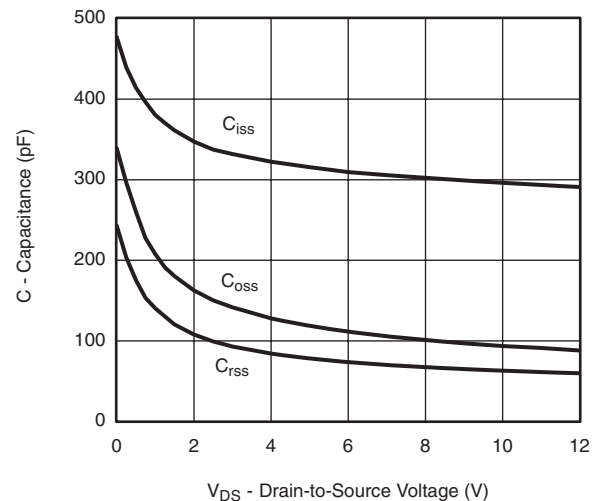
Output Characteristics



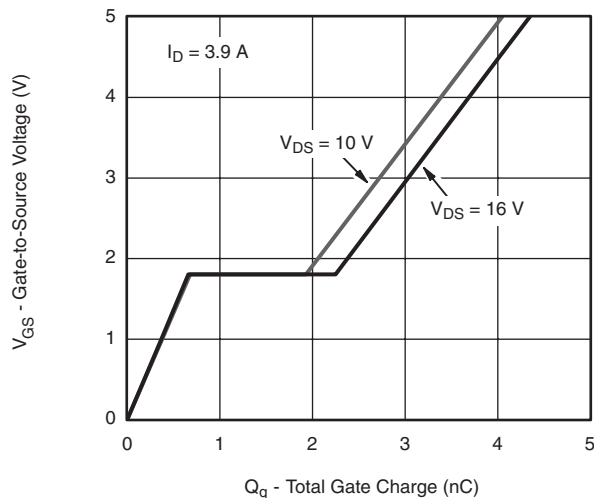
Transfer Characteristics



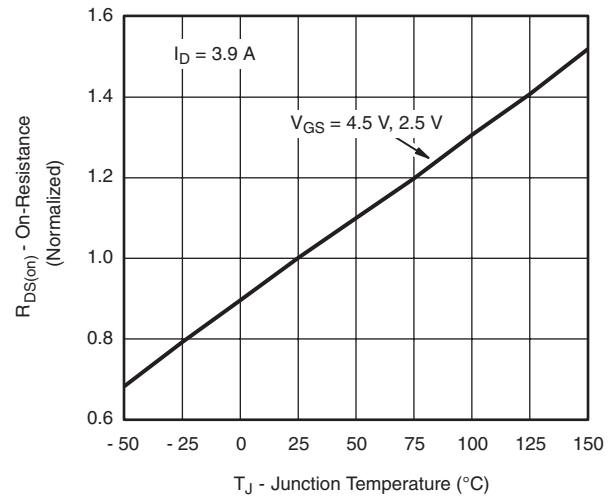
On-Resistance vs. Drain Current and Gate Voltage



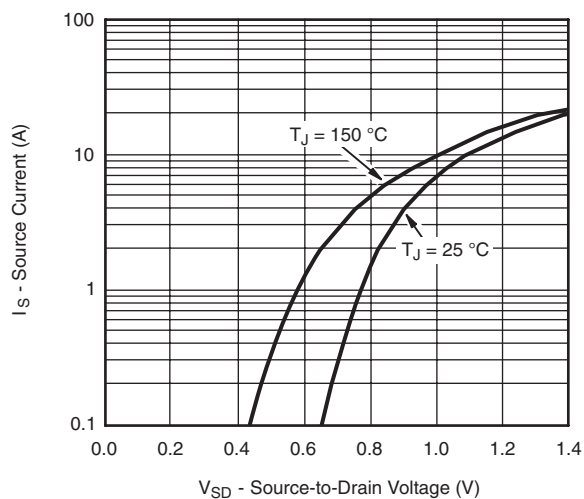
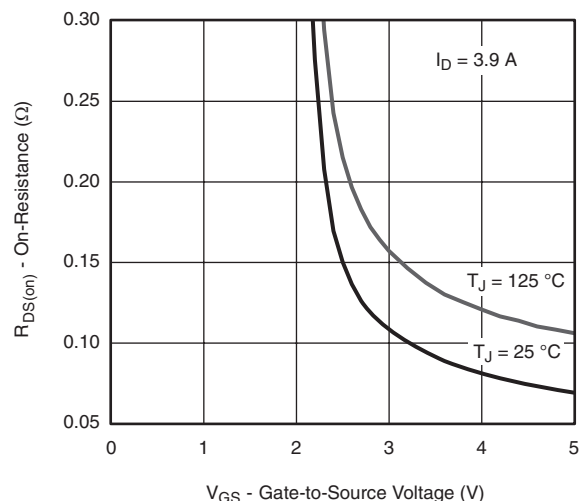
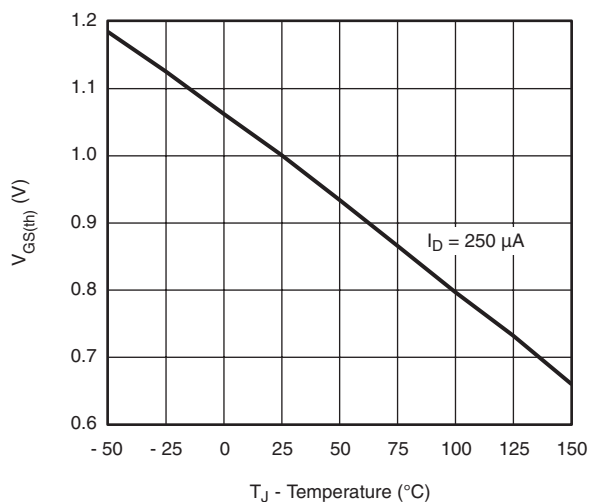
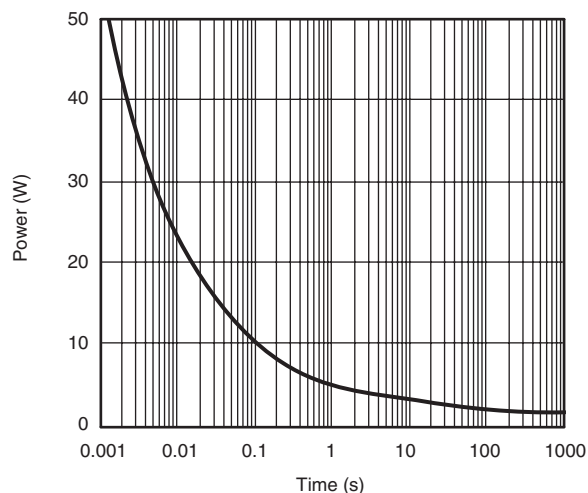
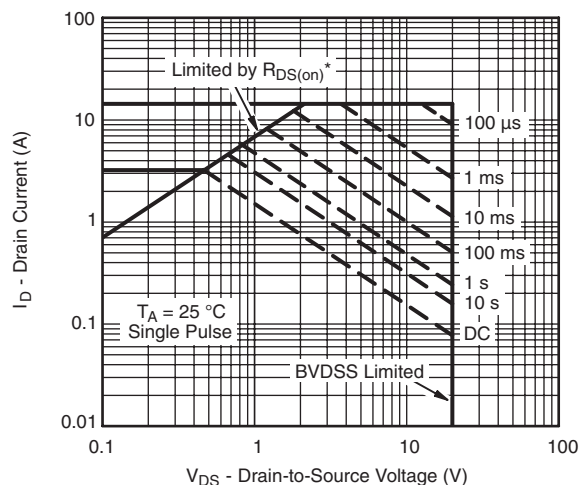
Capacitance



Gate Charge



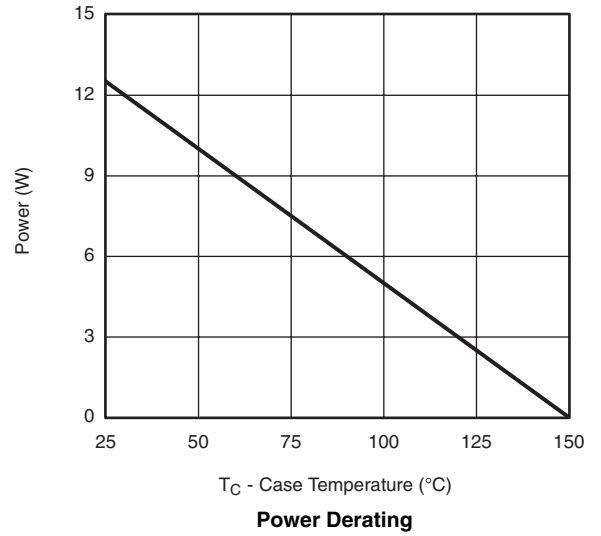
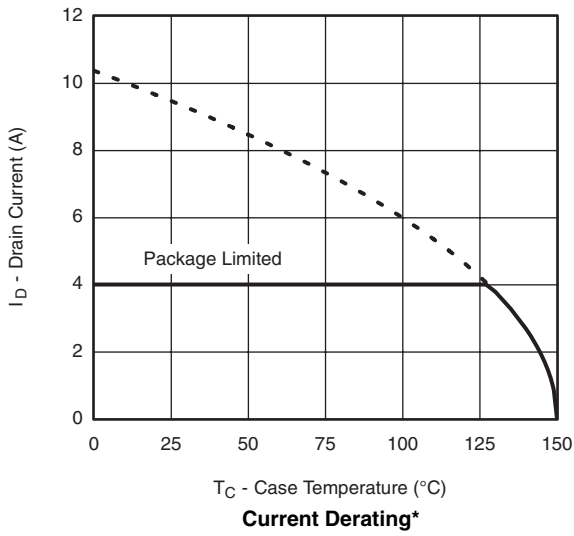
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


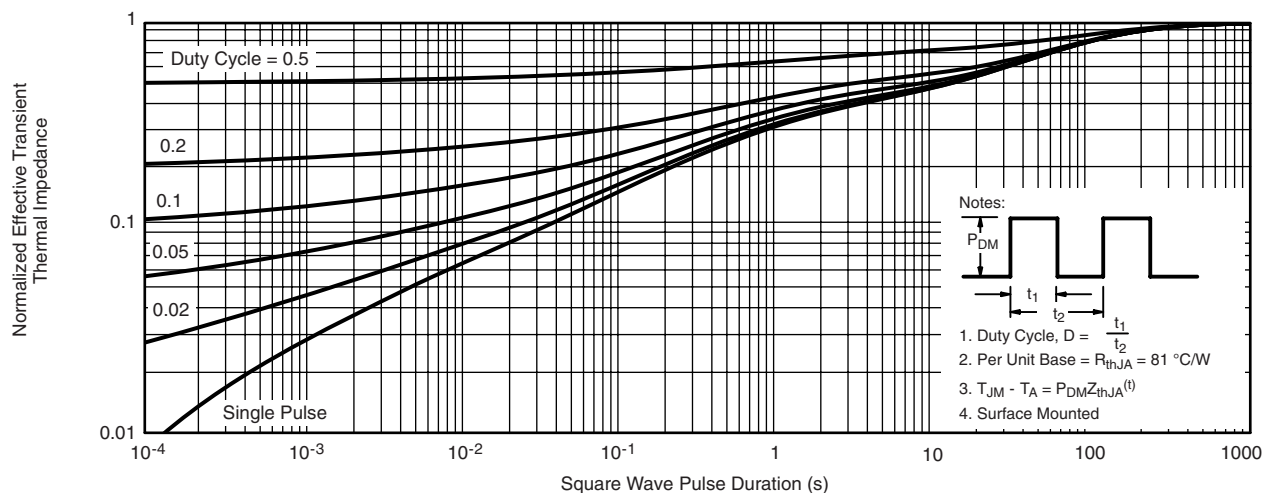
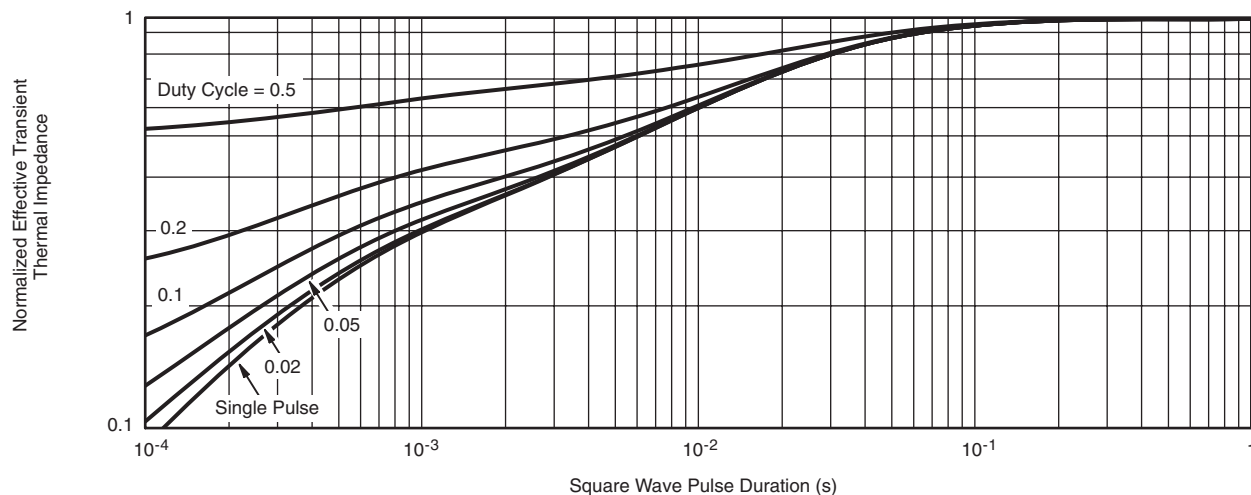
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65544.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.