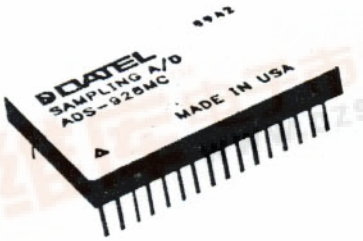
DATEL
INNOVATION and EXCELLENCE

ADS-928
500kHz, 14-Bit Sampling A/D Converter

FEATURES

- 14-Bit resolution
- 500kHz sampling rate
- Functionally complete
- Small 32-pin DIP
- Low-power, 3.1 Watts
- Excellent dynamic performance
- Samples up to Nyquist



GENERAL DESCRIPTION

DATEL's ADS-928 is a 14-bit, 500kHz sampling rate, functionally complete A/D converter. The ADS-928 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15V and +5V with 3.1 Watts power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	GAIN ADJUST	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	COMP BIN	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V SUPPLY	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V SUPPLY	28	BIT 3 OUT
13	−15V SUPPLY	29	BIT 2 OUT
14	NO CONNECTION	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT

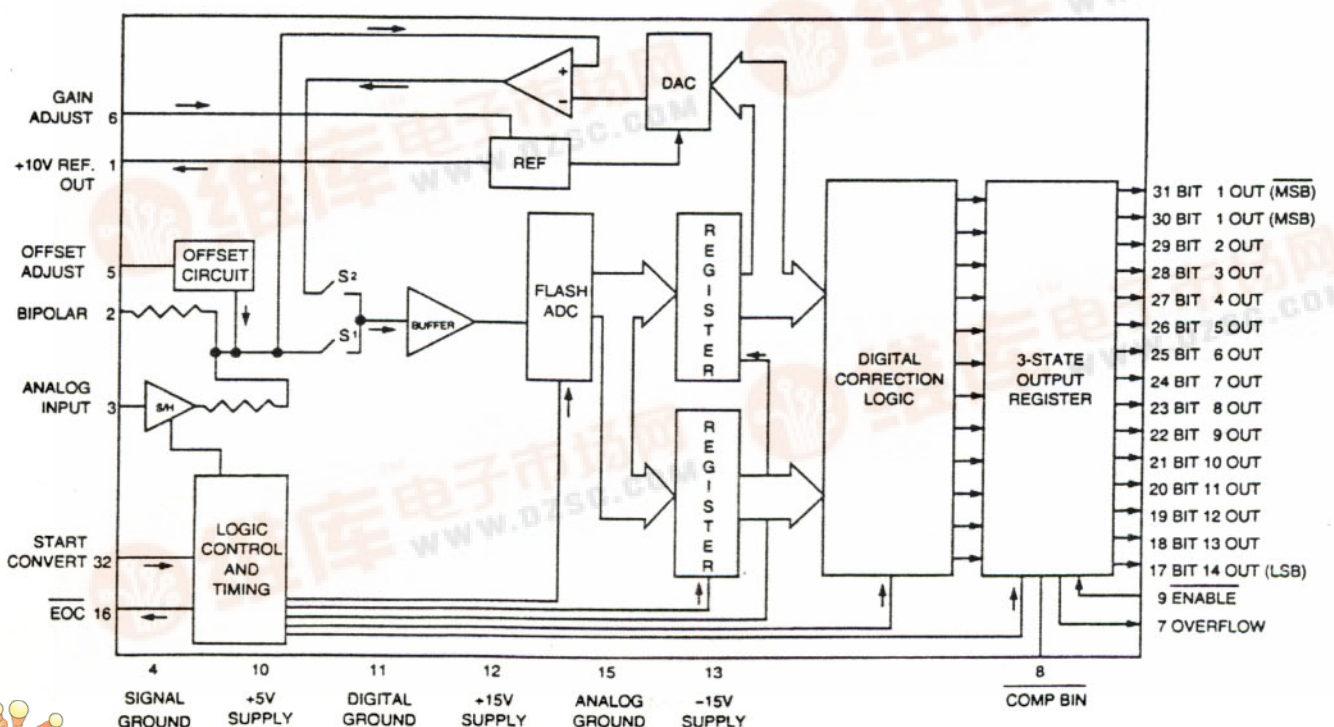


Figure 1. ADS-928 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	0 to +16	Volts
–15V Supply (Pin 13)	0 to –16	Volts
+5V Supply (Pin 10)	0 to +6	Volts
Digital Inputs (Pins 8, 9, 32)	–0.3 to +7.0	Volts
Analog Input (Pin 3)	–7.5 to +12.5	Volts
Lead Temp. (10 sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

T_A = +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, 500kHz sampling rate, and 5 minute warmup unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	–	0 to -10	–	Volts
	–	±5	–	Volts
Input Impedance	4.9	5	–	kOhms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0	–	–	Volts
Logic "0"	–	–	+0.8	Volts
Logic Loading "1"	–	–	+20	µA
Logic Loading "0"	–	–	–20	µA
PERFORMANCE				
nt. Non-Lin. @ f_{IN} = 10kHz				
+25°C	–	±1/2	±2	LSB
0 to +70°C	–	±1	±2	LSB
–55 to +125°C	–	±1	±3	LSB
Diff. Non-Lin. @ f_{IN} = 10kHz				
+25°C	–	±1/2	±0.85	LSB
0 to +70°C	–	±1/2	±0.95	LSB
–55 to +125°C	–	±3/4	±2	LSB
Full Scale Absolute Accuracy				
+25°C	–	±0.08	±0.18	%FSR
0 to +70°C	–	±0.2	±0.6	%FSR
–55 to +125°C	–	±0.4	±0.8	%FSR
Unipolar Zero Error,				
+25°C	–	±0.1	±0.15	%FSR
0 to +70°C	–	±0.1	±0.2	%FSR
–55 to +125°C	–	±0.2	±0.3	%FSR
Bipolar Zero Error,				
+25°C (Tech Note 1)	–	±0.1	±0.15	%FSR
0 to +70°C	–	±0.1	±0.25	%FSR
–55 to +125°C	–	±0.25	±0.5	%FSR
Bipolar Offset Error,				
+25°C (Tech Note 1)	–	±0.05	±0.1	%FSR
0 to +70°C	–	±0.1	±0.25	%FSR
–55 to +125°C	–	±0.25	±0.45	%FSR
Gain Error, +25°C (See Tech Note 1)	–	±0.1	±0.15	%
0 to +70°C	–	±0.15	±0.45	%
–55 to +125°C	–	±0.25	±0.75	%
No Missing Codes	0 to +70°C			
14 Bits	–55 to +125°C			
13 Bits	14 Bits			
Resolution				
Output Coding	Straight bin./offset bin./2's Comp.			
(Pin 8 Hi)	Comp. bin./Comp. offset bin., C2C			
(Pin 8 Low)				

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	+2.4	–	–	Volts
Logic "0"	–	–	0.4	Volts
Logic Loading "1"	–	–	–4	mA
Logic Loading "0"	–	–	+4	mA
Internal Reference Voltage, +25°C	+9.98	+10.0	+10.02	Volts
Drift	–	±30	–	ppm/ °C
External Current	–	–	2	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (-0.5dB)				
DC to 100kHz	–	–90	–83	dB
100kHz to 250kHz	–	–82	–77	dB
Signal-to-Noise Ratio (w/o distortion, -0.5dB)				
DC to 100kHz	78	83	–	dB
100kHz to 250kHz	74	77	–	dB
Signal-to-Noise Ratio & distortion, -0.5dB				
DC to 100kHz	77	80	–	dB
100kHz to 250kHz	72	76	–	dB
Two-tone Intermodulation Distortion (f_{IN} = 100kHz, 240kHz, Fs=500kHz, -0.5dB)	–	80	–	dB
Input Bandwidth (–3dB)				
Small Signal (–20dB input)	6	–	–	MHz
Large Signal (0.5dB input)	1.75	–	–	MHz
Feedthrough Rejection @ f_{IN} = 250kHz	–	90	–	dB
Slew Rate	–	±90	–	V/µs
Aperture Delay Time	–	±20	–	ns
Aperture Uncertainty	–	50	–	ps rms
S/H Acquisition Time (to 0.003%FS (10V step)	–	680	750	ns
Overvoltage Recovery, ±12V	–	600	1000	ns
A/D Conversion Rate	500	–	–	kHz
POWER REQUIREMENTS				
Power Supply Range				
+15V Supply	+14.5	+15.0	+15.5	Volts
-15V Supply	–14.5	–15.0	–15.5	Volts
+5V Supply	+4.75	+5.0	+5.0	Volts
Power Supply Current				
+15V Supply	–	+78	+90	mA
-15V Supply	–	–65	–75	mA
+5V Supply ①	–	+68	+78	mA
Power Dissipation	–	2.5	2.8	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range -MC	0	–	+70	°C
-MM	–55	–	+125	°C
Storage Temperature Range	–65	–	+150	°C
Package Type	32-pin hermetic sealed, ceramic TDIP			
Weight	0.42 ounces (12 grams)			

① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulse) must be present during warm up period.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to -10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20k trimming potentiometer for gain adjustment with the wiper tied to pin 6 (ground pin 6 for operation without adjustments). Use a 20k trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (connect pin 5 to pin 15, analog ground for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 8) to +5V or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect ENABLE (pin 9) to a logic "1" (high).

6. The 200 ns minimum START CONVERT pulse width assures the hold mode settling time requirements are met.

7. The specifications listed in Figure 2 (timing diagram) apply over the full operating temperature range unless otherwise specified.

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
0 to -10V	-305 µV	-9.999085V
±5V	-305 µV	-4.999085V

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 32) at a rate of 200kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and signal ground (pin 4). Adjust the output of the reference source per Table 2.

   For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 8) tied high (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with the pin 8 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied low (complementary offset binary).

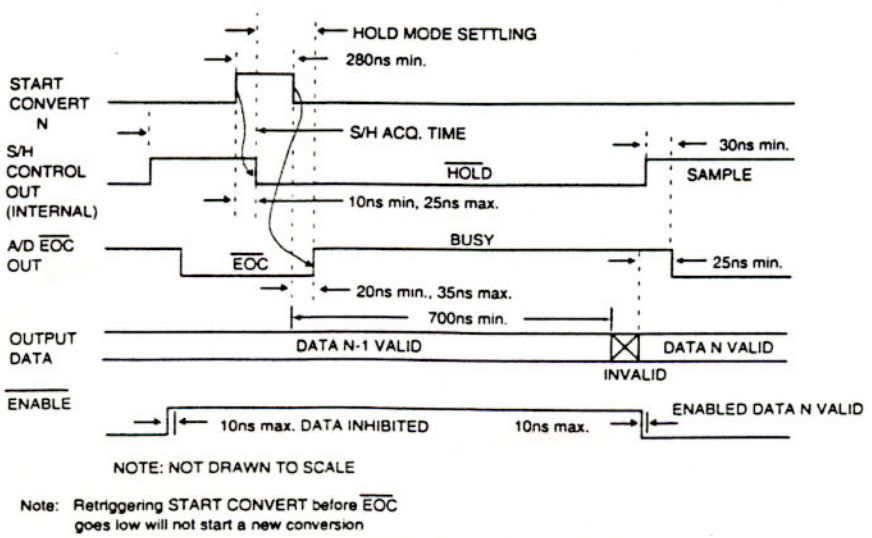
   Two's complement coding requires use of the MSB (pin 31) with pin 8 tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 for pin 8 tied high (straight binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 for pin 8 tied low (complementary binary).

   Two's complement coding requires use of the MSB (pin 31) with the pin 8 tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.



NOTE: NOT DRAWN TO SCALE

Note: Retriggering START CONVERT before $\overline{\text{EOC}}$ goes low will not start a new conversion

Figure 2.
ADS-928 Timing Diagram

Table 3. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES, V dc 0 to -10V	OUTPUT CODING STRAIGHT BIN. MSB	LSB	COMP. BINARY MSB	LSB	COMP. BINARY MSB	LSB	INPUT RANGE ±5V dc	BI POLAR SCALE
FS -1 LSB	-9.999390	11	1111 1111 1111	00	0000 0000 0000	01	1111 1111 1111	-4.99939	+FS -1 LSB
7/8 FS	-8.750000	11	1000 0000 0000	00	0111 1111 1111	01	1000 0000 0000	-3.75000	+3/4 FS
3/4 FS	-7.500000	11	0000 0000 0000	00	1111 1111 1111	01	0000 0000 0000	-2.50000	+1/2 FS
1/2 FS	-5.000000	10	0000 0000 0000	01	1111 1111 1111	00	0000 0000 0000	0.00000	0
1/4 FS	-2.500000	01	0000 0000 0000	10	1111 1111 1111	10	0000 0000 0000	+2.50000	-1/2 FS
1/8 FS	-1.250000	00	1000 0000 0000	11	0111 1111 1111	10	1000 0000 0000	+3.75000	-3/4 FS
1 LSB	-0.000610	00	0000 0000 0001	11	1111 1111 1110	10	0000 0000 0001	+4.99939	-FS +1 LSB
0	0.000000	00	0000 0000 0000	11	1111 1111 1111	10	00000000 0000	+5.00000	-FS
		OFF. BINARY		COMP. OFF. BIN.					

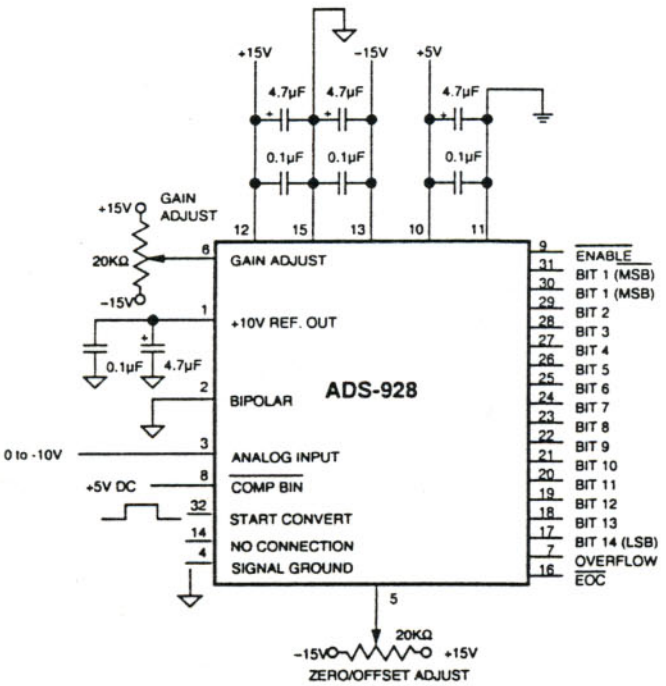
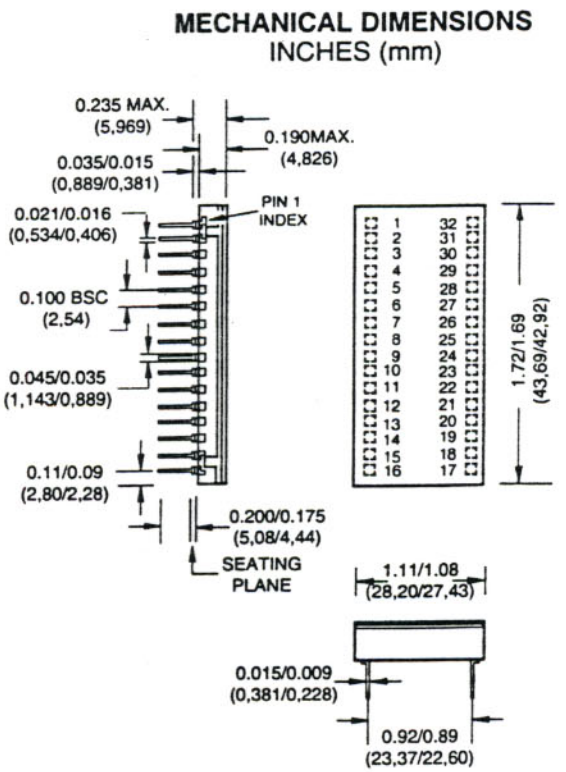


Figure 3. Typical ADS-928 Connection Diagram



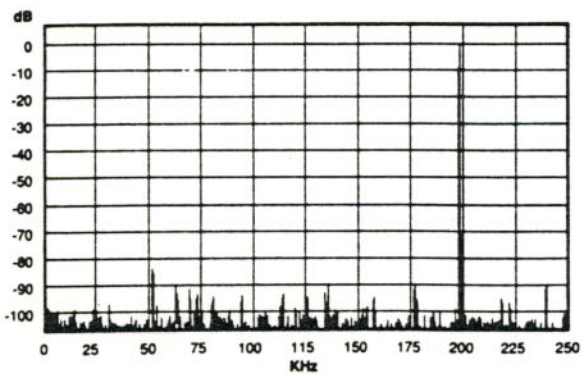


Figure 4. FFT Analysis of ADS-928

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-928MC	0 to +70°C	Hermetic
ADS-928MM	–55 to +125°C	Hermetic
ADS-EVAL1	Evaluation Board (without ADS-928)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For availibility of MIL-STD-883B versions, contact DATEL.

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