ADVANCED INFORMATION

MX28F640C3T/B

64M-BIT [4M x16] CMOS SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

- Bit Organization: 4,194,304 x 16
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
  - VCC=VCCQ=2.7~3.6V
  - Operating temperature:-40℃~85℃
- Fast access time : 90/120ns
- Low power consumption
  - 9mA maximum active read current, f=5MHz (CMOS input)
  - 21mA program erase current maximum (VPP=1.65~3.6V)
  - 7uA typical standby current under power saving mode
- Sector architecture
  - Sector Erase (Sector structure : 4Kword x 2 (boot sectors), 4Kword x 6 (parameter sectors), 32Kword x 127 (parameter sectors)
  - Top/Bottom Boot
- Auto Erase (chip & sector) and Auto Program
  - Automatically program and verify data at specified address
- Automatic Suspend Enhance
  - Word write suspend to read
  - Sector erase suspend to word write
  - Sector erase suspend to read register report
- Automatic sector erase, full chip erase, word write and sector lock/unlock configuration
- Status Reply
  - Detection of program and erase operation completion.
  - Command User Interface (CUI)
  - Status Register (SR)
- Data Protection Performance
  - Include boot sectors and parameter and main sectors to be block/unblock
- 100,000 minimum erase/program cycles
- Common Flash Interface (CFI)
- 128-bit Protection Register
  - 64-bit Unique Device Identifier
  - 64-bit User-Programmable
- Latch-up protected to 100mA from -1V to VCC+1V
- Package type:
  - 48-pin TSOP (12mm x 20mm)
  - 48-ball CSP (11mm x 12mm)

GENERAL DESCRIPTION

The MX28F640C3T/B is a 64-mega bit Flash memory organized as 4M words of 16 bits. The 1M word of data is arranged in eight 4Kword boot and parameter sectors, and 127 32Kword main sector which are individually erasable. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F640C3T/B is packaged in 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX28F640C3T/B offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F640C3T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming

mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX28F640C3T/B uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

The dedicated VPP pin gives complete data protection when VPP< VPPLK.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for erase, full chip erase, word write and sector lock/unlock configuration operations.

A sector erase operation erases one of the device's 32K-word sectors typically within 1.0s, 4K-word sectors typically within 0.5s independent of other sectors. Each sector can be independently erased minimum 100,000 times. Sector erase suspend mode allows system software to suspend sector erase to read or write data from any other sector.

Writing memory data is performed in word increments of the device's 32K-word sectors typically within 0.8s and 4K-word sectors typically within 0.1s. Word program suspend mode enables the system to read data or execute code from any other memory array location.

MX28F640C3T/B features with individual sectors locking by using a combination of bits thirty-nine sector lockbits and $\overline{WP}$, to lock and unlock sectors.

The status register indicates when the WSM's sector erase, full chip erase, word program or lock configuration operation is done.

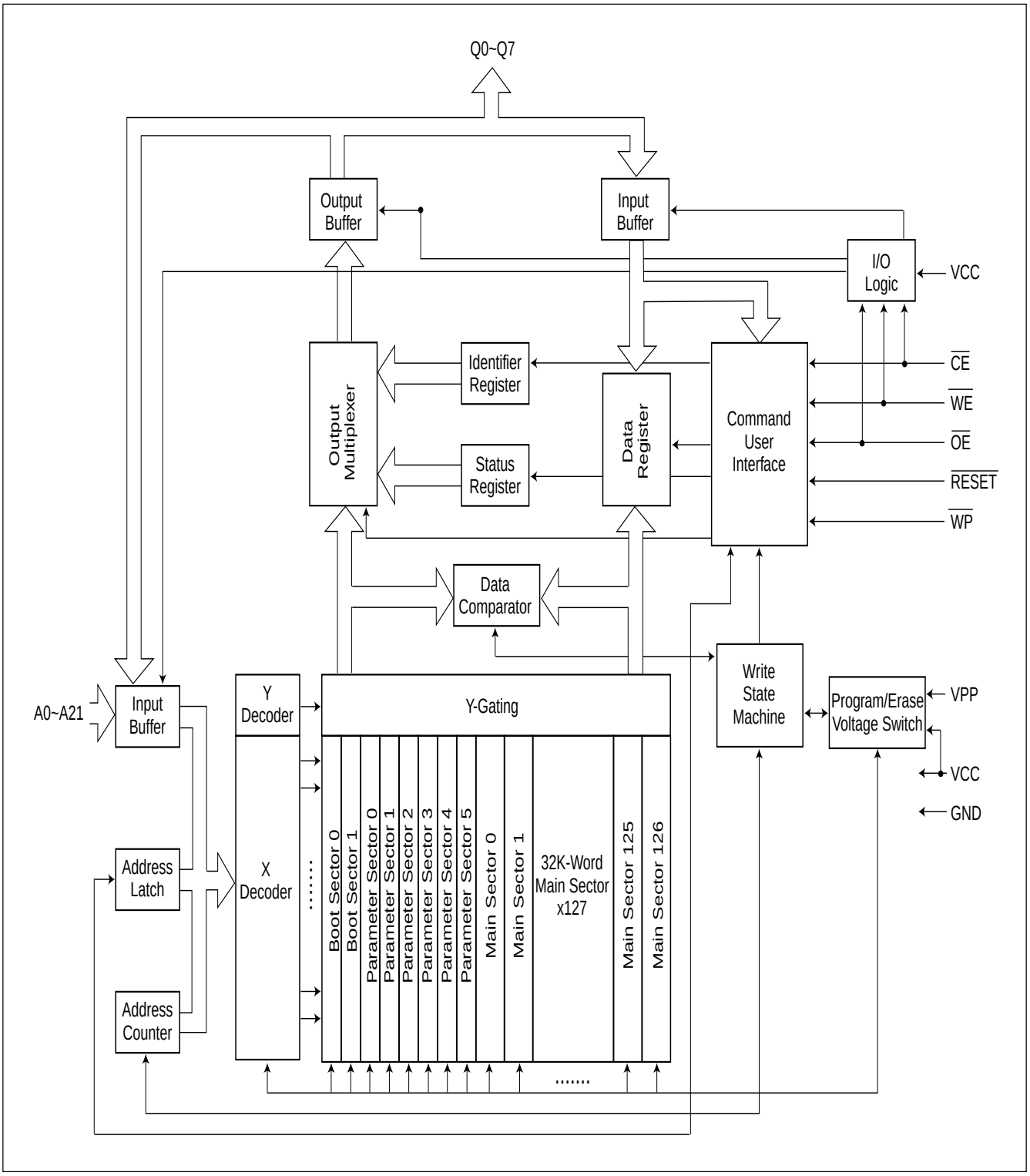
The access time is 90/120ns (tELQV) over the operating temperature range (-40℃ to +80℃) and VCC supply voltage range of 2.7V~3.6V.

MX28F640C3T/B's power saving mode feature substantially reduces active current when the device is in static mode (addresses not switching). In this mode, the typical ICCS current is 7uA (CMOS) at 3.0V VCC.

As $\overline{CE}$ and $\overline{RESET}$ are at VCC, ICC CMOS standby mode is enabled. When $\overline{RESET}$ is at GND, the reset mode is enabled which minimize power consumption and provide data write protection.

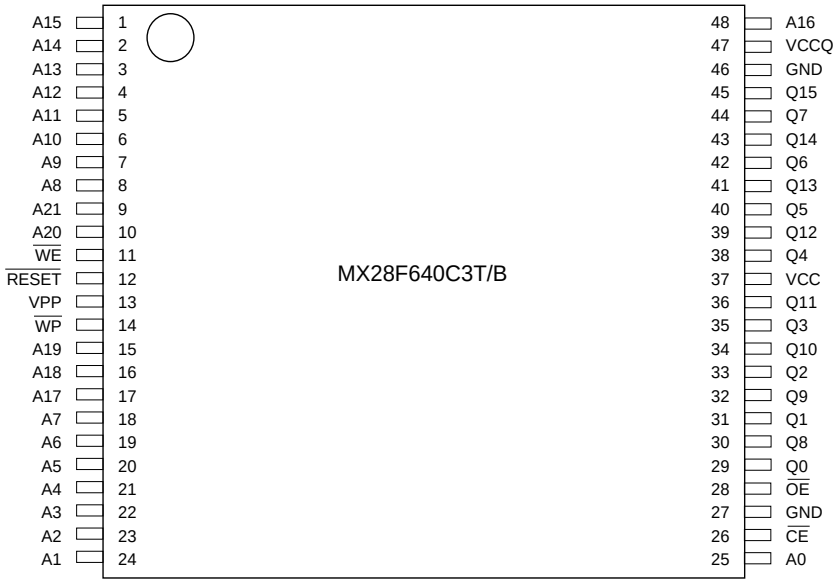
A reset time (tPHQV) is required from $\overline{RESET}$ switching high until outputs are valid. Similarly, the device has a wake time (tPHEL) from $\overline{RESET}$-high until writes to the CUI are recognized. With $\overline{RESET}$ at GND, the WSM is reset and the status register is cleared.

BLOCK DIAGRAM



PIN CONFIGURATIONS

48 TSOP (Standard Type) (12mm x 20mm)



48 Ball CSP (11 mm x 12 mm) Top View, Ball Down (Ball Pitch=0.75mm, Ball Width=0.35mm)

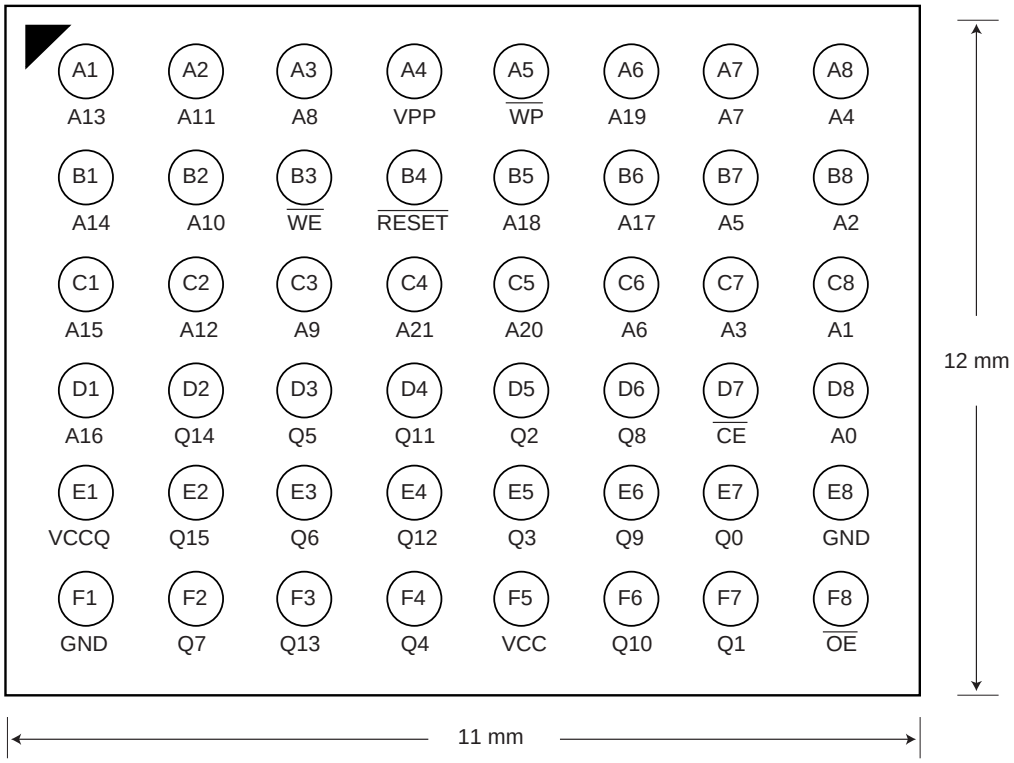


Table 1. Pin Description

Symbol	Type	Description and Function
A0-A21	input	Address inputs for memory address. Data pin float to high-impedance when the chip is deselected or outputs are disable. Addresses are internally latched during a write or erase cycle.
Q0-Q15	input/output	Data inputs/outputs: Inputs array data on the second $\overline{CE}$ and $\overline{WE}$ cycle during a program command. Data is internally latched. Outputs array and configuration data. The data pin float to tri-state when the chip is de-selected.
$\overline{CE}$	input	Activates the device's control logic, input buffers, and sense amplifiers. $\overline{CE}$ high deselects the memory device and reduce power consumption to standby level. $\overline{CE}$ is active low.
$\overline{RESET}$	input	Reset Deep Power Down: when $\overline{RESET}$=VIL, the device is in reset/deep power down mode, which drives the outputs to High Z, resets the WSM and minimizes current level. When $\overline{RESET}$=VIH, the device is normal operation. When $\overline{RESET}$ transition the device defaults to the read array mode.
$\overline{WE}$	input	Write Enable: to control write to CUI and array sector. $\overline{WR}$=VIL becomes active. The data and address is latched $\overline{WE}$ on the rising edge of the second $\overline{WE}$ pulse.
VPP	input/supply	Program/Erase Power Supply:(1.65V~3.6V) Lower VPP≤VPPLK, to protect any contents against Program and Erase Command. Set VPP=VCC for in-system Read, Program and Erase Operation.
$\overline{OE}$	input	Output enable: gates the device's outputs during a real cycle.
$\overline{WP}$	input	Write protect: when $\overline{WP}$ is VIL, the boot sectors cannot be written or erased. When $\overline{WP}$ is VIH, locked boot sectors cannot be written or erase. $\overline{WP}$ is not affected parameter and main sectors.
VCC	supply	Device power supply: (2.7V~3.6V).
VCCQ	input	I/O Power Supply: supplies for input/output buffers. [2.7V~3.6V] This input should be tied directly to VCC.
GND	supply	Ground voltage: all the GND pin shall not be connected.

SECTOR STRUCTURE (TOP)

Sector	Sector Size	Address Range (h)
Boot Sector 0	4K Word	3FF000-3FFFFF
Boot Sector 1	4K Word	3FE000-3FEFFF
Parameter Sector 0	4K Word	3FD000-3FDFFF
Parameter Sector 1	4K Word	3FC000-3FCFFF
Parameter Sector 2	4K Word	3FB000-3FBFFF
Parameter Sector 3	4K Word	3FA000-3FAFFF
Parameter Sector 4	4K Word	3F9000-3F9FFF
Parameter Sector 5	4K Word	3F8000-3F8FFF
Main Sector 0	32K Word	3F0000-3F7FFF
Main Sector 1	32K Word	3E8000-3EFFFF
Main Sector 2	32K Word	3E0000-3E7FFF
Main Sector 3	32K Word	3D8000-3DFFFF
Main Sector 4	32K Word	3D0000-3D7FFF
Main Sector 5	32K Word	3C8000-3CFFFF
Main Sector 6	32K Word	3C0000-3C7FFF
Main Sector 7	32K Word	3B8000-3BFFFF
Main Sector 8	32K Word	3B0000-3B7FFF
Main Sector 9	32K Word	3A8000-3AFFFF
Main Sector 10	32K Word	3A0000-3A7FFF
Main Sector 11	32K Word	398000-39FFFF
Main Sector 12	32K Word	390000-397FFF
Main Sector 13	32K Word	388000-38FFFF
Main Sector 14	32K Word	380000-387FFF
Main Sector 15	32K Word	378000-37FFFF
Main Sector 16	32K Word	370000-377FFF
Main Sector 17	32K Word	368000-36FFFF
Main Sector 18	32K Word	360000-367FFF
Main Sector 19	32K Word	358000-35FFFF
Main Sector 20	32K Word	350000-357FFF
Main Sector 21	32K Word	348000-34FFFF
Main Sector 22	32K Word	340000-347FFF
Main Sector 23	32K Word	338000-33FFFF
Main Sector 24	32K Word	330000-337FFF
Main Sector 25	32K Word	328000-32FFFF
Main Sector 26	32K Word	320000-327FFF
Main Sector 27	32K Word	318000-31FFFF
Main Sector 28	32K Word	310000-317FFF
Main Sector 29	32K Word	308000-30FFFF
Main Sector 30	32K Word	300000-307FFF
Main Sector 31	32K Word	2F8000-2FFFFF
Main Sector 32	32K Word	2F0000-2F7FFF
Main Sector 33	32K Word	2E8000-2EFFFF
Main Sector 34	32K Word	2E0000-2E7FFF
Main Sector 35	32K Word	2D8000-2DFFFF
Main Sector 36	32K Word	2D0000-2D7FFF
Main Sector 37	32K Word	2C8000-2CFFFF
Main Sector 38	32K Word	2C0000-2C7FFF
Main Sector 39	32K Word	2B8000-2BFFFF
Main Sector 40	32K Word	2B0000-2B7FFF
Main Sector 41	32K Word	2A8000-2AFFFF
Main Sector 42	32K Word	2A0000-2A7FFF
Main Sector 43	32K Word	298000-29FFFF
Main Sector 44	32K Word	290000-297FFF
Main Sector 45	32K Word	288000-28FFFF
Main Sector 46	32K Word	280000-287FFF
Main Sector 47	32K Word	278000-27FFFF
Main Sector 48	32K Word	270000-277FFF
Main Sector 49	32K Word	268000-26FFFF
Main Sector 50	32K Word	260000-267FFF
Main Sector 51	32K Word	258000-25FFFF
Main Sector 52	32K Word	250000-257FFF
Main Sector 53	32K Word	248000-24FFFF
Main Sector 54	32K Word	240000-247FFF
Main Sector 55	32K Word	238000-23FFFF
Main Sector 56	32K Word	230000-237FFF
Main Sector 57	32K Word	228000-22FFFF
Main Sector 58	32K Word	220000-227FFF
Main Sector 59	32K Word	218000-21FFFF
Main Sector 60	32K Word	210000-217FFF
Main Sector 61	32K Word	208000-20FFFF
Main Sector 62	32K Word	200000-207FFF
Main Sector 63	32K Word	1F8000-1FFFFF
Main Sector 64	32K Word	1F0000-1F7FFF
Main Sector 65	32K Word	1E8000-1EFFFF
Main Sector 66	32K Word	1E0000-1E7FFF
Main Sector 67	32K Word	1D8000-1DFFFF
Main Sector 68	32K Word	1D0000-1D7FFF
Main Sector 69	32K Word	1C8000-1CFFFF
Main Sector 70	32K Word	1C0000-1C7FFF

Sector	Sector Size	Address Range (h)
Main Sector 71	32K Word	1B8000-1BFFFF
Main Sector 72	32K Word	1B0000-1B7FFF
Main Sector 73	32K Word	1A8000-1AFFFF
Main Sector 74	32K Word	1A0000-1A7FFF
Main Sector 75	32K Word	198000-19FFFF
Main Sector 76	32K Word	190000-197FFF
Main Sector 77	32K Word	188000-18FFFF
Main Sector 78	32K Word	180000-187FFF
Main Sector 79	32K Word	178000-17FFFF
Main Sector 80	32K Word	170000-177FFF
Main Sector 81	32K Word	168000-16FFFF
Main Sector 82	32K Word	160000-167FFF
Main Sector 83	32K Word	158000-15FFFF
Main Sector 84	32K Word	150000-157FFF
Main Sector 85	32K Word	148000-14FFFF
Main Sector 86	32K Word	140000-147FFF
Main Sector 87	32K Word	138000-13FFFF
Main Sector 88	32K Word	130000-137FFF
Main Sector 89	32K Word	128000-12FFFF
Main Sector 90	32K Word	120000-127FFF
Main Sector 91	32K Word	118000-11FFFF
Main Sector 92	32K Word	110000-117FFF
Main Sector 93	32K Word	108000-10FFFF
Main Sector 94	32K Word	100000-107FFF
Main Sector 95	32K Word	0F0000-0FFFFF
Main Sector 96	32K Word	0F0000-0F7FFF
Main Sector 97	32K Word	0E8000-0EFFFF
Main Sector 98	32K Word	0E0000-0E7FFF
Main Sector 99	32K Word	0D8000-0DFFFF
Main Sector 100	32K Word	0D0000-0D7FFF
Main Sector 101	32K Word	0C8000-0CFFFF
Main Sector 102	32K Word	0C0000-0C7FFF
Main Sector 103	32K Word	0B8000-0BFFFF
Main Sector 104	32K Word	0B0000-0B7FFF
Main Sector 105	32K Word	0A8000-0AFFFF
Main Sector 106	32K Word	0A0000-0A7FFF
Main Sector 107	32K Word	098000-09FFFF
Main Sector 108	32K Word	090000-097FFF
Main Sector 109	32K Word	088000-08FFFF
Main Sector 110	32K Word	080000-087FFF

Sector	Sector Size	Address Range (h)
Main Sector 111	32K Word	078000-07FFFF
Main Sector 112	32K Word	070000-077FFF
Main Sector 113	32K Word	068000-06FFFF
Main Sector 114	32K Word	060000-067FFF
Main Sector 115	32K Word	058000-05FFFF
Main Sector 116	32K Word	050000-057FFF
Main Sector 117	32K Word	048000-04FFFF
Main Sector 118	32K Word	040000-047FFF
Main Sector 119	32K Word	038000-03FFFF
Main Sector 120	32K Word	030000-037FFF
Main Sector 121	32K Word	028000-02FFFF
Main Sector 122	32K Word	020000-027FFF
Main Sector 123	32K Word	018000-01FFFF
Main Sector 124	32K Word	010000-017FFF
Main Sector 125	32K Word	008000-00FFFF
Main Sector 126	32K Word	000000-007FFF

SECTOR STRUCTURE (BOTTOM)

Sector	Sector Size	Address Range (h)
Boot Sector 0	4K Word	000000-000FFF
Boot Sector 1	4K Word	001000-001FFF
Parameter Sector 0	4K Word	002000-002FFF
Parameter Sector 1	4K Word	003000-003FFF
Parameter Sector 2	4K Word	004000-004FFF
Parameter Sector 3	4K Word	005000-005FFF
Parameter Sector 4	4K Word	006000-006FFF
Parameter Sector 5	4K Word	007000-007FFF
Main Sector 0	32K Word	008000-00FFFF
Main Sector 1	32K Word	010000-017FFF
Main Sector 2	32K Word	018000-01FFFF
Main Sector 3	32K Word	020000-027FFF
Main Sector 4	32K Word	028000-02FFFF
Main Sector 5	32K Word	030000-037FFF
Main Sector 6	32K Word	038000-03FFFF
Main Sector 7	32K Word	040000-047FFF
Main Sector 8	32K Word	048000-04FFFF
Main Sector 9	32K Word	050000-057FFF
Main Sector 10	32K Word	058000-05FFFF
Main Sector 11	32K Word	060000-067FFF
Main Sector 12	32K Word	068000-06FFFF
Main Sector 13	32K Word	070000-077FFF
Main Sector 14	32K Word	078000-07FFFF
Main Sector 15	32K Word	080000-087FFF
Main Sector 16	32K Word	088000-08FFFF
Main Sector 17	32K Word	090000-097FFF
Main Sector 18	32K Word	098000-09FFFF
Main Sector 19	32K Word	0A0000-0A7FFF
Main Sector 20	32K Word	0A8000-0AFFFF
Main Sector 21	32K Word	0B0000-0B7FFF
Main Sector 22	32K Word	0B8000-0BFFFF
Main Sector 23	32K Word	0C0000-0C7FFF
Main Sector 24	32K Word	0C8000-0CFFFF
Main Sector 25	32K Word	0D0000-0D7FFF
Main Sector 26	32K Word	0D8000-0DFFFF
Main Sector 27	32K Word	0E0000-0E7FFF
Main Sector 28	32K Word	0E8000-0EFFFF
Main Sector 29	32K Word	0F0000-0F7FFF
Main Sector 30	32K Word	0F8000-0FFFFF
Main Sector 31	32K Word	100000-107FFF
Main Sector 32	32K Word	108000-10FFFF
Main Sector 33	32K Word	110000-117FFF
Main Sector 34	32K Word	118000-11FFFF
Main Sector 35	32K Word	120000-127FFF
Main Sector 36	32K Word	128000-12FFFF
Main Sector 37	32K Word	130000-137FFF
Main Sector 38	32K Word	138000-13FFFF
Main Sector 39	32K Word	140000-147FFF
Main Sector 40	32K Word	148000-14FFFF
Main Sector 41	32K Word	150000-157FFF
Main Sector 42	32K Word	158000-15FFFF
Main Sector 43	32K Word	160000-167FFF
Main Sector 44	32K Word	168000-16FFFF
Main Sector 45	32K Word	170000-177FFF
Main Sector 46	32K Word	178000-17FFFF
Main Sector 47	32K Word	180000-187FFF
Main Sector 48	32K Word	188000-18FFFF
Main Sector 49	32K Word	190000-197FFF
Main Sector 50	32K Word	198000-19FFFF
Main Sector 51	32K Word	1A0000-1A7FFF
Main Sector 52	32K Word	1A8000-1AFFFF
Main Sector 53	32K Word	1B0000-1B7FFF
Main Sector 54	32K Word	1B8000-1BFFFF
Main Sector 55	32K Word	1C0000-1C7FFF
Main Sector 56	32K Word	1C8000-1CFFFF
Main Sector 57	32K Word	1D0000-1D7FFF
Main Sector 58	32K Word	1D8000-1DFFFF
Main Sector 59	32K Word	1E0000-1E7FFF
Main Sector 60	32K Word	1E8000-1EFFFF
Main Sector 61	32K Word	1F0000-1F7FFF
Main Sector 62	32K Word	1F8000-1FFFFF
Main Sector 63	32K Word	200000-207FFF
Main Sector 64	32K Word	208000-20FFFF
Main Sector 65	32K Word	210000-217FFF
Main Sector 66	32K Word	218000-21FFFF
Main Sector 67	32K Word	220000-227FFF
Main Sector 68	32K Word	228000-22FFFF
Main Sector 69	32K Word	230000-237FFF
Main Sector 70	32K Word	238000-23FFFF

Sector	Sector Size	Address Range (h)
Main Sector 71	32K Word	240000-247FFF
Main Sector 72	32K Word	248000-24FFFF
Main Sector 73	32K Word	250000-257FFF
Main Sector 74	32K Word	258000-25FFFF
Main Sector 75	32K Word	260000-267FFF
Main Sector 76	32K Word	268000-26FFFF
Main Sector 77	32K Word	270000-277FFF
Main Sector 78	32K Word	278000-27FFFF
Main Sector 79	32K Word	280000-287FFF
Main Sector 80	32K Word	288000-28FFFF
Main Sector 81	32K Word	290000-297FFF
Main Sector 82	32K Word	298000-29FFFF
Main Sector 83	32K Word	2A0000-2A7FFF
Main Sector 84	32K Word	2A8000-2AFFFF
Main Sector 85	32K Word	2B0000-2B7FFF
Main Sector 86	32K Word	2B8000-2BFFFF
Main Sector 87	32K Word	2C0000-2C7FFF
Main Sector 88	32K Word	2C8000-2CFFFF
Main Sector 89	32K Word	2D0000-2D7FFF
Main Sector 90	32K Word	2D8000-2DFFFF
Main Sector 91	32K Word	2E0000-2E7FFF
Main Sector 92	32K Word	2E8000-2EFFFF
Main Sector 93	32K Word	2F0000-2F7FFF
Main Sector 94	32K Word	2F8000-2FFFFF
Main Sector 95	32K Word	300000-307FFF
Main Sector 96	32K Word	308000-30FFFF
Main Sector 97	32K Word	310000-317FFF
Main Sector 98	32K Word	318000-31FFFF
Main Sector 99	32K Word	320000-327FFF
Main Sector 100	32K Word	328000-32FFFF
Main Sector 101	32K Word	330000-337FFF
Main Sector 102	32K Word	338000-33FFFF
Main Sector 103	32K Word	340000-347FFF
Main Sector 104	32K Word	348000-34FFFF
Main Sector 105	32K Word	350000-357FFF
Main Sector 106	32K Word	358000-35FFFF
Main Sector 107	32K Word	360000-367FFF
Main Sector 108	32K Word	368000-36FFFF
Main Sector 109	32K Word	370000-377FFF
Main Sector 110	32K Word	378000-37FFFF

Sector	Sector Size	Address Range (h)
Main Sector 111	32K Word	380000-387FFF
Main Sector 112	32K Word	388000-38FFFF
Main Sector 113	32K Word	390000-397FFF
Main Sector 114	32K Word	398000-39FFFF
Main Sector 115	32K Word	3A0000-3A7FFF
Main Sector 116	32K Word	3A8000-3AFFFF
Main Sector 117	32K Word	3B0000-3B7FFF
Main Sector 118	32K Word	3B8000-3BFFFF
Main Sector 119	32K Word	3C0000-3C7FFF
Main Sector 120	32K Word	3C8000-3CFFFF
Main Sector 121	32K Word	3D0000-3D7FFF
Main Sector 122	32K Word	3D8000-3DFFFF
Main Sector 123	32K Word	3E0000-3E7FFF
Main Sector 124	32K Word	3E8000-3EFFFF
Main Sector 125	32K Word	3F0000-3F7FFF
Main Sector 126	32K Word	3F8000-3FFFFF

2 PRINCIPLES OF OPERATION

The product includes an on-chip WSM to manage sector erase, word write and lock-bit configuration functions.

After initial device power-up or return from reset mode (see section on Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the VPP voltage. All functions associated with altering memory contents-sector erase, word write, sector lock/unlock, status and identifier codes - are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the sector erase, word write and sector lock/unlock. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Address is latched at falling edge of $\overline{CE}$ and data latched at rising edge of $\overline{WE}$. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of sector erase, full chip erase, word write and sector lock/unlock can be stored in any sector. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Sector erase suspend allows system software to suspend a sector erase to read/write data from/to sectors other than that which is suspend. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

With the mechanism of sector lock, memory contents cannot be altered due to noise or unwanted operation. When $\overline{RESET}$=VIH and VCC<VLKO (lockout voltage), any data write alteration can be failure. During read operation, if write VPP voltage is below VPPLK, then hardware level data protection is achieved. With CUI's two-step command sequence sector erase, word write or sector lock/unlock, software level data protection is achieved also.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any sector, configuration codes or status register independent of the VPP voltage. $\overline{RESET}$ can be at VIH.

The first task is to write the appropriate read mode command (Read Array, Read Configuration, Read Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. In order to read data, control pins set for $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{RESET}$ and $\overline{WP}$ must be driven to active. $\overline{CE}$ and $\overline{OE}$ must be active to obtain data at the outputs. $\overline{CE}$ is the device selection control. $\overline{OE}$ is the data output (Q0-Q15) control and active drives the selected memory data onto the I/O bus, $\overline{WE}$ must be VIH, $\overline{RESET}$ must be VIH, $\overline{WP}$ must be at VIL or VIH.

3.2 Output Disable

With $\overline{OE}$ at a logic-high level (VIH), the device outputs are disabled. Output pins (Q0-Q15) are placed in a high-impedance state.

3.3 Standby

$\overline{CE}$ at a logic-high level (VIH) places the device in standby mode which substantially reduces device power consumption. Q0~Q15 outputs are placed in a high-impedance state independent of $\overline{OE}$. If deselected during sector erase, word write or sector lock/unlock, the device continues functioning, and consuming active power until the operation completes.

3.4 Reset

As $\overline{RESET}$=VIL, it initiates the reset mode. The device enters reset/deep power down mode. However, the data stored in the memory has to be sustained at least 100ns in the read mode before the device becomes deselected

and output high impedance state.

In read modes, RESET-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RESET must be held low for a minimum of 100ns. Time tPHQV is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval tPHEL or tPHWL, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H. Sector lock bit is set at lock status.

During sector erase, word write or sector lock/unlock modes, RESET-low will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or written.

In addition, CUI will go into either array read mode or erase/write interrupted mode. When power is up and the device reset subsequently, it is necessary to read status register in order to assure the status of the device. Recognizing status register (SR.7~0) will assure if the device goes back to normal reset and enters array read mode.

3.5 Read Configuration Codes

The read configuration codes operation outputs the manufacturer code, device code, sector lock configuration codes, and the protection register Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The sector lock codes identify locked and unlocked sectors.

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When VCC=2.7V-3.6V and VPP=VPPH1/2, the CUI additionally controls sector erase, full chip erase, word write and sector lock/unlock.

The Sector Erase command requires appropriate command data and an address within the sector to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word Write command requires the command and address of the location to be written. Set Sector lock/unlock commands require the command and address within the device or sector within the device (Sector Lock) to be locked. The Clear Sector Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE and CE are active (whichever goes high first). The address and data needed to execute a command are latched on the rising edge of WE or CE. Standard microprocessor write timings are used.

4 COMMAND DEFINITIONS

When the VPP voltage < VPPLK, read operations from the status register, identifier codes, or sectors are enabled. Placing VPP on VPPH1/2 enables successful sector erase, full chip erase, word write and sector lock/unlock.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

Table 2. Bus Operation [1,2]

Mode	Notes	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Q0~Q15
Read	1,2	VIH	VIL	VIL	VIH	DOUT
Output Disable	2	VIH	VIL	VIH	VIH	High Z
Standby	2	VIH	VIH	X	X	High Z
Reset	2	VIL	X	X	X	High Z
Write	2,3,4,5	VIH	VIL	VIH	VIL	DIN

Notes:
1. Refer to DC Characteristics for VPPLK, VPP1, VPP2, VPP3 voltage.
2. X can be VIL or VIH for pin and addresses.
3. $\overline{RESET}$ at GND±0.2 to ensure the lowest power consumption.
4. Refer to Table 3 for valid DIN during a write operation.
5. To program or erase the lockable sectors holds $\overline{WP}$ at VIH.

Table 3. Command Definition (1)

Command	Bus Cycles Required	Notes	First Bus Cycle			Second Bus Cycle		
			Operation (1)	Address (2)	Data (3)	Operation (1)	Address (2)	Data (3)
Read Array	1		Write	X	FFH			
Read Configuration	≥ 2	3,4	Write	X	90H	Read	IA	ID
Read Query	2	2,7	Write	X	98H	Read	QA	QD
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1	3	Write	X	50H			
Sector Erase/Confirm	2		Write	X	20H	Write	BA	D0H
Word Write	2	5	Write	X	40H/10H	Write	WA	WD
Program/Erase Suspend	1		Write	X	B0H			
Program/Erase Resume	1		Write	X	D0H			
Sector Lock	2		Write	X	60H	Write	BA	01H
Sector Unlock	2	6	Write	X	60H	Write	BA	D0H
Lock-Down Sector	2		Write	X	60H	Write	BA	2FH
Protection Program	2		Write	X	C0H	Write	PA	PPH

Notes:
1. Bus operation are defined in Table 2 and referred to AC Timing Waveform.
2. X=Any address within device
   IA=ID-Code Address (refer to Table 4)
   BA=Sector within the sector being erased
   WA=Address of memory location to be written
   QA=Query Address, QD=Query Data
3. Data is latched from the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first)
   SRD=Data read from status register, see Table 6 for description of the status register bits.
   WD=Data to be written at location WA. ID=Data read from identifier codes
4. Following the Read configuration codes command, read operation access manufacturer, device codes, sector lock/unlock codes, see chapter 4.2.
5. Either 40H or 10H are recognized by the WSM as word write setup.
6. The sector unlock operation simultaneously clear all sector lock.
7. Read Query Command is read for CFI query information.

4.1 Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a sector erase, word write or sector lock configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via a Sector Erase Suspend or Word Write Suspend command. If RESET=VIL device is in read Read Array command mode, this read operation no longer requires VPP. The Read Array command functions independently of the VPP voltage and RESET can be VIH.

4.2 Read Configuration Codes Command

The configuration code operation is initiated by writing the Read Configuration Codes command (90H). To return to read array mode, write the Read Array Command (FFH). Following the command write, read cycles from addresses shown in Table 4 retrieve the manufacturer, device, sector lock configuration codes (see Table 4 for configuration code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Configuration Codes command functions independently of the VPP voltage and RESET can be VIH. Following the Read Configuration Codes command, the information is shown:

Table 4: ID Code

Code	Address (A19-A0)	Data (Q15-Q0)
Manufacturer Code	00000H	00C2H
Device Code	00001H	88CC/88CDH
Sector Lock Configuration	XX002H	LocK
- Sector is unlocked		Q0=0
- Sector is locked		Q0=1
- Sector is locked-down		Q1=1
Protection Register Lock	80	PR-LK
Protection Register	81-88	PR

4.3 Read Status Register Command

CUI writes read status command (70H). The status register may be read to determine when a sector erase, word write or lock-bit configuration is complete and whether the operation completed successfully. (refer to table 6) It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of CE or OE, whichever occurs. CE or OE must toggle to VIH before further reads to update the status register latch. The Read Status Register command functions independently of the VPP voltage. RESET can be VIH.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command (50H). These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple sectors or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written on CUI. It functions independently of the applied VPP Voltage. RESET can be VIH. This command is not functional during sector erase or word write suspend modes.

4.5 Sector Erase Command

Erase is executed one sector at a time and initiated by a two-cycle command. A sector erase setup is first written (20H), followed by a sector erase confirm (D0H). This command sequence requires appropriate sequencing and an address within the sector to be erased. Sector preconditioning, erase, and verify are handled internally by the WSM. After the two-cycle sector erase sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect sector erase completion by analyzing the output data of the status register bit SR.7.

When the sector erase is complete, status register bit SR.5 should be checked. If a sector erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that sector contents are not accidentally erased. An invalid sector Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable sector erasure can only occur when 2.7V~3.6V and VPP=VPPH1/2. In the absence of this high voltage, sector contents are protected against erasure. If sector erase is attempted while VPP≤VPPLK SR.3 and SR.5 will be set to "1". To successfully erase the boot sector, the corresponding sector lock-bit must be clear first. In parameter and sectors case, it must be cleared the corresponding sector lock-bit. If sector erase is attempted when the excepting above sector being locked conditions, SR.1 and SR.5 will be set to "1". Sector erase is not functional.

4.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data. The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the word write event by analyzing the status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when VCC=2.7V~3.6V and VPP=VPPH1/2. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while VPP≤VPPLK, status register bits SR.3 and SR.4 will be set to "1". Successful word write requires for boot sector that WP is VIH the corresponding sector lock-bit be cleared. In parameter and main sectors case, it must be cleared the corresponding sector lock-bit. If word write is attempted when the excepting above sector being clocked conditions, SR.1 and SR.4 will be set to "1". Word write is not functional.

4.7 Sector Erase Suspend Command

The Sector Erase Suspend command (50H) allows sector-erase interruption to read or word write data in another sector of memory. Once the sector erase process starts, writing the Sector Erase Suspend command requests that the WSM suspend the sector erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Sector Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the sector erase operation has been suspended (both will be set to "1"). Specification tWHR12 defines the sector erase suspend latency.

When Sector Erase Suspend command write to the CUI, if sector erase was finished, the device places read array mode. Therefore, after Sector Erase Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.6 should be checked for placing the device in suspend mode.

At this point, a Read Array command can be written to read data from sectors other than that which is suspended. A Word Write commands sequence can also be issued during erase suspend to program data in other sectors. Using the Word Write Suspend command (see Section 4.9), a word write operation can also be suspended. During a word write operation with sector erase suspended, status register bit SR.7 will return to "0".

However, SR.6 will remain "1" to indicate sector erase suspend status.

The only other valid commands while sector erase is suspended are Read Status Register and sector erase Resume. After a Sector Erase Resume command is written to the flash memory, the WSM will continue the sector erase process. Status register bits SR.6 and SR.7 will automatically clear. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 4). VPP must remain at VPPH1/2 while sector erase is suspended. RESET must also remain at VIL or VHH (the same RESET level used for sector erase). WP must also remain at VIL or VIH (the same WP level used for sector erase). Sector cannot resume until word write operations initiated during sector erase suspend has completed.

If the time between writing the Sector Erase Resume command and writing the Sector Erase Suspend command is shorter than 15ms and both commands are written repeatedly, a longer time is required than standard sector erase until the completion of the operation.

4.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the Word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). Specification tWHR11 defines the word write suspend latency.

When Word Write Suspend command write to the CUI, if word write was finished, the device places read array mode. Therefore, after Word Write Suspend command write to the CUI, Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked for placing the device in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the Word write process. Status register bits SR.2 and SR.7 will automatically clear. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 4). VPP must remain at VPPH1/2 while in word write suspend mode. RESET must also remain at VIL or VHH (the same RESET level used for word write).

If the time between writing the Word Write Resume command and writing the Word Write Suspend command is short and both commands are written repeatedly, a longer time is required than standard word write until the completion of the operation.

4.9 Sector Lock/Unlock /Lock-down Command

4.9.1 Sector Locked State

The default status of all sectors when power-up or reset is locked. Any attempt on program or erase operations will result in an error on bit SR.1 of a locked sector. The status of a locked sector can be changed to unlocked or lock-down using software commands. An unlocked sector can be locked by writing the sector lock command sequence, 60H followed by 01H.

4.9.2 Sector Unlocked State

An unlocked sector can be programmed or erased. All unlocked sector return to the locked state when the device is either reset or powered down. The status of an unlocked sector can be changed to locked or locked-down using software commands. A locked sector can be unlocked by writing unlock command sequence, 60H followed by D0H.

4.9.3 Sector Locked-Down State

Sectors which are locked-down are protected from program and erase operation; however, the protection status of three sectors cannot be changed using software commands alone. Any sector locked or unlocked can be locked-down by writing the lock-down command sequence, 60H followed by 2FH. When the device is reset or powered down, the locked-down sectors will revert to the locked state.

The status of $\overline{WP}$ will determine the function of sector lock-down and is summarized is followed:

$\overline{WP}$	Sector Lock-down Description
$\overline{WP}$=0	- sectors are protected from program, erase, and lock status changes
$\overline{WP}$=1	- the sector lock-down function is disabled - an individual lock-down sector can be un locked and relocked via software command. Once $\overline{WP}$ goes low, sectors that previously locked-down returns to lock-down state regardless of any changes when $\overline{WP}$ was high.

In addition, sector lock-down is cleared only when the device is reset or powered down.

4.9.4 Read Sector Lock Status

The lock status of every sector can be read through Read Configuration mode. To enter this mode first command write 90H to the device. The next sector reads at address +00002 will output the lock status of this sector. The lock status can be read from the lowest two output pins Q0 and Q1. Q0, Q0 indicates the sector lock/unlock status and set by the lock command and cleared by the unlock command. When entering lock-down, the lock status is automatically set. Q1 indicates lock-down status and is set by the lock-down command. It cannot be further cleared by software, only by device reset or power-down.

Sector Lock Configuration Table

Lock Status	Data
Sector is unlocked	Q0=0
Sector is locked	Q0=1
Sector is locked-down	Q1=1

4.9.5 Sector Locking while Erase Suspend

The sector lock status can be performed during an erase suspend by using standard locking command sequences to unlock, lock, or lock-down a sector.

In order to change sector locking during an erase operation, the write erase suspend command (B0H) is placed first; then check the status register until it is shown that the actual erase operation has been suspended. Subsequent writing the desired lock command sequence to a sector and the lock status will be changed. When completing any desired lock, read or program operation, resume the erase operation with the Erase Resume Command (D0H).

If a sector is locked or locked-down during the same sector is being placed in erase suspend, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Locking operation cannot be performed during a program suspend.

4.9.6 Status Register Error Checking

The operation of locking system for this device can be used the term "state (X,Y,Z)" to specify locking status, where X=value of $\overline{WP}$, Y=bit Q1 of the sector lock status register, and Z=bit Q0 of the sector lock status register. Q0 indicates if a sector is locked (1) or unlocked (0). Q1 indicates if a sector has been locked-down(1) or not (0).

Table 5. Sector Locking State Transitions

Current State (X, Y, Z)=				Erase/Prog. Operation if	Lock Command Input Result (Next State) (X, Y, Z)=		
$\overline{WP}$	Q1	Q0	Name	Enable ?	Lock	Unlock	Lock-Down
0	0	0	Unlocked	Yes	(001)	Unchanged	(011)
0	0	1	Locked (Default)	No	Unchanged	(000)	(011)
0	1	1	Locked-Down	No	Unchanged	Unchanged	Unchanged
1	0	0	Unlocked	Yes	(101)	Unchanged	(111)
1	0	1	Locked	No	Unchanged	(100)	(111)
1	1	0	Lock-Down Disabled	Yes	(111)	Unchanged	(111)
1	1	1	Lock-Down Disabled	No	Unchanged	(110)	Unchanged

Table 6. Status Register Definition

WSMS	BESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

SR.6 = SECTOR ERASE SUSPEND STATUS (ESS)
1 = Sector ERASE Suspended
0 = Sector Erase in Progress/Completed

SR.5 = ERASE STATUS (ES)
1 = Error in Programming
0 = Successful Sector Erase or Clear Sector Lock-Bits

SR.4 = PROGRAM STATUS (PS)
1 = Error in Programming
0 = Successful Programming

SR.3 = VPP STATUS (VPPS)
1 = VPP Low Detect, Operation Abort
0 = VPP OK

SR.2 = PROGRAM SUSPEND STATUS (PSS)
1 = Program Suspended
0 = Program in Progress/Completed

SR.1 = SECTOR LOCK STATUS
1 =Program/Erase attempted an a locked sector; operation aborted
0 = No operation to locked sectors

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:
Check WSM bit first to determine word program or sector Erase completion, before checking Program or Erase Status bits.

When Erase Suspend is issued, WSM halts execution and sets both WSMs and ESS bits to "1". ESS bit remains set to "1" until an Erase Resume command is issued.

When this bit (SR.5) is set to "1", it means WSM is unable to verify successful sector erasure.

When this bit is set to "1", WSM has attempted but failed to program a word.

SR.3 bit is not guaranteed to report accurate feedback between VPPLK and VPP min.

When program suspend is issued, WSM halts the execution and sets both WSMs and SR.2 bit to "1". SR.2 remains set to "1" until a Program Resume command is issued.

If a program or erase operation is attempted to one of the locked sectors, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.

SR. 0 is reserved for future use and should be masked out when polling the status register.

5. 128-Bit Protection Register

The 128-bits of protection register are divided into two 64-bit segments. One of the segments is programmed at MXIC side with unique 64-bit number; where changes are forbidden. The other segment is left empty for customer to program. Once the customer segment is programmed, it can be locked to prevent further reprogramming.

5.1 Protection Register Read & Programming

The protection register is read in the configuration read mode, which follows the stated Command Bus Definitions.

The device is switched to this read mode by writing the Read Configuration command (90H). Once this mode, read cycles from addresses shown in Table 7 will retrieve the specified information. To return to read array mode, write the Read Array Command (FFH).

Two-cycle Protection Program Command is used to program protection register bits. The 64-bit register is programmed 16-bits at a time. First write C0H protection program setup. The next write to the device will latch in address and data and program the specified location. The allowable address are also show in Table 7. Refer to Figure 6 for the Protection Register Programming Flowchart.

Any attempt to address Protection Program command onto undefined protection register address space will result in a Status Register error (SR.4 set to "1"). In addition, attempting to program or to previously locked protection register segment will result in a status register error (SR.4=1, SR.1=1).

Table 7. Word-Wide Protection Register Addressing

Word	User	A7	A6	A5	A4	A3	A2	A1	A0
Lock	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	Customer	1	0	0	0	0	1	0	1
5	Customer	1	0	0	0	0	1	1	0
6	Customer	1	0	0	0	0	1	1	1
7	Customer	1	0	0	0	1	0	0	0

Notes: 1. Set address bit A21-A15=1 for TOP Boot device.
2. Set address bit A21-A15=0 for Bottom Boot device.
3. The address not specified in above are don't care.

5.2 Protection Register Locking

The user-programmable segment of the protection register is lockable by programming Bit 1 of the PR-Lock location to 0. Bit 0 of this location is programmed to 0 at MXIC to protect the unique device number. This bit is set using the unique device number. This bit is set using the protection program command to program "FFFD" to PR-LOCK location. After these bits have been programmed, no further changes can be made to the value stored in the protection register. Protection program command to a locked section will result in a status register error (Program Error bit SR.4 and Lock Error bit SR.1 will be set to 1). Protection register lockout state is not reversible.

Table 8. Protection Register Memory Map

Protection Register Bit Address	Purpose
88H~85H	4 word user program Register
84H~81H	4 word factory program Register
80H(Bit0 & Bit1)	Protection Register Lock (PR-Lock)

6 ELECTRICAL SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Operating Temperature
During Read, Sector Erase, Word Write . . . . . -40°C to +85°C
Storage Temperature . . . . . .-65°C to +125°C
Voltage on Any Pin (except VCC and VPP with respect to GND) . . . . . .-0.5 V to +5V(1)
VCC Supply Voltage . . . . . .-0.2V to +4.6V(2)
VPP Supply Voltage (for sector erase and VPP with respect to GND) . . . . . .-0.5V to +4.6V(1,2)
VCC and VCCQ Supply Voltage with respect to GND. . . . . .-0.2V to +3.6V(1)
Output Short Circuit Voltage 100mA

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

1. Minimum DC voltage is -0.5V on input pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins to VCC+0.5V which during transition; may overshoot to VCC+2.0V for periods <20ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions (Temperature and VCC Operating Conditions)

Symbol	Parameter	Min.	Max.	Unit	Notes
TA	Operating Temperature	-40	+85	°C	
VCC1	VCC Supply Voltage	2.7	3.6	V	1
VCCQ1	I/O Supply Voltage	2.7	3.6	V	1
VPP1	Supply Voltage	1.65	3.6	V	1
Cycling	Sector Erase Cycling	100,000			2

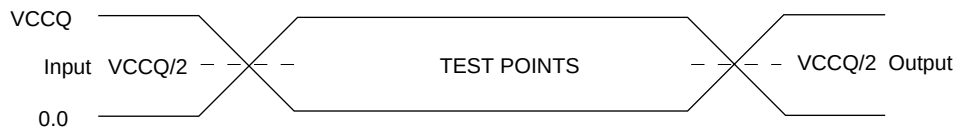
NOTE:
1.VCC and VCCQ must share the same supply when they are in the VCC1 range.

6.2.1 Capacitance (1) (TA=+25°C, f=1MHz)

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
CIN	Input Capacitance	6	8	pF	VIN=0.0V
COUT	Output Capacitance	10	12	pF	VOUT=0.0V

NOTE:
1. Sampled, not 100% tested.

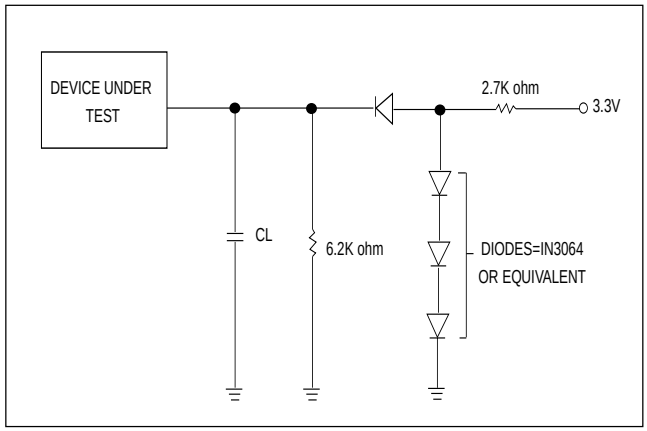
6.2.2 AC Input/Output Test Conditions



Note:AC test inputs are driven at VCCQ/2 for a Logic "1" and 0.0V for a Logic "0".

Figure 1. Transient Input/Output Reference Waveform

Figure 2. SWITCHING TEST CIRCUITS



TEST SPECIFICATIONS

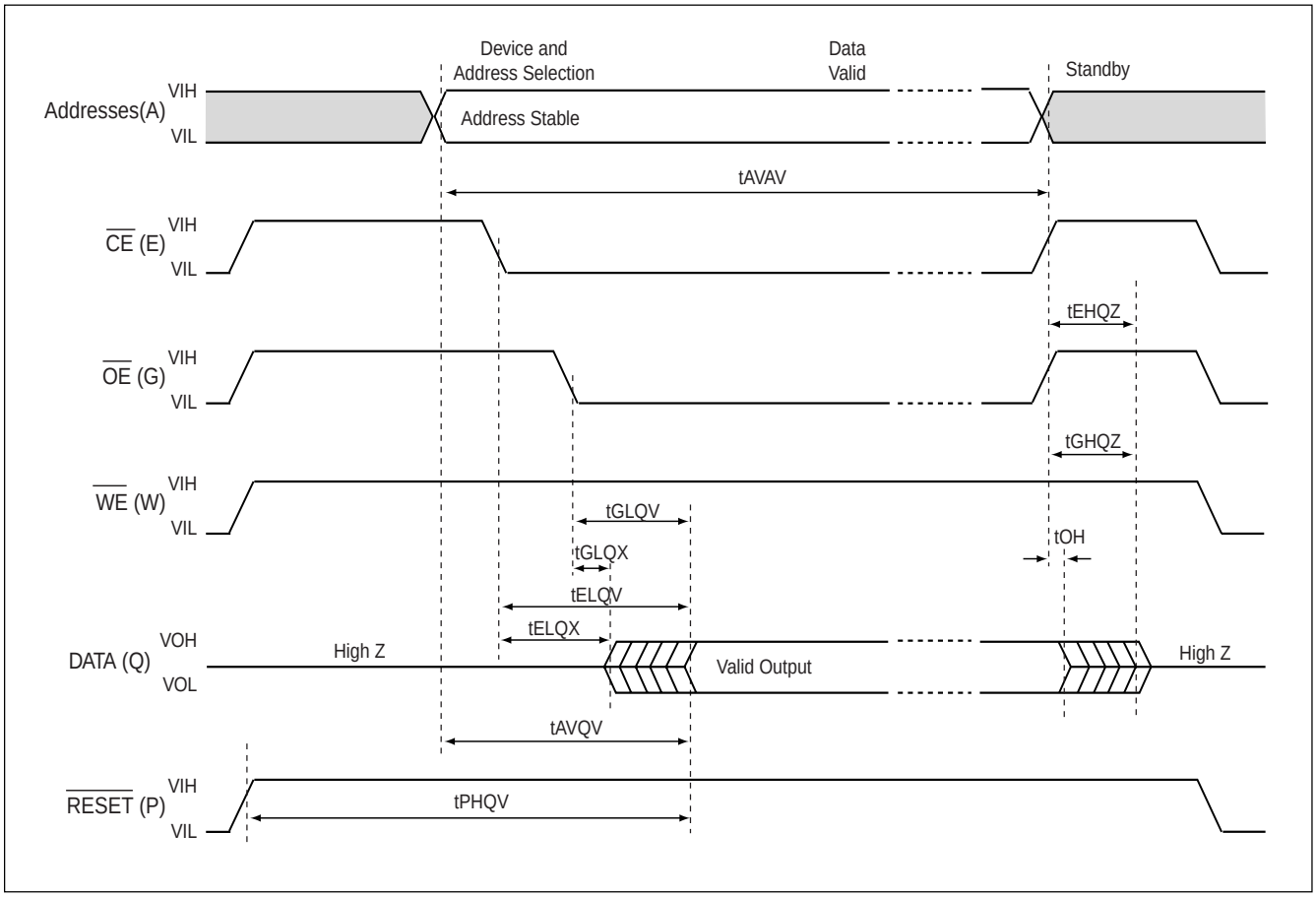
Test Condition	90	120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

6.2.3 AC Characteristic -- Read Only Operation (1)

Sym.	Parameter	Notes	-90		-110		Unit
			Min.	Max.	Min.	Max.	
tAVAV	Read Cycle Time		90		110		ns
tAVQV	Address to Output Delay			90		110	ns
tELQV	$\overline{CE}$ to Output Delay	2		90		110	ns
tGLQV	$\overline{OE}$ to Output Delay	2		30		30	ns
tPHQV	$\overline{RESET}$ to Output Delay			150		150	ns
tELQX	$\overline{CE}$ to Output in Low Z	3	0		0		ns
tGLQX	$\overline{OE}$ to Output in Low Z	3	0		0		ns
tEHQZ	$\overline{CE}$ to Output in High Z	3		20		20	ns
tGHQZ	$\overline{OE}$ to Output in High Z	3		20		20	ns
tOH	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change, Whichever Occurs First	3	0		0		ns

Notes:
1. See AC Waveform: Read Operations.
2. $\overline{OE}$ may be delayed up to tELQV-tGLQV after the falling edge of $\overline{CE}$ without impact on tELQV.
3. Sampled, but not 100% tested.
4. See test Configuration.

Figure 3. READ-ONLY OPERATION AC WAVEFORM

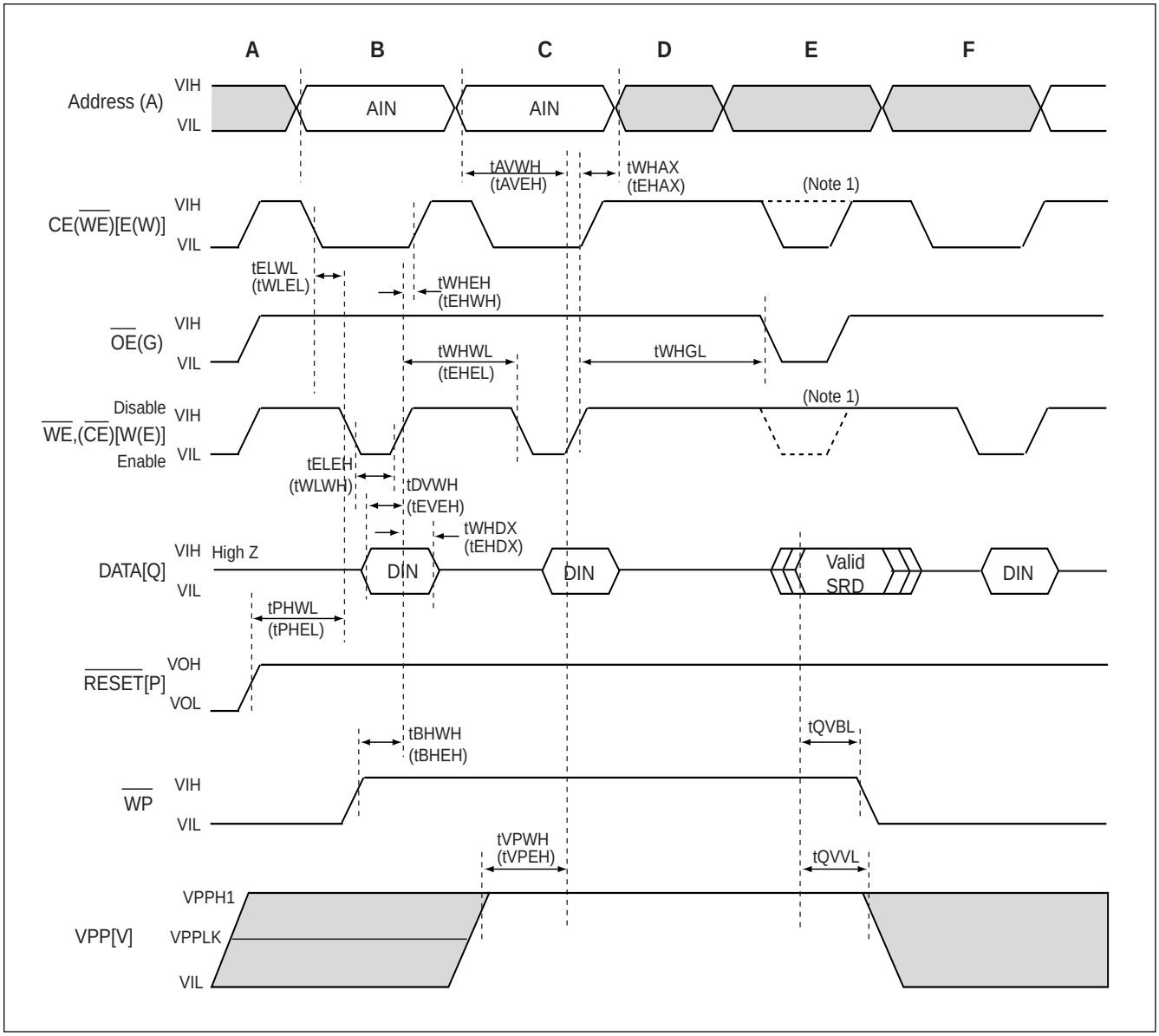


6.2.5 AC Characteristic -- Write Operation

Sym.	Parameter	Note	-90 Min.	-110 Min.	Unit
tPHWL/tPHEL	$\overline{RESET}$ High Recovery to $\overline{WE}$($\overline{CE}$) Going Low		150	150	ns
tELWL/tWLEL	$\overline{CE}$($\overline{WE}$) Setup to $\overline{WE}$($\overline{CE}$) Going Low		0	0	ns
tELEH/tWLWH	$\overline{WE}$($\overline{CE}$) Pulse Width	4	50	70	ns
tDVWH/tDVEH	Data Setup to $\overline{WE}$($\overline{CE}$) Going High	2	50	60	ns
tAVWH/tAVEH	Address Setup to $\overline{WE}$($\overline{CE}$) Going High	2	50	70	ns
tWHEH/tEHWH	$\overline{CE}$($\overline{WE}$) Hold Time from $\overline{WE}$($\overline{CE}$) High		0	0	ns
tWHDX/tEHDX	Data Hold Time from $\overline{WE}$($\overline{CE}$) High	2	0	0	ns
tWHAX/tEHAX	Address Hold Time from $\overline{WE}$($\overline{CE}$) High	2	0	0	ns
tWHWL/tEHEL	$\overline{WE}$($\overline{CE}$) Pulse Width High	4	30	30	ns
tVPWH/tVPEH	VPP Setup to $\overline{WE}$($\overline{CE}$) Going High	3	200	200	ns
tQVVL	VPP Hold from Valid SRD	3	0	0	ns
tBHWH/tBHEH	$\overline{WP}$ Setup to $\overline{WE}$($\overline{CE}$) Going High	3	0	0	ns
tQVBL	$\overline{WP}$ Hold from Valid SRD	3	0	0	ns
tWHGL	$\overline{WE}$ High to $\overline{OE}$ Going Low	3	30	30	ns

Notes:
1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. Refer to Table 5 for valid AIN or DIN.
3. Sampled, not 100% tested.
4. Write pulse width (tWP) is defined from $\overline{CE}$ or $\overline{WE}$ going low (whichever goes low last) to $\overline{CE}$ or $\overline{WE}$ going high (whichever goes high first). Hence, tWP=tWLWH=tELEH=tELWH. Similarly, Write pulse width high (tWPH) is defined from $\overline{CE}$ or $\overline{WE}$ going high (whichever goes high first) to $\overline{CE}$ or $\overline{WE}$ going low (whichever goes low first). Hence, tWPH=tWHWL=tEHEL=tEHWL.
5. See Test Configuration.
6. Vcc Max = 3.3V.

Figure 4. PROGRAM AND ERASE OPERATION AC WAVEFORM



Notes:

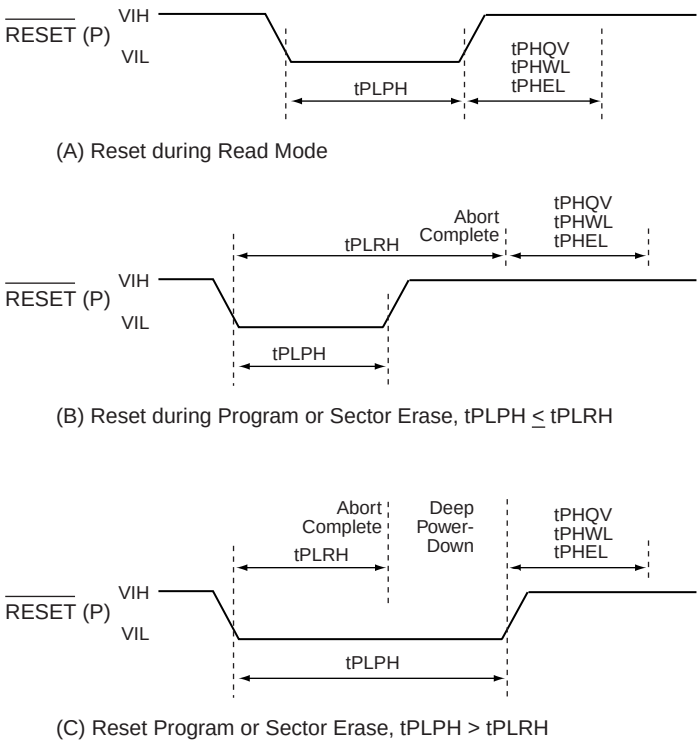
1. $\overline{CE}$ must be toggled low when reading Status Register Data. $\overline{WE}$ must be inactive (high) when reading Status Register Data.
   A. VCC Power-Up and Standby.
   B. Write Program or Erase Setup Command.
   C. Write Valid Address and Data (for Program) or Erase Confirm Command.
   D. Automated Program or Erase Delay.
   E. Read Status Register Data (SRD): reflects completed program/erase operation.
   F. Write Read Array Command.

6.2.5 Erase and Program Timing (1)

Symbol	Parameter	Vpp Note	1.65V-3.6V Typ(1)	1.65V-3.6V Max	Unit
tBWPB	4-KW Parameter Sector Word Program Time(Word)	2,3	0.10	0.30	s
tBWMB	32-KW Main Sector Word Program Time	2,3	0.8	2.4	s
tWHQV1/ tEHQV1	Word Program Time	2,3	12	200	us
tWHQV2/ tEHQV2	4-KW Parameter Sector Erase Time	2,3	0.5	4	s
tWHQV3/ tEHQV3	32-KW Main Sector Erase Time	2,3	1	5	s
tWHRH1/ tEHRH1	Program Suspend Latency	3	5	16	us
tWHRH2/ tEHRH2	Erase Suspend Latency	3	5	20	us

Notes:
1. Typical values measured at TA=+25℃ and nominal voltage.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

Figure 5. $\overline{\text{RESET}}$ WAVEFORM



AC Characteristic -- Under Reset Operation

Sym.	Parameter	VCC=2.7V~3.6V		Unit	Notes
		Min.	Max.		
tPLPH	$\overline{\text{RESET}}$ Low to Reset during Read (If $\overline{\text{RESET}}$ is tied to VCC, this specification is applicable)	100		ns	2,4
tPLRH1	$\overline{\text{RESET}}$ Low to Reset during Sector Erase		22	us	3,4
tPLRH2	$\overline{\text{RESET}}$ Low to Reset during Program		12	us	3,4

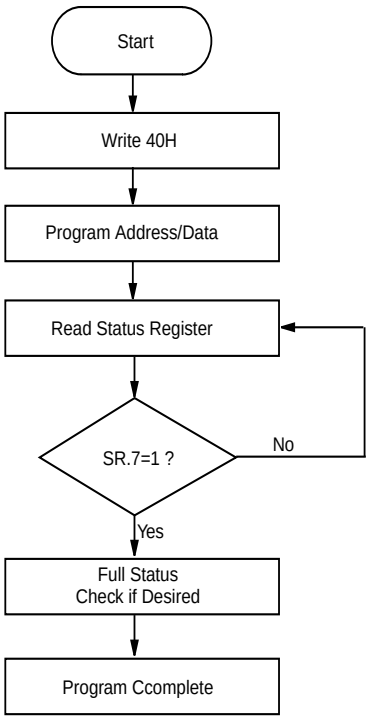
Notes:
1. See Section 3.4 for a full description of these conditions.
2. If tPLPH is < 100ns the device may still reset but this is not guaranteed.
3. If $\overline{\text{RESET}}$ is asserted while a sector erase or word program operation is not executing, the reset will complete within 100ns.
4. Sampled, but not 100% tested.

6.2.6 DC Characteristics

Sym.	Parameter	VCC Note	2.7V-3.6V Typ.	2.7V-3.6V Max.	Unit	Test Conditions
ILI	Input Load Current	1,2		± 1	uA	VCC=VCC Max., VCCQ=VCCQ Max. VIN=VCCQ or GND
ILO	Output Leakage Current	1,2	0.2	± 10	uA	VCC=VCC Max., VCCQ=VCCQ Max. VIN=VCCQ or GND
ICCS	VCC Standby Current	1	7	15	uA	VCC=VCC Max., $\overline{CE}$=$\overline{RESET}$=VCCQ or during Program/Erase Suspend $\overline{WP}$=VCCQ or GND
ICCD	VCC Power-Down Current	1,2	7	15	uA	VCC=VCC Max., VCCQ=VCCQ Max. VIN=VCCQ or GND,$\overline{RESET}$=GND±0.2V
ICCR	VCC Read Current	1,2,3	9	18	mA	VCC=VCC Max.,VCCQ=VCCQ Max. $\overline{OE}$=VIH, $\overline{CE}$=VIL f=5MHz, IOUT=0mA, Inputs=VIL or VIH
IPPD	VPP Deep Power-Down Current	1	0.2	5	uA	$\overline{RESET}$=GND±0.2V VPP < VCC
ICCW	VCC Program Current	1,4	18	55	mA	VPP=VPP1, Program in Progress
ICCE	VCC Erase Current	1,4	16	45	mA	VPP=VPP1, Erase in Progress
ICCES	VCC Erase Suspend Current	1,4	7	15	mA	$\overline{CE}$=VCC, Erase Suspend in Progress
IPPR	VPP Read Current	1,4	2	±15	uA	VPP ≤ VCC
IPPW	VPP Program Current	1,4	0.05	0.1	mA	VPP=VPP1, Program in Progress
IPPE	VPP Erase Current	1,4	0.05	0.1	mA	VPP=VPP1, Program in Progress
VIL	Input Low Voltage		-0.4	VCC* 0.22V	V	
VIH	Input High Voltage		2.0	VCCQ +0.3V	V	
VOL	Output Low Voltage		-0.1	0.1	V	VCC=VCC Min, VCC=VCCQ Min IOL=100uA
VOH	Output High Voltage		VCCQ -0.1V		V	VCC=VCC Min, VCC=VCCQ Min IOH=-100uA
VPPLK	VPP Lock-Out Voltage	6		1.0	V	Complete Write Protection
VPP1	VPP during Program/ Erase Operations	6	1.65	3.6	V	
VLKO	VCC Prog/Erase Lock Voltage		1.5		V	
VLKO2	VCCQ Prog/Erase Lock Voltage		1.2		V	

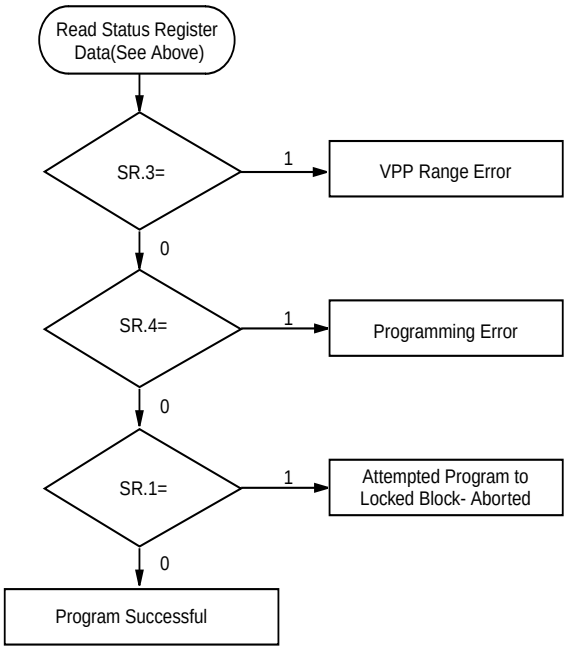
Notes:
1. All currents are in RMS unless otherwise noted. Typical values at nominal VCC, TA=+25℃.
2. The test conditions VCC Max, VCCQ Max, VCC Min, and VCCQ Min refer to the maximum or minimum VCC or VCCQ voltage listed at the top of each column. VCC Max=3.3V for 0.25um 32-Mbit devices.
3. Power Savings (Mode) reduces ICCR to approximately standby levels in static operation (CMOS inputs).
4. Sampled, but not 100% tested.
5. ICCES and ICCWS are specified with device de-selected. If device is read while in erase suspend, current draw is sum of ICCES and ICCR. If the device is read while in program suspend, current draw is the sum of ICCWS and ICCR.
6. Erase and Program are inhibited when VPP<VPPLK and not guaranteed outside the valid VPP ranges of and VPP2.

Figure 6. Automated Word Programming Flowchart



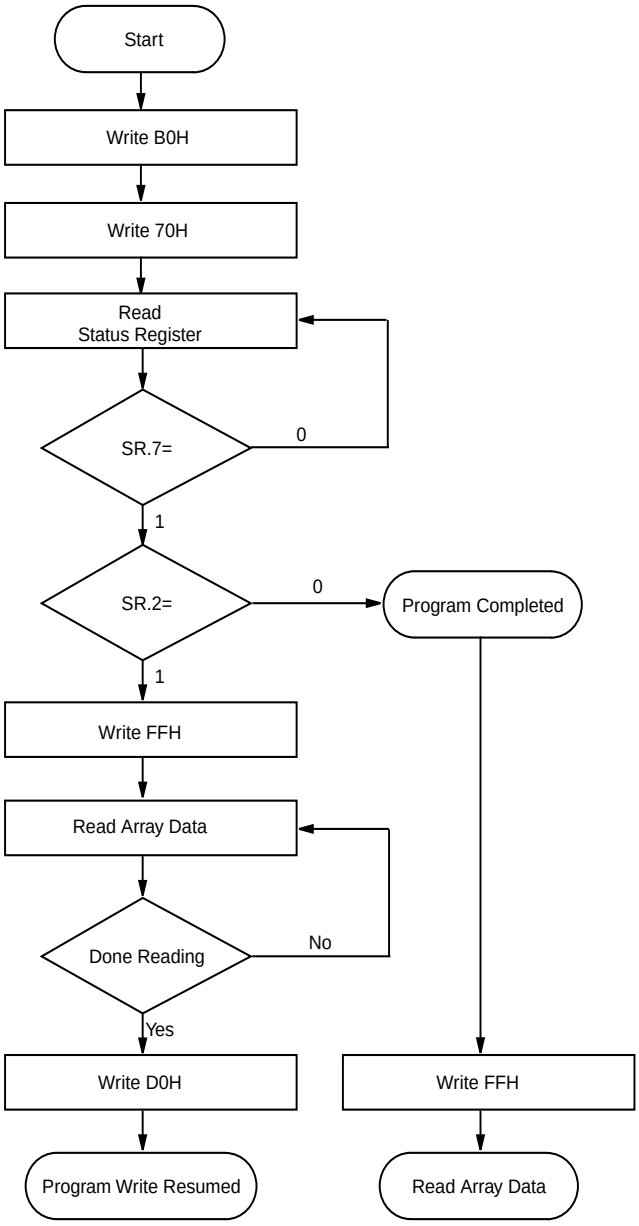
Bus Operation	Command	Comments
Write	Program Setup	Data=40H
Write	Program	Data=Data to Program Addr=Location to Program
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent programming operations. SR full status check can be done after each program or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



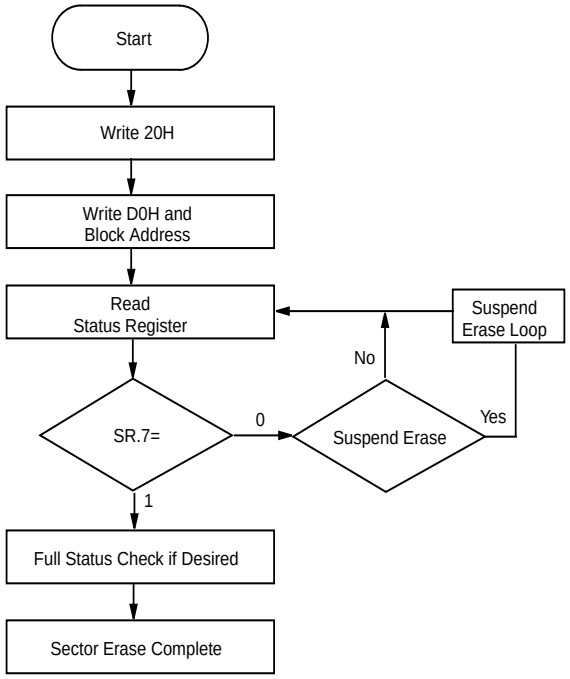
Bus Operation	Command	Comments
Standby		Check SR.3 1=VPP Low Detect
Standby		Check SR.4 1=VPP Program Detect
Standby		Check SR.11 1=Attempted Program to Locked Sector-Program Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command, in cases where multiple programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 7. Program Suspend/Resume Flowchart



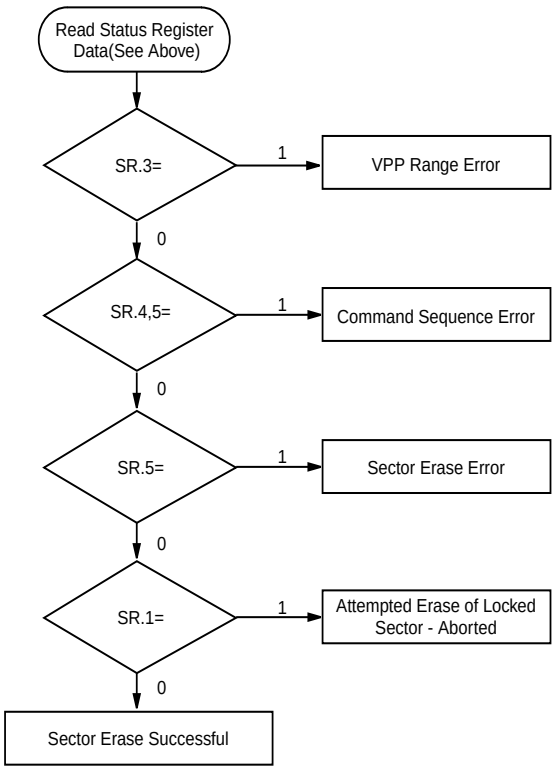
Bus Operation	Command	Comments
Write	Program Suspend	Data=B0H Addr=X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Stanby		Check SR.2 1=Program Suspended 0=Program Completed
Write	Read Array	Data=FFH Addr=X
Read		Read array data from sector other than the one being programmed.
Write	Program Resume	Data=D0H Addr=X

Figure 8. Automated Sector Erase Flowchart



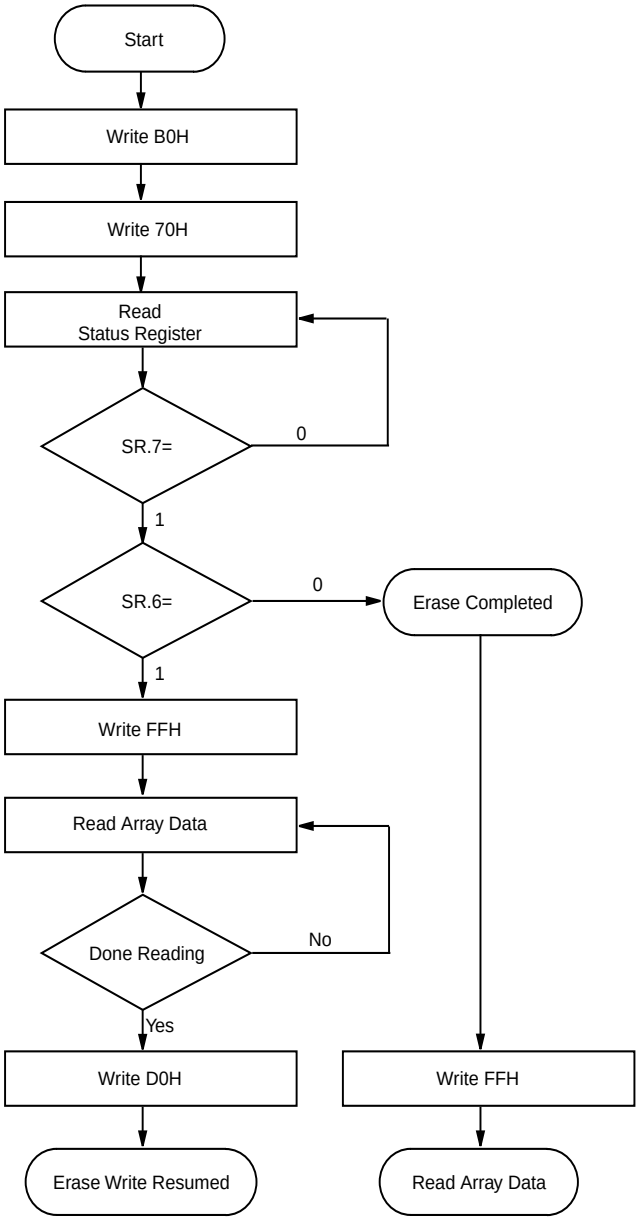
Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Sector to Be Erased
Write	Erase Confirm	Data=D0H Addr=Within Sector to Be Erased
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each sector erase or after a sequence of sector erasures. Write FFH after the last write operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



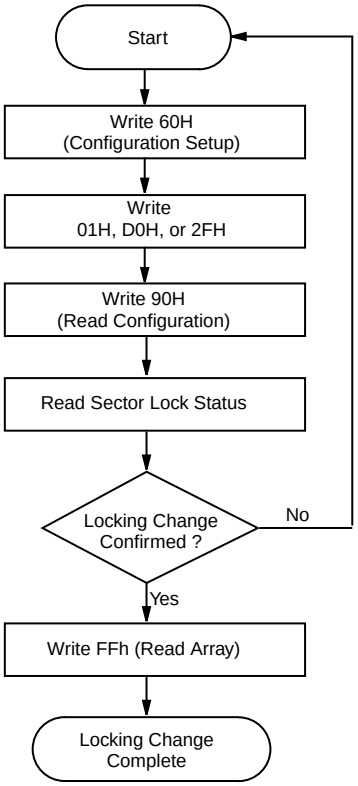
Bus Operation	Command	Comments
Standby		Check SR.3 1=VPP Low Detect
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Sector Erase Error
Standby		Check SR.1 1=Attempted Erase of Locked Sector- Erase Aborted
SR.1 and SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine. SR.1,3,4,5 are only cleared by the Clear Status Register Command, in cases where multiple sectors are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 9. Erase Suspend/Resume Flowchart



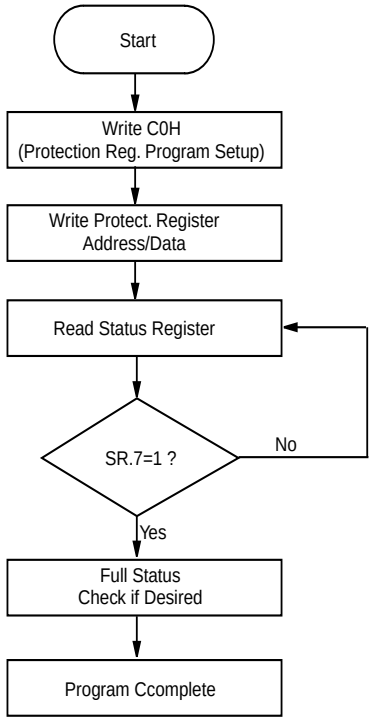
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Stanby		Check SR.6 1=Erase Suspended 0=Erase Completed
Write	Read Array	Data=FFH Addr=X
Read		Read array data from sector other than the one being erased.
Write	Erase Resume	Data=D0H Addr=X

Figure 10. Locking Operations Flowchart



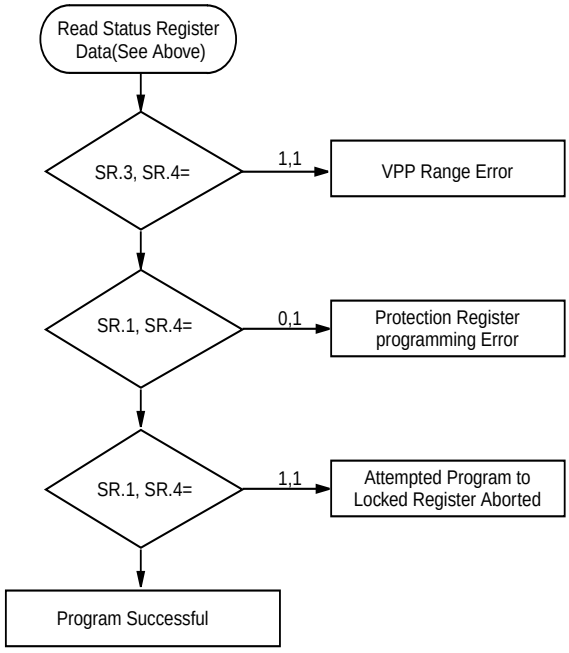
Bus Operation	Command	Comments
Write	Config. Setup	Data=60H Addr=X
Write	Lock, unlock or Lockdown	Data=01H (Sector Lock) D0H(Sector Unlock) 2FH(Sector Lockdown) Addr=Within sector to lock
Write (Optional)	Read Configuration	Data=90H Addr=X
Read (Optional)	Sector Lock Status	Sector Lock Status Data Addr=Second addr of sector
Stanby		Confirm Locking Change on Q1, Q0 (See Sector Locking State Table for valid combinations.)

Figure 11. Protection Register Programming Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data=C0H
Write	Protection Program	Data=Data to Program Addr=Location to Program
Read		Status Register Data Toggle $\overline{CE}$ or $\overline{OE}$ to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Protection Program operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error. Repeat for subsequent programming operations. SR Full Status Check can be done after each program or after a sequence of program operations. Write FFH after the last operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		SR.1, SR.3, SR.4 0 1 1 VPP Low
Standby		0 0 1 Prot. Reg. Prog. Error
Stanby		1 0 1 Register Locked: Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.1,3,4 are only cleared by the Clear Status Register Command, in cases of multiple protection register program operations before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

7 VPP Program and Erase Voltage

When VPP is between 1.65V and 3.6V, all program and erase current is drawn through the VCC pin. If VPP is driven by a logic signal, VIH=1.65V. That is, VPP must remain above 1.65V to perform in-system flash update/ modifications.

7.1 Protection Under VPP<VPPLK

VPP can off additional hardware write protection. The VPP programming voltage can be kept low for the absolute hardware protection of all sector in the flash device. As VPP is below VPPLK, any program or erase operation will result in a error, prompting the corresponding status register bit (SR.3) to be set.

8. QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX28F640C3T/B is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table X.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Program Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, Program Suspend or read ID mode. The command is valid only when the device is in the CFI mode.

Table 9-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address h	Data h
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0003
	14	0000
Address for primary algorithm extended query table	15	0035
	16	0000
Alternate vendor command set and control interface ID code (none)	17	0000
	18	0000
Address for secondary algorithm extended query table (none)	19	0000
	1A	0000

Table 9-2. CFI Mode: System Interface Data Values

Description	Address h	Data h
VCC supply, minimum (2.7V)	1B	0027
VCC supply, maximum (3.6V)	1C	0036
VPP supply, minimum (none)	1D	0017
VPP supply, maximum (none)	1E	0036
Typical timeout for single word write (2^N us)	1F	0005
Typical timeout for maximum size buffer write (2^N us)	20	0000
Typical timeout for individual block erase (2^N ms)	21	000A
Typical timeout for full chip erase (2^N ms)	22	0000
Maximum timeout for single word write times (2^N X Typ)	23	0004
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	0000
Maximum timeout for individual block erase times (2^N X Typ)	25	0003
Maximum timeout for full chip erase times (not supported)	26	0000

Table 9-3. CFI Mode: Device Geometry Data Values

Description	Address h	Data h	
Device size (2N bytes)	27	0017	
Flash device interface code (02=asynchronous x8/x16)	28	0001	
	29	0000	
Maximum number of bytes in multi-byte write (not supported)	2A	0000	
	2B	0000	
Number of erase block regions	2C	0002	
Erase block region 1 information		T	B
[2E,2D] = # of blocks in region -1	2D	07	TE
[30, 2F] = size in multiples of 256-bytes	2E	00	00
	2F	20	00
	30	00	01
Erase Sector Region 2 information	31	07	7E
[32,31] = number of same-size sectors in region 2-1	32	00	00
[34,33] = region erase sector size in multiples of 256-bytes	33	20	00
	34	00	01

Table 9-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

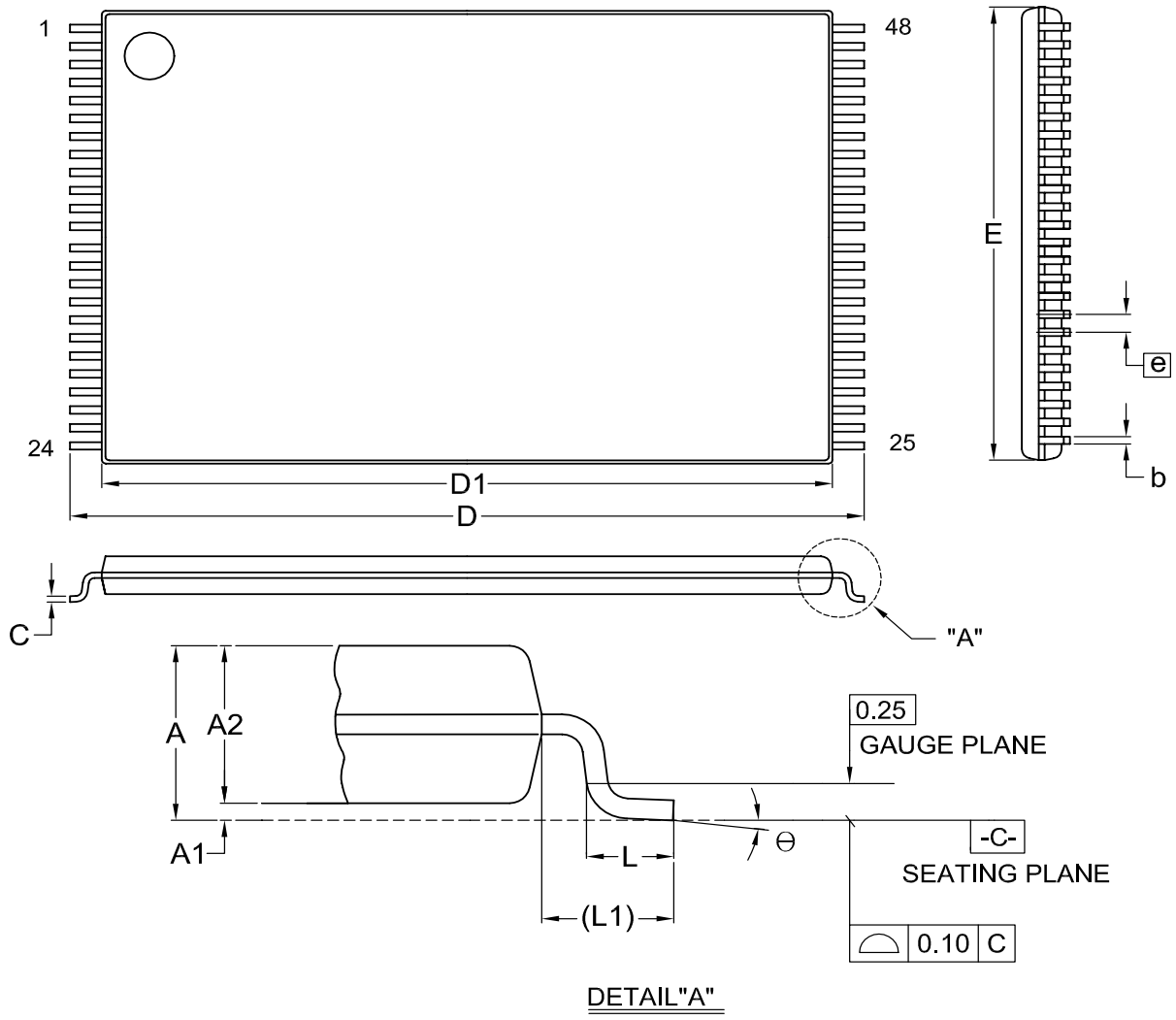
Description	Address h	Data h
Query-unique ASCII string "PRI"	35	0050
	36	0052
	37	0049
Major version number, ASCII	38	0031
Minor version number, ASCII	39	0030
Optional Feature & Command Support	3A	66
bit 0 Chip Erase Supported (1=yes, 0=no)	3B	00
bit 1 Suspend Erase Supported (1=yes, 0=no)	3C	00
bit 2 Suspend Program Supported (1=yes, 0=no)	3D	00
bit 3 Lock/Unlock Supported (1=yes, 0=no)		
bit 4 Queued Erase Supported (1=yes, 0=no)		
bits 5-31 revered for future use; undefined bits are "0"		
Sector Lock Status	3F	03
Define which bits in the sector status Register section of the Query are implemented.	40	00
bit 0 sector Lock Status Register Lock/Unlock bit (bit 0) active; (1=yes, 0=no)		
bit 1 sector Lock Status Register Lock/Unlock bit (bit 1) active; (1=yes, 0=no)		
Bits 2-15 reserved for future use. Undefined bits are 0.		
VCC Logic Supply Optimum Program/Erase Voltage (highest performance)	41	33
bits 7-4 BCD value in volts		
bits 3-0 BCD value in 100mV		
VPP (Programming) Supply Optimum Program/Erase Voltage	42	33
bits 7-4 HEX value in volts		
bits 3-0 BCD value in 100mV		

ORDER INFORMATION

PART NO.	ACCESS TIME (ns)	OPERATING Current MAX.(mA)	STANDBY Current MAX.(uA)	PACKAGE
MX28F640C3TTC-90	90	30	5	48 Pin TSOP
MX28F640C3BTC-90	90	30	5	48 Pin TSOP
MX28F640C3TTC-12	120	30	5	48 Pin TSOP
MX28F640C3BTC-12	120	30	5	48 Pin TSOP
MX28F640C3TTI-90	90	30	5	48 Pin TSOP
MX28F640C3BTI-90	90	30	5	48 Pin TSOP
MX28F640C3TTI-12	120	30	5	48 Pin TSOP
MX28F640C3BTI-12	120	30	5	48 Pin TSOP
MX28F640C3TXAC-90	90	30	5	48 Ball CSP
MX28F640C3BXAC-90	90	30	5	48 Ball CSP
MX28F640C3TXAC-12	120	30	5	48 Ball CSP
MX28F640C3BXAC-12	120	30	5	48 Ball CSP
MX28F640C3TXAI-90	90	30	5	48 Ball CSP
MX28F640C3BXAI-90	90	30	5	48 Ball CSP
MX28F640C3TXAI-12	120	30	5	48 Ball CSP
MX28F640C3BXAI-12	120	30	5	48 Ball CSP

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



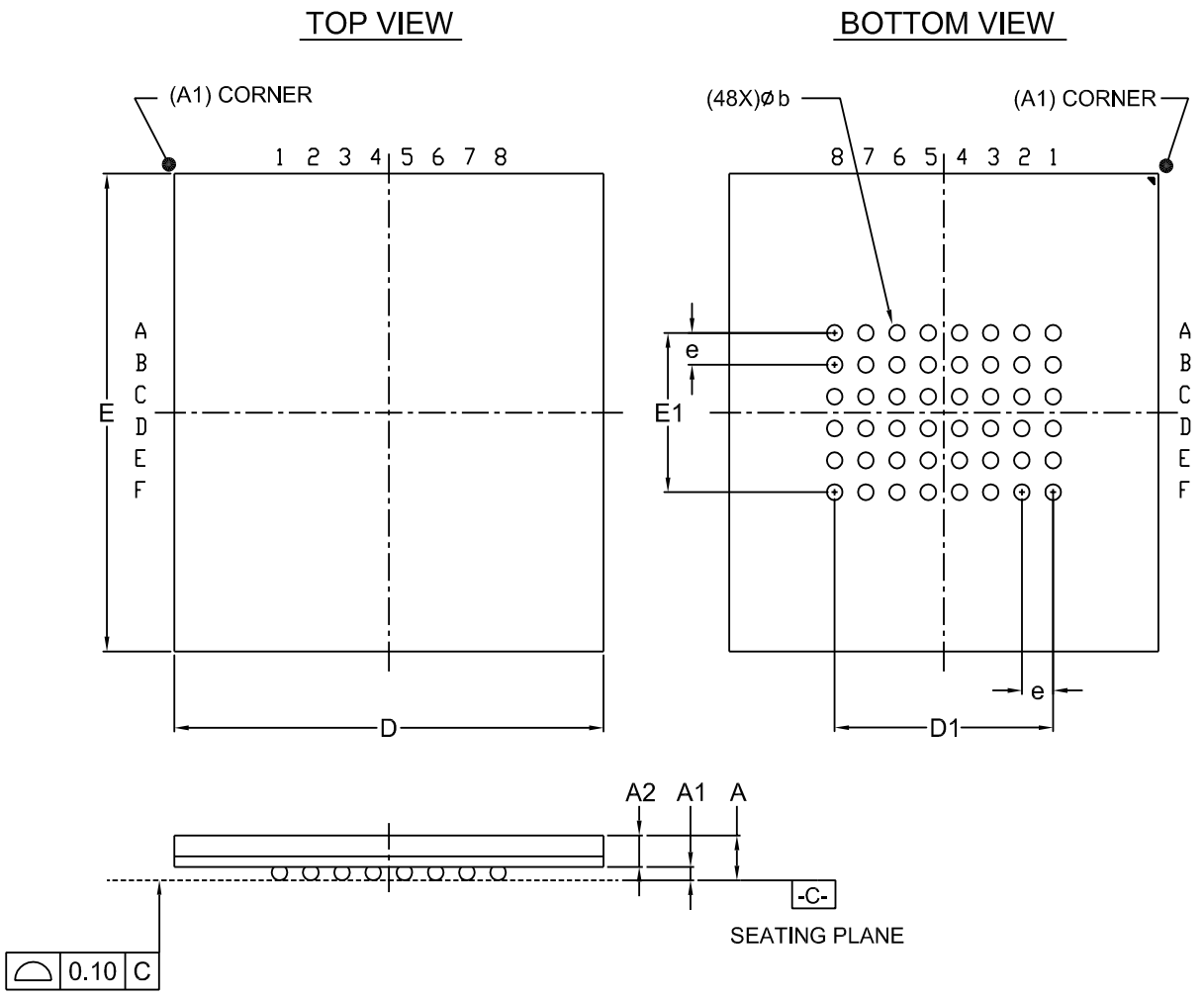
DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-'02

Title: **Package Outline for CSP 48BALL(11X12X1.2MM,BALL PITCH 0.75MM,BALL DIAMETER 0.35MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.22	0.65	0.30	10.90		11.90		
	Nom.	---	0.27	--	0.35	11.00	5.25	12.00	3.75	0.75
	Max.	1.20	0.32	--	0.40	11.10		12.10		
Inch	Min.	---	0.009	0.026	0.012	0.429		0.469		
	Nom.	---	0.011	---	0.014	0.433	0.207	0.472	0.148	0.030
	Max.	0.047	0.013	---	0.016	0.437		0.476		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4225	1	MO-207			07-31-'02

REVISION HISTORY

Revision No.	Description	Page	Date
0.1	Revise 48-ball CSP size	P1,4	FEB/19/2002
0.2	1. Remove 70ns speed information	P1,2,26,28,43	JUN/19/2002
	2. To added the 48 CSP package size	P1,4	
	3. Correct content error	P22	
	4. Modified the testing load circuit & test spec	P25	
0.3	1. To modify Package Information	P44,45	NOV/21/2002
0.4	1. Correct wording error:RP-->RESET, word/byte-->word, DQ-->Q	All	JAN/22/2003
	2. To change the voltage range of VCCQ pin from 1.65V~3.6V to 2.7V~3.6V	P1,5,21,29,30	
	3. Correct the sector range of sector structure table	P7,8	
	4. To modify the locking operation flowchart	P35	
	5. To correct the CFI table	P38,39	
0.5	1. To added address definition notes for Top/Bottom boot device of Protection Register Section	P20	MAY/05/2003
0.6	1. Removed VPP fast programming function	P5,21,26,27 29,30,37~39	AUG/20/2003

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com